An Analog Silicon Retina With Multichip Configuration

Seiji Kameda and Tetsuya Yagi

***Abstract*—The neuromorphic silicon retina is a novel analog very large scale integrated circuit that emulates the structure and the function of the retinal neuronal circuit. We fabricated a neuromorphic silicon retina, in which sample/hold circuits were embedded to generate fluctuation-suppressed outputs in the previous study [1]. The applications of this silicon retina, however, are limited because of a low spatial resolution and computational variability. In this paper, we have fabricated a multichip silicon retina in which the functional network circuits are divided into two chips: the photoreceptor network chip (P chip) and the horizontal cell network chip (H chip). The output images of the P chip are transferred to the H chip with analog voltages through the line-parallel transfer bus. The sample/hold circuits embedded in the P and H chips compensate for the pattern noise generated on the circuits, including the analog communication pathway. Using the multichip silicon retina together with an off-chip differential amplifier, spatial filtering of the image with an odd- and an even-symmetric orientation selective receptive fields was carried out in real time. The analog data transfer method in the present multichip silicon retina is useful to design analog neuromorphic multichip systems that mimic the hierarchical structure of neuronal networks in the visual system.**

***Index Terms*—Analog VLSI, multichip, neuromorphic sensor, real time image processing, robot vision, silicon retina.**

I. Introduction

THE visual information is processed by the retinal circuit following photo-transduction in the photoreceptors. The retinal circuit consists of several hierarchically arranged layers of neuronal syncytia that are relevant to lateral interactions among homogeneous type of neurons. Inspired by this unique architecture of the retinal circuit, neuromorphic silicon retinas, novel analog very large scale integrated (aVLSI) circuits, have been fabricated ([2]–[4] for outlines). The architecture of the neuromorphic chip becomes more complex to implement details of the retinal circuit [5], [6]. These neuromorphic chips, however, always encounter an intrinsic problem, namely, the tradeoff between the resolution and the computational complexity of the chip. Moreover, computations carried out on a single-chip are restricted, since the silicon retina computes an image with the physical properties of the built-in aVLSI circuit embedded on the chip. In the previous study, we fabricated a single-chip silicon retina that calculates spatial and temporal derivatives [1]. This silicon retina also encountered the same problem raised above, and, therefore, the applications of the silicon retina are confined. One of the feasible strategies to solve the problem, albeit only partially, is to divide the circuit into separate chips and carry out the computation in conjunction with simple off-chip circuits.

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S. Kameda was with the Department of Electronic Engineering, Graduate School of Engineering, Osaka University, Osaka 565-0871 Japan. He is now with the Graduate School of Advanced Sciences of Matter, Hiroshima University, Hiroshima, Japan (e-mail: kameda@dsl.hiroshima-u.ac.jp).

T. Yagi is with the Department of Electronic Engineering, Graduate School of Engineering, Osaka University, Osaka 565-0871, Japan (e-mail: yagi@ele.eng.osaka-u.ac.jp).

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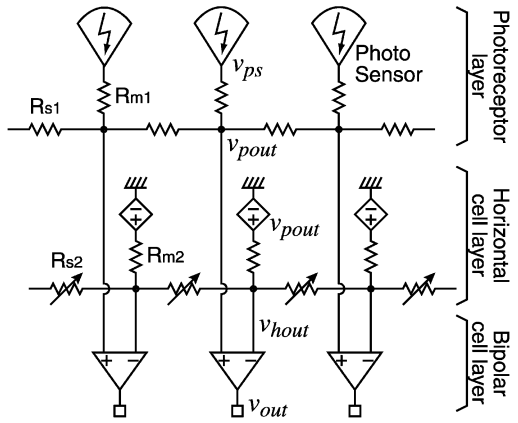

Fig. 1. Outer retinal circuit model. The model consists of two resistive network layers and a differential amplifier layer. In the vertebrate retina, the first and second resistive networks represent a photoreceptor and horizontal cell layers, respectively. The differential amplifier layer represents a bipolar cell layer and takes the difference between two resistive networks. The receptive field is approximated by the $\nabla^2 G$ filter.

In previous studies, the multichip systems have been fabricated [7]–[13]. In these multichip systems, high resolution and advanced functions are realized using the address event representation (AER) for data transfer between chips [14]–[17]. The AER preserves the continuous time nature of neural processing in the brain, and is advantageous in terms of low power communication.

In this paper, we have fabricated a multichip silicon retina, in which the functional network circuits are divided and fabricated in separate chips. These separate chips are linked by a line-parallel transfer bus and communicate with analog signals under conditions of synchronous discrete time sampling. The analog image transfer method employed in the present multichip is thought to be suitable to engineering applications with regard to compatibility with the conventional image processing systems. Using the multichip silicon retina in combination with an off-chip differential amplifier under a control by field programmable gate array (FPGA) logic, even- and odd-symmetric orientation selective filterings were carried out in real time.

II. Multichip Silicon Retina

The outer retinal circuit consisting of the photoreceptor, the horizontal cell and the bipolar cell, has been described as a two layers of resistive network [18], [19] as shown in Fig. 1. In

Fig. 1, the first resistive network represents the photoreceptor layer, and the second one represents the horizontal cell layer of the vertebrate retina. Each resistive network has a different tightness of electrical coupling between neighboring nodes. In our previous study, this network model was fabricated on a single-chip [1]. In this paper, each resistive network was fabricated on a separate chip. By being fabricated in such a way, the spatial resolution of the chip can be increased and more flexible computations can be carried out as will be shown later.

The previously fabricated single-chip silicon retina emulates the sustained and transient responses found in the vertebrate retina [1]. The single-chip silicon retina, however, includes two layers of resistive networks and two arrays of sample/hold (S/H) circuits, besides the photo sensors. Therefore, the circuits following the photo sensors occupy a significant chip area, which limits the fill factor and resolution. To overcome this problem, the circuits embedded in the single-chip were divided and fabricated into two separate chips: a photoreceptor network chip and a horizontal cell network chip. The photoreceptor network chip (P chip) corresponds to the first resistive network and the horizontal cell network chip (H chip) corresponds to the second resistive network.

A. Circuit Designs

Fig. 2(A) shows the circuit design depicting a single pixel of the P chip. In the P chip, an image is obtained by the photo sensors. The photo sensor is an active pixel sensor (APS) that consists of a standard n+/Psub photo-diode and a source-follower circuit [20], [21]. The APS has a high sensitivity to light, by accumulating the photoelectron in the parasitic capacitor of the photo-diode. A dynamic range of the photo sensor can be controlled by changing the accumulation time. The image is smoothed by a resistive network that corresponds to the first resistive network of the previous single-chip silicon retina. The resistive network consists of a MOS resistor [3], [22]. Fig. 2(B) shows the detailed design of the resistive network. The resistances of MOS resistors can be controlled by external bias voltages ($V_{\rm bm1}, V_{\rm bs1}, V_{\rm bm2}$, and $V_{\rm bs2}$), and the variable range of the resistance depends on the PMOS transistor aspect ratio W/L. The extent of smoothing can be controlled by external bias voltages applied to the MOS resistors, and the variable range of smoothing is determined by the ratio between the resistances of the $\rm R_{m1}$ and $\rm R_{s1}$. The S/H circuits, Nbuf1, consists of a wide range amplifier [Fig. 2(C)] and two capacitors, and is embedded to compensate for the circuit offsets, namely, the amplifier offset and the fixed pattern noise due to the statistical mismatch of transistor characteristics [23], [24]. The offset compensation on each chip is indispensable to the multichip silicon retina. A current applied to the amplifier is about 10 μA, which comprises a large percentage of a current applied to the pixel circuit in order to speed up a read time of output voltages.

Fig. 3(A) shows a circuit design depicting a single pixel of the H chip. The input to the H chip pixel from the corresponding P chip pixel, $v_{\rm hi}$, is stored in an analog memory (AMem). Fig. 3(B) shows the detailed design of the analog memory, which consists of a capacitor and a voltage follower with a transconductance amplifier [3]. The stored voltage is smoothed by the resistive network of the H chip, corresponding

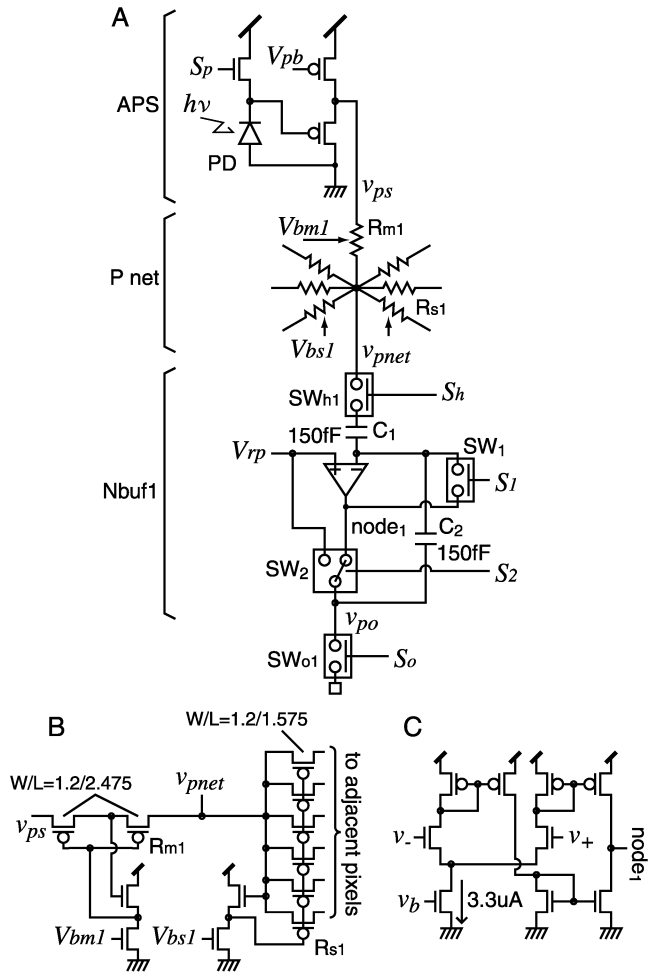

Fig. 2. A: Circuit design depicting the single pixel of the photoreceptor network chip (P chip). The pixel circuit consists of a photo sensor (APS), a resistive network (P net), and a S/H circuit (Nbuf1). B: Detailed design of the P net. The P net is controlled separately by two MOS resistors, $\rm R_{m1}$ and $\rm R_{s1}$. Therefore, an extent of smoothing is controlled by bias voltages, $V_{\rm bm1}$ and $V_{\rm bs1}$. C: Detailed design of a wide range amplifier of the Nbuf1 [3]. A current applied to the amplifier is about 10 mA. A transmission gate is used on each of the switches, $\rm SW_x$.

to the second resistive network of the single-chip silicon retina. Fig. 3(C) shows the detailed design of the resistive network. The extent of smoothing is controllable by external bias voltages ($V_{\rm bm2}, V_{\rm bs2}x, V_{\rm bs2}y$, and $V_{\rm bs2}z$). Note that the electrical coupling can be modulated in one of three orientations since the bias voltages ($V_{\rm bs2}x, V_{\rm bs2}y$, and $V_{\rm bs2}z$) are controlled independently. The variable range of smoothing of the H chip is larger than that of the P chip. S/H circuits, which are the same as the P chip, compensate for the pattern noise generated on the transfer bus as well as the circuit offsets of the H chip.

Fig. 4 illustrates a block diagram depicting the pixel arrangement of the P and H chips. In the P chip, the photo-diodes (PD: shadowed squares) are arranged on a hexagonal grid for better circular symmetry, as well as for better spatial sampling efficiency compared to a square grid [3], [25]. The output of a pixel selected by the vertical and the horizontal shift registers (VSR and HSR) is read out successively: the outputs of P chip pixels are transferred to the H chip using a line parallel method, in which the outputs of the pixels in the same row are read out and

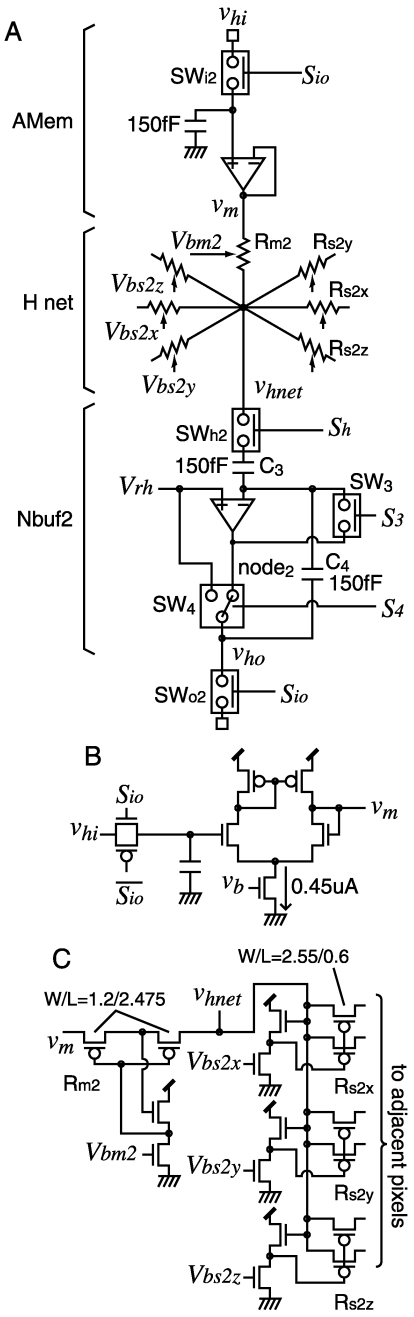

Fig. 3. A: Circuit design depicting the single pixel of the horizontal cell network chip (H chip). The pixel circuit consists of an analog memory (AMem), a resistive network (H net), and a S/H circuit (Nbuf2). B: Detailed design of the AMem. A current applied to the AMem is 0.45 μA and is much less than that applied to the Nbuf2. C: Detailed design of the H net. The H net is controlled separately by four MOS resistors: $\mathrm{R_{m2}}, \mathrm{R_{s2x}}, \mathrm{R_{s2y}}$, and $\mathrm{R_{s2z}}$. Therefore, an extent of smoothing and an orientation of electrical coupling are controlled by bias voltages, $V_{\mathrm{bm2}}, V_{\mathrm{bs2}x}, V_{\mathrm{bs2}y}$, and $V_{\mathrm{bs2}z}$. The Nbuf2 is the same design as the Nbuf1 of the P chip.

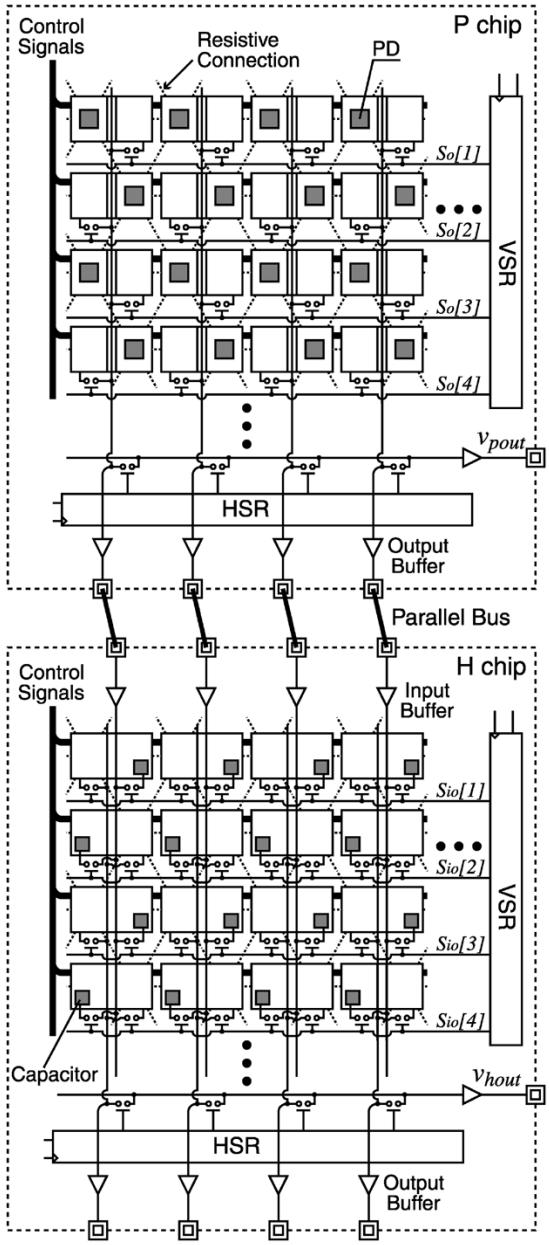

Fig. 4. Block diagrams of the photoreceptor network chip (P chip: top) and the horizontal network chip (H chip: bottom). These chips consist of a pixel array, VSR (vertical shift register), HSR (vertical shift register), and line parallel input/output buffers. In the P chip, the photo-diodes (PD: shadowed) are arranged on a hexagonal grid. The P and H chips are connected by a parallel bus. Each row of output selected by the VSR of the P chip is transferred to a corresponding row of the H chip pixel array through the parallel bus. Outputs of the P and H chips are read, pixel by pixel, by the VSR, and HSR.

transferred through a parallel bus simultaneously [26]. The line parallel transfer is carried out by the input and output buffers, which are voltage followers with wide range amplifiers. A current applied to the I/O buffer is about 50 μA, in order to drive I/O pads and the transfer bus quickly. Due to the line parallel transfer, the transfer time for one frame takes only less than 100 μs. In the H chip, each pixel is connected to neighboring ones by MOS resistors. The spatial arrangement of pixels is the same as that of the P chip. The image processing can be carried out with externally applied control signals—in this case, generated by a FPGA.

B. Operation of the Line Parallel Data Transfer

The voltages transferred through the separate transfer path in parallel are degraded by the pattern noise due to the statistical mismatch of circuit elements. Fig. 5 shows a schematic diagram of a single transfer path connecting a P chip pixel and corresponding H chip pixel. Circuit elements relevant to the source of the fixed pattern noise on the transfer path are the output buffer in the P chip, the input buffer in the H chip, the analog memory

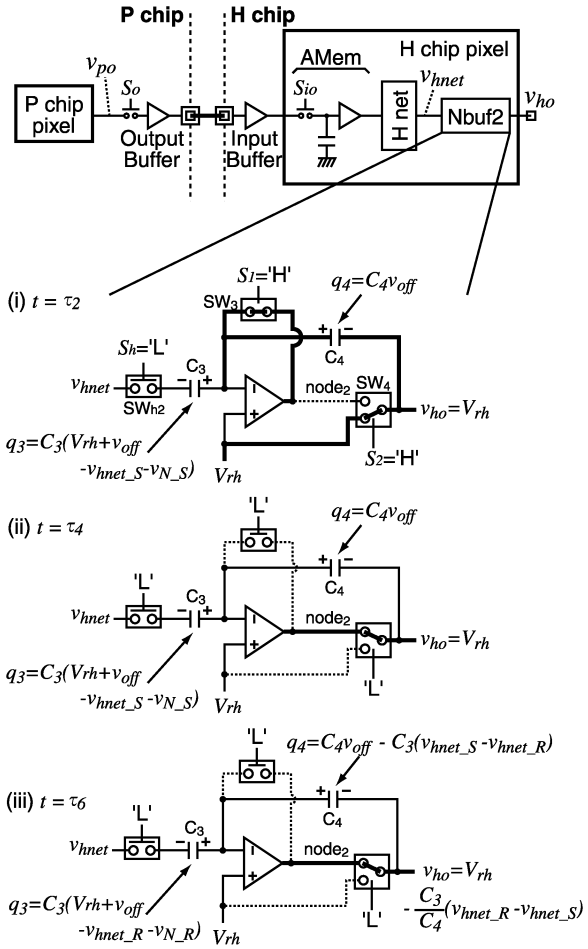

Fig. 5. Schematic diagram of one transfer path from a P chip pixel to (top) an H chip pixel. The left and right rectangles show the P chip pixel and the corresponding H chip pixel, respectively. The bottom shows states of the Nbuf2 at major times of the operation for image transfer in Fig. 6.

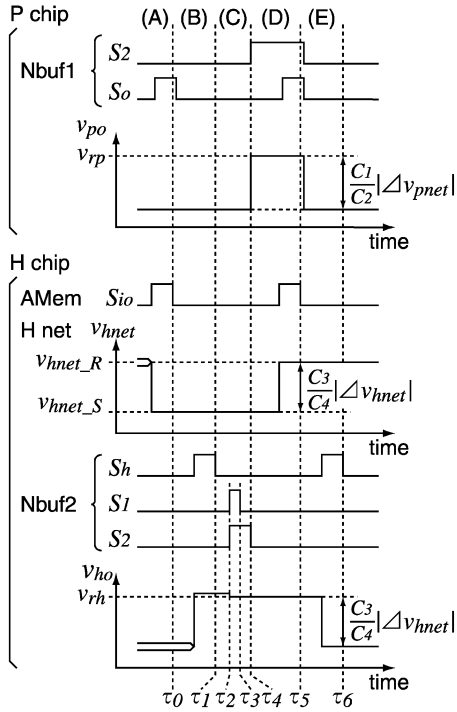

Fig. 6. Operation of data transfer between the P and H chips. Transitions of major responses and control signals on the transfer path are indicated.

buffer in the H chip and the H chip resistive network. In our multichip silicon retina, Nbuf2 of Fig. 3, compensates for the pattern noise.

Fig. 6 demonstrates an operation of the data transfer from the P chip to the H chip. During the period of (A), the output voltage of a P chip pixel, $v_{\rm po}$ of Fig. 2, is obtained as [1]

$$v_{\rm po}(\tau_0) = -\frac{C_1}{C_2}\Delta v_{\rm pnet} + V_{\rm rp} \tag{1}$$

where

$$C_1 = C_2.$$

Here, $\Delta v_{\rm pnet}$ is the light-induced voltage change of the P chip resistive network during the accumulation time. Note that the output voltage of the P chip, $v_{\rm po}$, does not contain fixed-pattern noise occurring in the APS, the P chip resistive network nor the offset of the Nbuf1 since the noise is compensated for by the S/H circuit of the P chip [1]. During the same period, the $\rm SW_{o1}$ of Fig. 2 and $\rm SW_{i2}$ of Fig. 3 are closed to transfer the P chip pixel voltage, $v_{\rm po}(\tau_0)$, to the analog memory of the H chip (read operation), and then disconnected to hold the voltage (write operation). The voltage of the analog memory is smoothed by the H chip resistive network. The smoothed output of the H chip resistive network, $v_{\rm hnet}(\tau_0)$ of Fig. 3, is expressed as

$$v_{\rm hnet}(\tau_0) = v_{\rm hnet\_S} + v_{N\_S}$$

where v_{N_S} is the pattern noise component induced in the transfer path including the output buffer of the P chip, the input buffer of the H chip, the analog memory of the H chip and the H chip resistive network. $v_{\rm hnet\_S}$ represents an image of the H chip resistive network.

At $\rm t = \tau_1$, the $\rm SW_{h2}$ of Fig. 3 is closed to sample $v_{\rm hnet}(\tau_0)$ in the capacitor $\rm C_3$ of Nbuf2, and then disconnected to hold the voltage. This operation is referred to as a sample operation. During the period of (C), an output of the Nbuf2 is reset to the reference voltage $V_{\rm rh}$ as follows. At first, the $\rm SW_3$ of Fig. 3 is closed and the $\rm SW_4$ of Fig. 3 is connected to $V_{\rm rh}$ at $\rm t = \tau_2$ and then the $\rm SW_3$ is opened again at $\rm t = \tau_3$. Here, the inverting node of the Nbuf2 becomes floating and the accumulated charges q_3 and q_4 at $\rm t = \tau_2$ are preserved in the capacitors $\rm C_3$ and $\rm C_4$, respectively. Next, the $\rm SW_4$ is connected to the amplifier output, $\rm node_2$ at $\rm t = \tau_4$. Fig. 5(i) and (ii) shows the states of the Nbuf2 at $\rm t = \tau_2$ and τ_4, respectively. In these cases, the inverting input node voltage of the amplifier v_- is

$$v_- = V_{\rm rh} + v_{\rm off}$$

where $v_{\rm off}$ is an offset of the Nbuf2. Therefore, the accumulated charges of the capacitors $\rm C_3$ and $\rm C_4$ at $\rm t = \tau_4$ are expressed as

$$q_3(\tau_4) = C_3(V_{\rm rh} + v_{\rm off} - v_{\rm hnet\_S} - v_{N\_S}) \tag{2}$$

$$q_4(\tau_4) = C_4 v_{\rm off} \tag{3}$$

respectively. Equations (2) and (3) show that these capacitors store the image signal of the H chip resistive network at $\rm t = \tau_0$,

the pattern noise components and the offset of the Nbuf2. This operation is referred to as a reset operation.

During the period of (D), the output voltage of the P chip pixel, $v_{\rm po}$, is fixed to the reference voltage, $V_{\rm rp}$, for all pixels. This operation is carried out by connecting the $\rm SW_2$ of the Nbuf1 to $V_{\rm rp}$ without destructing the P chip image signal, since $\rm C_1$ and $\rm C_2$ of the Nbuf1 hold the image signal. During this period, the $\rm SW_{o1}$ and $\rm SW_{o2}$ are closed and the reference voltage of the P chip pixel is transferred to and stored in the analog memory of its corresponding H chip pixel. The $\rm SW_{o1}$ and $\rm SW_{o2}$ are opened at $\rm t = \tau_5$ (these operations are referred to as read and write operations of reference voltage). Accordingly, the reference voltage of the H chip resistive network, $v_{\rm hnet}(\tau_5)$, is varied to

$$v_{\rm hnet}(\tau_5) = v_{\rm hnet\_R} + v_{N\_R}.$$

Here, v_{N_R} is the pattern noise component occurring in the transfer path as v_{N_S}. $v_{\rm hnet\_R}$ is the voltage of the H chip resistive network measured when $V_{\rm rp}$, the reference voltage of the Nbuf1 of Pchip, is fed in.

During the period of (E), the $\rm SW_{h2}$ is closed again to memorize the reference voltage of the H chip resistive network, $v_{\rm hnet}(\tau_5)$, in $\rm C_3$ of Nbuf2, and is then disconnected to hold the voltage at $\rm t = \tau_6$ [this is the same as the sample operation during the period of (B)]. Fig. 5(iii) shows the state of Nbuf2 at $\rm t = \tau_6$. The accumulating charge q_3 at $\rm t = \tau_6$ is expressed as

$$q_3(\tau_6) = C_3(V_{\rm rh} + v_{\rm off} - v_{\rm hnet\_R} - v_{N\_R}). \tag{4}$$

The difference between $q_3(\tau_4)$ and $q_3(\tau_6)$ is accumulated in the capacitor $\rm C_4$. The accumulated charge q_4 at $\rm t = \tau_6$ is expressed as

$$\begin{aligned} q_4(\tau_6) &= q_4(\tau_4) + q_3(\tau_4) - q_3(\tau_6) \\ &= C_4 v_{\rm off} - C_3(v_{\rm hnet\_S} - v_{\rm hnet\_R}) \end{aligned} \tag{5}$$

because v_{N_R} is equal to v_{N_S}. Therefore, the output voltage of the H chip pixel of Fig. 3, $v_{\rm ho}$, is expressed as

$$\begin{aligned} v_{ho}(\tau_6) &= v_{\_} - \frac{q_4(\tau_6)}{C_4} \\ &= -\frac{C_3}{C_4}(v_{\rm hnet\_R} - v_{\rm hnet\_S}) + V_{\rm rh} \\ &= -\frac{C_3}{C_4}\Delta v_{\rm hnet} + V_{\rm rh} \end{aligned} \tag{6}$$

where

$$C_3 = C_4.$$

Here, $\Delta v_{\rm hnet}$ represents the output image of the H chip smoothed by the resistive network, and does not contain the pattern noise nor the offset of the Nbuf2.

C. Specifications

The specifications of the multichip silicon retina (the P and H chips) and the single-chip silicon retina are shown in Table I. The multichip and single-chip silicon retinas were implemented with a 0.6 μm, double-poly, three-metal, standard CMOS technology and these die sizes were 8.9×8.9 mm^2. The P and H chips have 70×80 pixels. The pixel area of these chips was 103.5×89.6 μm. The photo diode area was 647.4 μm^2. As is clearly shown, the fill factor and the number of pixels have been improved significantly. The number of pixels has tripled, and the fill factor has more than doubled compared to the single-chip silicon retina. Note that the pixel area of the single-chip is larger than a total pixel area of the P and H chips although the pixel circuit of the single-chip is redistributed to the pixel circuits of the P and H chips with some additional circuits, which are the analog memory and the bias circuits of the H chip resistive network. We reduced wasted spaces and design margins in the pixel layout, which existed in the single-chip, as much as possible. The design margins of source and signal line width were improved. The reduction of the wasted spaces in the P and H chips was easier than in the single-chip because the pixel circuit of the P and H chips had less transistors and simpler design in terms of the hexagonal arrangement.

TABLE I
SPECIFICATIONS OF THE MULTICHIP AND SINGLE-CHIP SILICON RETINAS

	multichip	single-chip[1]
Process	CMOS 0.6um double poly three metal	
Die size [mm^2]	8.9 x 8.9	
Number of pixels [pixel]	70(H) x 80(V)	40(H) x 46(V)
Pixel area [um^2]	103.5 x 89.6 (= 9273.6) 2 : $\sqrt{3}$	178.7 x 154.7 (= 27644.9) 2 : $\sqrt{3}$
PD area [um^2]	647.4	868.0
Fill factor[%]	6.98	3.14
Transistor count/pixel	P chip : 34 H chip : 38	63
Power consumption [mW@3.3V]	P chip : 217.1 H chip : 217.8 - -	power saving off 367.9 power saving on 40.0
Read time [ms/frame]	serial : 3.4 parallel : 0.091	serial : 1.2 -

The power consumptions of the P and H chips were about 220 mW at 3.3-V power supply. These chips had no power-saving function embedded in the single-chip to reduce the power consumption. If the power-saving mode is active, current is not supplied to the S/H circuit array except for the S/H circuit in the row selected by the vertical shift register during a read time. The power-saving function in the single-chip reduced the power consumption to about one-ninth, as shown in Table I. The total power consumption of the P and H chips is the same level as that of the single-chip, although the number of pixels of the P and H chips was tripled. If the power-saving function is embedded in the P and H chips [1], the power consumption will be substantially reduced.

The read time of the P and H chips using a serial method took 3.4 ms and had tripled compared to the single-chip silicon retina due to the increase in pixel count. The read time, however, entailed no adverse consequences for real-time processing, because the read time is sufficiently shorter than the accumulation time of the APS (which is several tens of ms). Furthermore, the read time using a parallel method took only 91 μs. Thus, the line parallel method makes higher speed transfer possible between the chips comprising the multichip system.

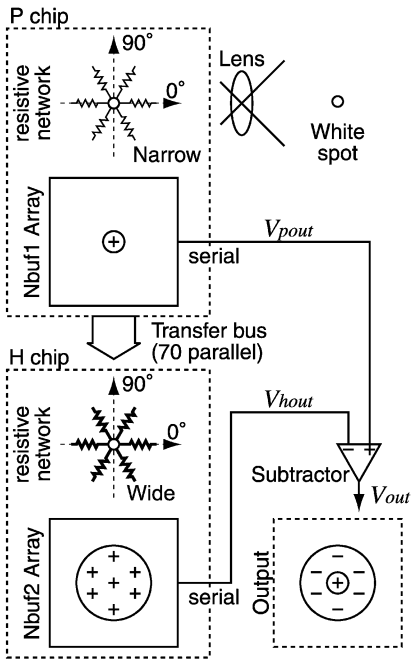

Fig. 7. System design of the multichip silicon retina. The system consists of the P chip, the H chip, and an off-chip subtractor. Two dotted rectangles show the (top) P chip and (bottom) the H chip. In the dotted rectangle, six resistors represent resistances between adjacent pixels at 0°, 60°, and 120° in the resistive network, and wider line represents lower resistance. A square in the dotted rectangle is a processed and stored image in the Nbuf(1,2) array and "+" and "−" represent a positive and negative responses compared with a baseline voltage, respectively.

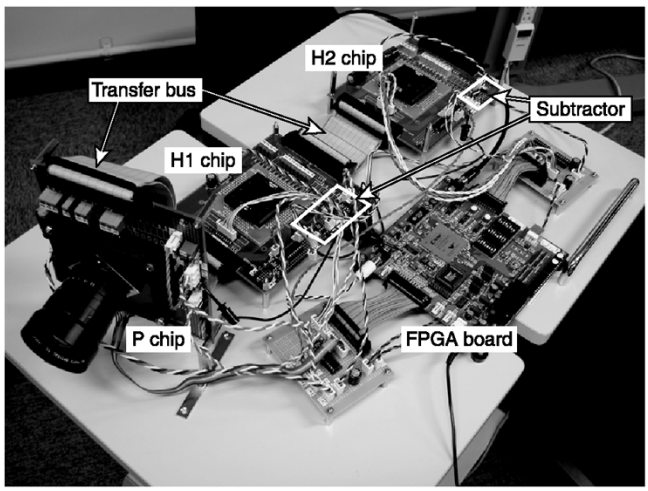

Fig. 8. Overview of the multichip system. In this case, the system consists of a P chip board, two H chip boards, and a FPGA board. Each of the chip boards has the off-chip subtractor. These chip boards are connected by a wire harness.

III. Center-Surround Receptive Field of Multichip Silicon Retina

The multichip silicon retina was configured as illustrated in Fig. 7. A camera lens was mounted on the P chip. The P and H chips were connected by a transfer bus consisting of 70 parallel lines. Output voltages of corresponding pixels in the P and H chips were read out simultaneously and their voltage difference was obtained through an off-chip differencing circuit (subtractor). Fig. 8 shows an overview of the multichip silicon retina. A wire harness was used as the transfer bus. Each chip was controlled by FPGA logic.

The center-surround receptive field of the multichip silicon retina is obtained as follows. First, the APS array outputs a light-induced image for a white spot. The image is smoothed weakly by the resistive network of the P chip. The weakly smoothed image is sampled and held in the Nbuf1 array by the sample operation as in the period (B) of Fig. 6. The Nbuf1 array is reset to output $v_{\rm rp}$ by the reset operation as in the period (C) of Fig. 6. Then, the APS array is initialized by setting S_p high. The initialized voltage of the P chip resistive network is sampled and held in the Nbuf1 array as reference voltage, and is used in pattern noise compensation by the sample operation as in the period of (E) of Fig. 6. Thus, the weakly smoothed spot image is stored in the Nbuf1 array without being influenced by the pattern noise components.

Second, by the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred to the H chip through the line parallel transfer bus by vertical shift register, and is smoothed strongly by the wide receptive field produced by the H chip resistive network. The strongly smoothed image is stored in the Nbuf2 array and is not influenced by the pattern noise components.

Finally, the outputs of the P and H chips are read successively by horizontal and vertical shift registers, and are fed directly into the off-chip subtractor at the same timing. The output of the subtractor $V_{\rm out}$ is expressed as

$$V_{\rm out} = V_{\rm pout} - V_{\rm hout}. \tag{7}$$

This is the difference between the outputs of the two resistive networks. The distribution of $V_{\rm out}$ exhibits the center-surround antagonistic response to the spot image. The receptive field is approximated by the $\nabla^2{\rm G}$ filter. Here, the processing speed of the subtractor is sufficiently faster than the read speed of these chips. Therefore, the subtractor allows real-time processing at the same time as the read operation without time delay. The processing time of the multichip silicon retina containing the transfer time is about 3.6 ms, and is less than the accumulation time; therefore, the system can realize real-time processing.

A. Response to a Black-White Edge

To examine the properties of the center-surround receptive field quantitatively, the voltage response of the multichip silicon retina to a black-white edge was measured. Fig. 9 shows the responses of the P chip (A), the H chip (B), and the off-chip subtractor (C) to the black–white image. The location of the introduced pattern is shown on the top of the figures. The experiment was carried out under indoor illumination (0.65 [W/m^2]). The accumulation time of the photo-sensors was 15.0 ms. The bias voltage applied to the resistive network of the P chip, $V_{\rm bs1}$, was 0.50 V. The bias voltage applied to the resistive network of the H chip $V_{{\rm bs2}\{x,y,z\}}$ varied from 0.45 to 0.85 V. In these figures, the horizontal axis measures the pixel position and the vertical axis measures the pixel voltage of the 40th row of each chip.

As shown in Fig. 9(A), the voltage dropped about 400 mV within six pixels from the black region to the white region. This

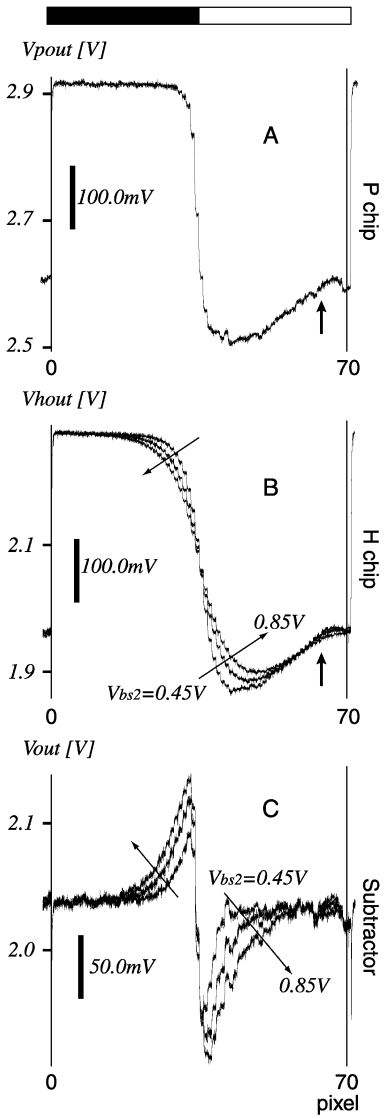

Fig. 9. Responses to a black-white edge obtained from (A) the P chip, (B) the H chip, and (C) the subtractor. The top shows the black-white image presented to the P chip. $V_{\mathrm{bs2}\{x,y,z\}}$ was varied from 0.45 to 0.85 V in the directions of the arrows.

indicates that the edge of the black-white edge was slightly blurred, since the neighboring pixels of the P chip are weakly coupled. The fluctuation of voltage due to the pattern noise was suppressed within 5mV of the black region and 10 mV of the white region with the aid of the S/H circuits. On contrast, the border was strongly blurred in the H chip [Fig. 9(B)]. The fluctuation of voltage is smaller than that of the P chip due to the smoothing effect of the tight electrical coupling between neighboring pixels in the H chip. The border is blurred more as $V_{\mathrm{bs2}\{x,y,z\}}$ is increased because the resistance connecting the neighboring pixels decreases.

The output of the subtractor shows a Mach band-like effect near the black-white border as shown in Fig. 9(C). The receptive field size becomes wider and the response amplitude becomes larger when the resistance of the H chip, $\mathrm{R_{s2}}$ of Fig. 3, is decreased by increasing $V_{\mathrm{bs2}\{x,y,z\}}$ [19], [27]. These properties are thought to be relevant to a part of the neural dark adaptation controlled by the IP cell [28]. The fluctuation is larger in the

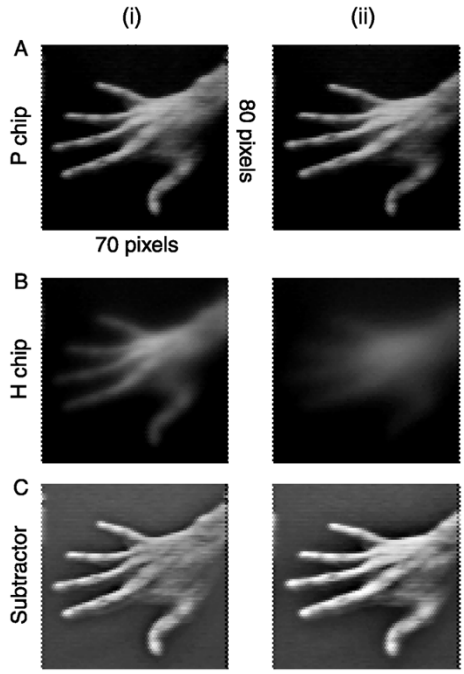

Fig. 10. Responses to a hand obtained from (A) the P chip, (B) the H chip, and (C) the subtractor. The images in column (i) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ is 0.45 V, and the images in column (ii) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ is 0.85 V.

white region but suppressed within 10 mV. A gradual decrease of the amplitude (upward decline indicated by arrows) is seen. The reason for this phenomenon is probably a light falloff or a vignetting due to the mounted lens.

Fig. 10 shows the responses to a hand obtained from the P chip (A), the H chip (B), and the subtractor (C). The hand was presented on a black background. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time of the photo sensors was 33.3 ms. In this case, the bias voltage of the P chip V_{bs1} is 0.0 V and the MOS resistor has high impedance to decouple the neighboring pixels. The images in column (i) were obtained when the bias voltage of the H chip, $V_{\mathrm{bs2}\{x,y,z\}}$, was 0.45 V and the images in column (ii) were obtained when $V_{\mathrm{bs2}\{x,y,z\}}$ was 0.85 V. The responses were displayed with a PC through an interface board. As shown in A-(i) and A-(ii), the hand is clearly captured by the P chip. In contrast, the H chip outputs strongly blurred images as shown in B-(i) and B-(ii). In B-(ii), the image is blurred more strongly and the fingers of the hand are not discernible. C-(i) and C-(ii) show subtraction between these output images and exhibit clear Mach band-like effects around the contour of the hand, indicating that the multichip silicon retina possesses a $\nabla^2\mathrm{G}$-like receptive field. The contour of the hand is enhanced more prominently and the output voltages are smaller in C-(i) than in C-(ii).

B. Effects of Offset Compensation

We verified the effects of the S/H circuit in offset compensation. Statistical mismatch of the transistor characteristics is a bottleneck in the design of analog silicon retinas [3], [29], [30]. The mismatch yields a pattern noise such as the fixed-pattern noise of a photo-sensor [31] and the offset of the amplifier [3]. As a result, the output voltages of the silicon retina become seriously degraded [3]. To compensate for the pattern noise of the

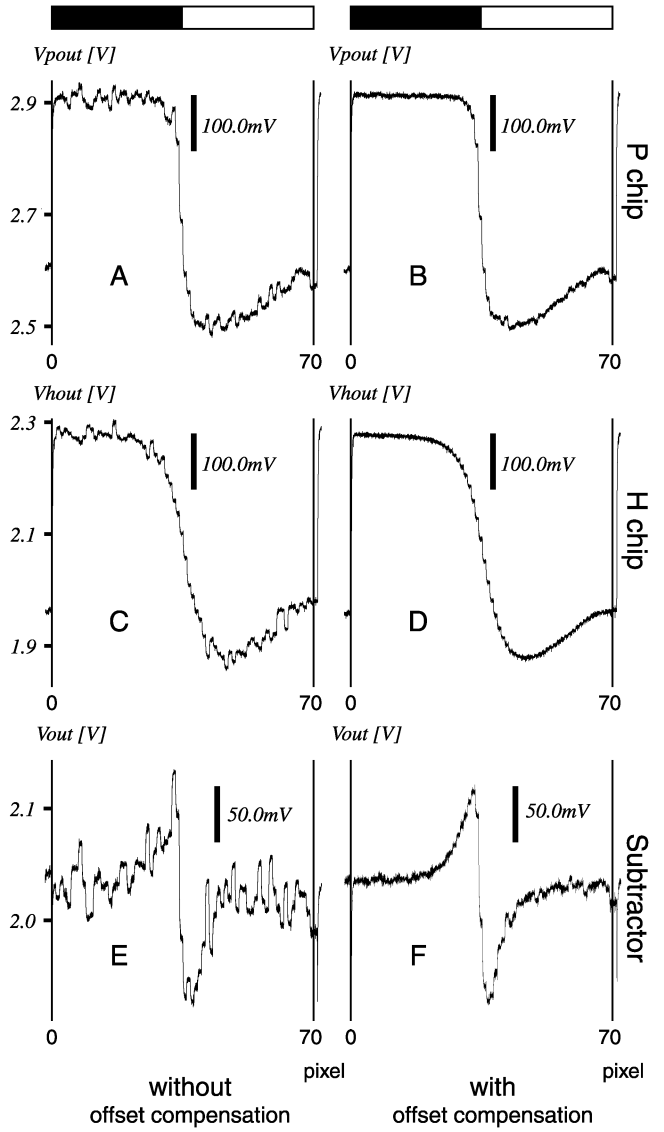

Fig. 11. Effects of offset compensation on the multichip silicon retina. These responses were obtained from (top) the P chip, (middle) the H chip, and (bottom) the subtractor. B, D, and F show the responses obtained when the offset compensation is activated.

P chip, SW_1 is opened first and then SW_2 is connected to the amplifier output, node_1 (Fig. 2). The offset compensation can be deactivated by changing the control sequence. Namely, SW_2 is connected to node_1 first and then SW_1 is opened. In this case, (1) becomes

$$v_{\mathrm{po}} = -\Delta v_{\mathrm{pnet}} + V_{\mathrm{rp}} + v_{\mathrm{off1}}.$$

Here, the offset in Nbuf1 v_{off1} remains. By controlling Nbuf2 in a similar way, (6) becomes

$$v_{\mathrm{ho}} = -\Delta v_{\mathrm{hnet}} + V_{\mathrm{rh}} + v_{\mathrm{off2}}.$$

Here, the offset in Nbuf2 v_{off2} remains.

In Fig. 11, the output voltage of the P chip (A and B), the H chip (C and D), and the subtractor (E and F) in response to a black-white edge are shown to examine the effects of offset compensations. The introduced pattern is illustrated on the top. The experiment was carried out under indoor illumination (0.65 [W/m^2]). The accumulation time of the photo-sensors was 15.0 ms. The bias voltage applied to the resistive network of the P chip V_{bs1} was 0.50 V and to the resistive network of the H chip $V_{\mathrm{bs2}\{x,y,z\}}$ was 0.65 V. In these figures, the horizontal axis measures the pixel position and the vertical axis shows the corresponding pixel voltage of the 40th row of each chip.

Fig. 11(A) and (B) shows the output voltages of the P chip obtained when the offset compensation was deactivated and activated, respectively. As shown in Fig. 11(A), when the compensation was deactivated, the output voltage fluctuates due to the variation of the offset among Nbuf1s. The fluctuation reaches about 40 mV. In contrast, when the compensation was activated as shown in Fig. 11(B), the fluctuation due to the offset was suppressed below 5 mV in the black region. The fluctuation was relatively large in the white region compared to the black region, indicating the gain mismatch among APSs. In this design, this gain mismatch cannot be compensated for; however, the fluctuation caused by the gain mismatch is not as prominent as that caused by the offset.

Fig. 11(C) and (D) shows the output voltages of the H chip. The offset compensation was activated in the P chip in this measurement. Fig. 11(C) was obtained when the offset compensation in the H chip was deactivated, and Fig. 11(D) was obtained when the offset compensation in the H chip was activated. The fluctuation of the voltage among the pixels was prominently reduced below 2 mV by the offset compensation in the H chip. The fluctuation level of the H chip is smaller than that of the P chip due to the tight electrical coupling between the neighboring pixels in the H chip. The voltage fluctuation of the H chip did not change, even when the offset compensation was deactivated in the P chip (not shown). This also suggests that the fluctuation of the P chip output shown in A is smoothed out by the tight electrical coupling among H chip pixels.

Fig. 11(E) shows the output voltage of the subtractor obtained when the offset compensation is deactivated in both chips. Fig. 11(F) shows the output voltage obtained when the compensation is activated in both the P and H chips. When the offset compensation was deactivated in both chips, the fluctuations reached 65 mV at a maximum. In contrast, when the compensation was activated on both chips, the fluctuation in the black region had been drastically reduced to below 5 mV, and those in the white region below 10 mV. These results indicate that the pattern noise due to the amplifier offsets is effectively compensated for by the S/H circuit.

The pattern noise arises, however, from the fixed pattern noise of the APS, the offset of the line parallel I/O buffer, the mismatch of the transistors in the MOS resistors and switches other than the amplifier offsets. Therefore, the signal-to-noise ratio would be worse if the S/H circuits in the chip were completely removed.

C. Chip Response With Different Accumulation Times

In Fig. 12, the responses of the photo sensor with different accumulation times are shown. Fig. 12(A)–(C) shows the responses of the P chip, the H chip and the subtractor, respectively. The introduced pattern is the black-white paper, as shown at the top. The experiment was carried out under indoor illumination

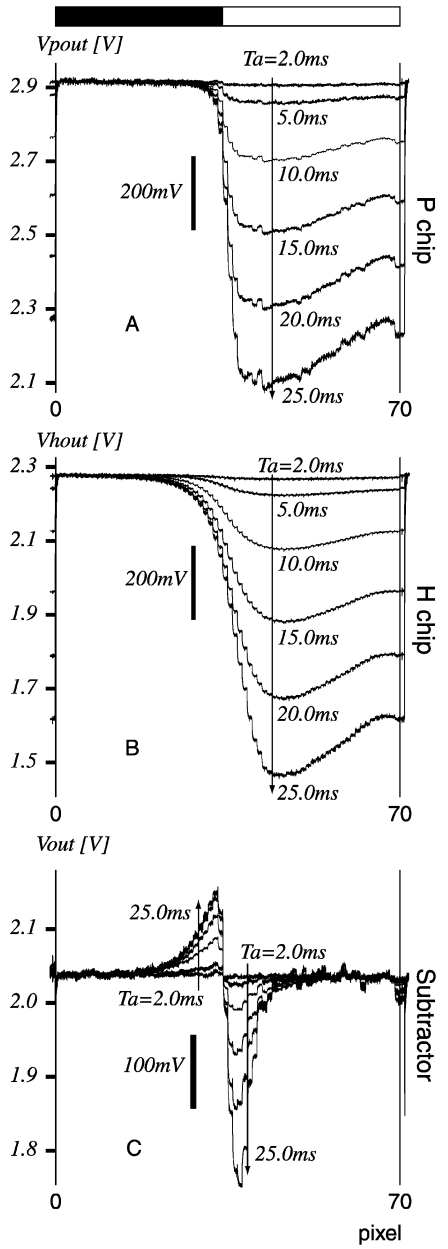

Fig. 12. Responses with different accumulating durations obtained from the (A) P chip, (B) the H chip, and (C) the subtractor. The accumulation time $\mathrm{T_a}$ was changed from 2.0 to 25.0 ms in the directions of the arrows.

(0.65 [W/m^2]). The accumulation time, $\mathrm{T_a}$, was changed from 2.0 to 25.0 ms. In these figures, the horizontal axis measures the pixel position and the vertical axis measures the corresponding voltage output of the 40th row. As shown in Fig. 12(A) and (B), the voltage drops of the P and H chips in the white region become larger as the accumulation time is increased. The increase of the voltage drop is relatively linear with respect to the intensity of light within these accumulation times. As shown in Fig. 12(C), the response of the subtractor also increases as the accumulation time increased. However, the amplitude of the response is asymmetric to the border of the black-white image. This is because the resistance of the MOS resistor varies with the bias voltage of the input terminal. The current of the MOS resistor increases nonlinearly by the body effect as the bias voltage level of the terminal increases even if the potential difference

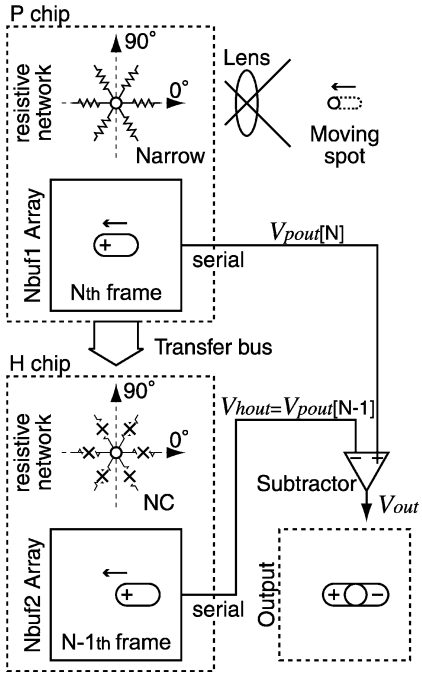

Fig. 13. System design for the frame subtraction. The system is the same configuration as the multichip silicon retina. A "×" on the resistance in the H chip square represents that the resistance has high impedance. The H chip serves as a frame memory when the resistances of $\mathrm{R_{s2\{x,y,z\}}}$ have high impedance.

between two input terminals of the MOS resistor remains constant. Therefore, the space constant of the resistive network is different between the black and white regions. The baseline of the subtractor's response, however, does not change regardless of the accumulation time.

IV. Application

The advantage of the present multichip silicon retina is not limited to the improvement of pixel resolution. Some useful spatiotemporal filtering functions can be achieved with the multichip system by changing the control signal and the chip configuration.

A. Frame Subtraction

The detection (or segmentation) of moving objects is a basic task of computer vision. Frame subtraction is a standard technique for motion detection. Namely, subtraction of the current frame from the previous frame will remove most of the static background and extract only moving objects. The motion detection chips using the frame subtraction technique have been fabricated [20], [32] including the single-chip silicon retina of our previous study. The multichip silicon retina can also perform the frame subtraction using the same configuration as the ∇^2G-like filtering in the Section III.

Fig. 13 shows a system design for frame subtraction. The system consists of the P chip, the H chip, and the subtractor. The P chip outputs the current frame image and transfers to the H chip under which the bias voltage $V_{\mathrm{bs2}\{x,y,z\}}$ of the H chip is 0.0 V so that the MOS resistor $\mathrm{R_{s2\{x,y,z\}}}$ decouples the neighboring pixels. In this condition, the H chip serves as a frame memory that stores the previous frame image of the P chip. The

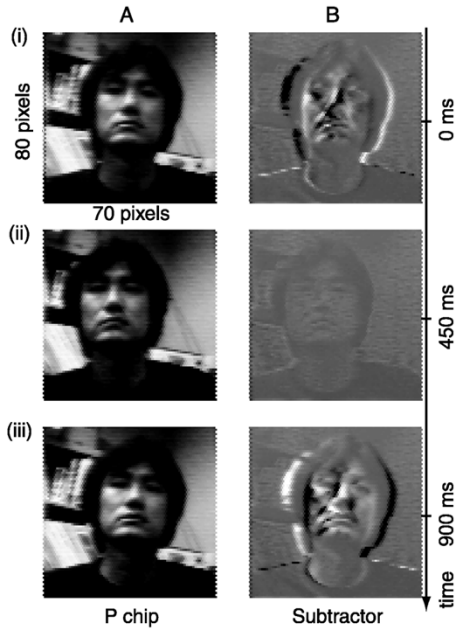

Fig. 14. Responses to a moving face obtained from (A) the P chip and (B) the subtractor by the frame subtraction. Times obtained with these images are indicated on the right side.

current and previous images are read out from these chips sequentially at the same timing and the frame subtraction is obtained through the off-chip subtractor.

Fig. 14 shows the response to a face obtained by the frame subtraction operation. The experiment was carried out under the same conditions as Fig. 10. The accumulation time of the photo sensors was 50 ms. In this case, the bias voltage of the P chip, $V_{\rm bs1}$, was 0.0 V. The face was moved right and left in front of the lens mounted on the chip. Each frame represents output images of the P chip and the subtractor picked up once every nine frames at a time indicated right side. The face was moving from right to left at 0 and 450 ms, and from right to left at 450 to 900 ms. At the time that the face was moving (0 and 900 ms), the moving face image of the subtractor was represented and the static background disappeared. And at the time that the face almost stopped (450 ms), the face image also disappeared.

B. Odd-Symmetric Orientation Selective Filter

In the digital image processing, the Sobel operator performs discrete differentiation on the image using small conventional masks to approximate the first derivative [33]. This operator takes the derivative in one direction, and smoothes in the orthogonal direction and is designed to respond maximally to edges running along the direction of smoothing.

A Sobel-like odd-symmetric receptive field is obtained by the multichip silicon retina. Fig. 15 shows a system design for the Sobel-like filtering. In Fig. 15, $V_{h1\rm out}(i,j)$ and $V_{h2\rm out}(i,j)$ are the output voltage of the pixel at $(\rm i,j)$ from the H1 chip and H2 chip, respectively. The system consists of the P chip, two H chips (H1 chip and H2 chip) and the subtractor. The H1 chip smoothes the image obtained from the P chip by the resistive network connected at one of three orientations. The H2 chip stores the elongated image of the H1 chip, without smoothing by the resistive network of the H2 chip. Thus, the H1 and H2 chips store the same image. The H1 and H2 chips output the elongated images

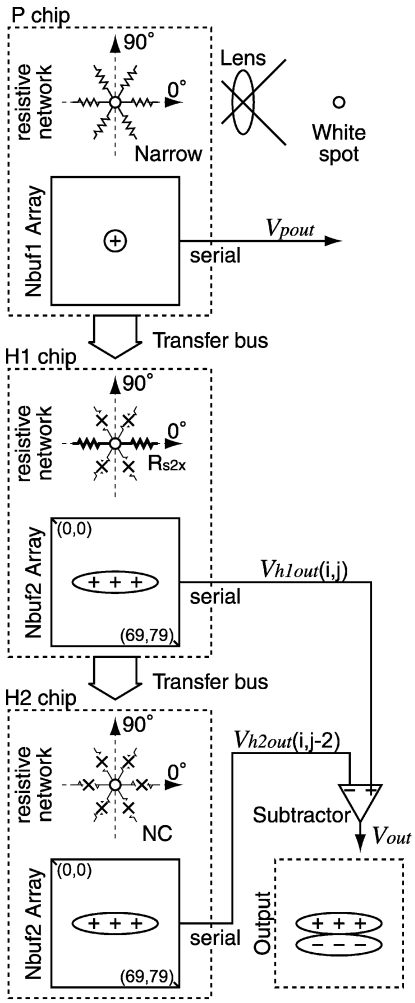

Fig. 15. System design for the Sobel-like odd-symmetric orientation selective filter. The system consists of the P chip, two H chips, and the off-chip subtractor.

to the off-chip subtractor sequentially. However, the timing of the readout in the H2 chip delays by a few columns and/or rows (two rows in this case), and outputs $V_{h1\rm out(i,j-2)}$. Accordingly, the subtractor takes the derivative in one direction and the output of the subtractor is

$$V_{\rm out}(i,j-1) = V_{h1\rm out}(i,j) - V_{h1\rm out}(i,j-2). \qquad (8)$$

This is the difference between the jth and $(j-2)$th row of the image elongated at horizontal orientation. Thus, the multichip system takes the derivative in the vertical direction and smoothes in the horizontal direction. The filter property is similar to the Sobel operator, since the smoothing function by the resistive network is approximated by the exponential function. Note that the filter size is easily controllable by modulating the bias voltage of the resistive network and the readout timing of the H2 chip. The processing time of the Sobel-like filtering including the transfer time is about 3.8 ms and is less than the accumulation time.

Fig. 16 shows the responses of the P chip (A) and the H2 chip (B and C) obtained by the Sobel-like operation. Fig. 16(B) shows the responses obtained when the resistive network of the H1 chip was connected at 0° and the timing of the H2 chip readout was delayed by two rows. Fig. 16(C) shows the responses obtained when the resistive network of the H1 chip was

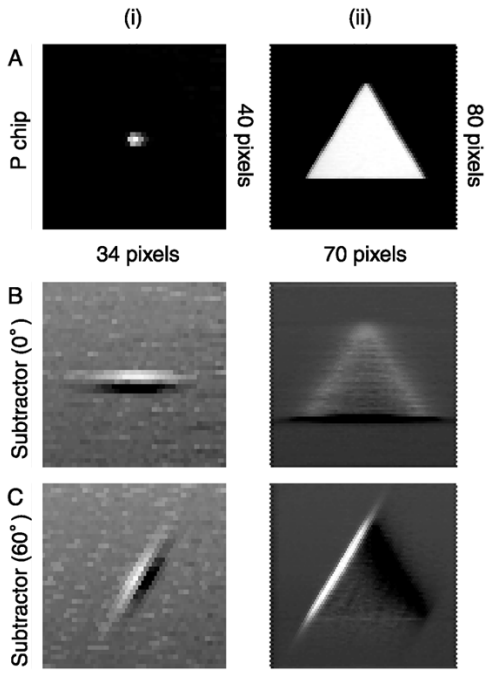

Fig. 16. Responses of the Sobel-like first derivative filtering to (i) a white spot and (ii) an equilateral triangle. A shows the responses obtained from the P chip. B and C show the responses obtained when the H net of the H1 chip was connected at 0° and 60° and the timing of the H2 chip readout was delayed by two rows and columns, respectively.

connected at 60° and the readout timing of the H2 chip was delayed by two columns. The images in column (i) were obtained when a white spot on a black background was presented, and the images in column (ii) were obtained when a equilateral triangle on a black background was presented. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time was 33.3 ms. The bias voltage of the P chip $V_{\rm bs1}$ was 0.0 V, and the bias voltage of the H1 chip $V_{\rm bs2}x$ or $V_{\rm bs2}y$ was 0.85 V. As shown in Fig. 16(B)-(i) and (C)-(i), elongated responses are arranged odd-symmetrically at 0° and 60° orientations, respectively. As shown in Fig. 16(B)-(i) and (B)-(ii), only one side of the triangle matching the preferred orientation is extracted while the other sides are blurred.

C. Even-Symmetric Orientation Selective Filter

An even-symmetric derivative filter can be also obtained with the multichip silicon retina. The center-surround receptive fields are smoothed for one orientation by two separate resistive networks and then the difference of these receptive fields is obtained by the subtractor. Fig. 17 shows a system design for even-symmetric orientation selective filtering. The system consists of a P chip and two H chips (H1 chip and H2 chip). The H1 chip outputs the center-surround responses generated with and without resistive coupling to the H2 chip in sequential order. The H2 chip smoothes these responses by the resistive network connected at one orientation and subtracts these elongated responses by the Nbuf2 array.

Fig. 17 demonstrates the operation for an even-symmetric receptive field oriented at 60°. The P chip takes a white spot image in order to indicate a receptive field of the system. First, the weakly smoothed spot image is stored in the Nbuf1 array.

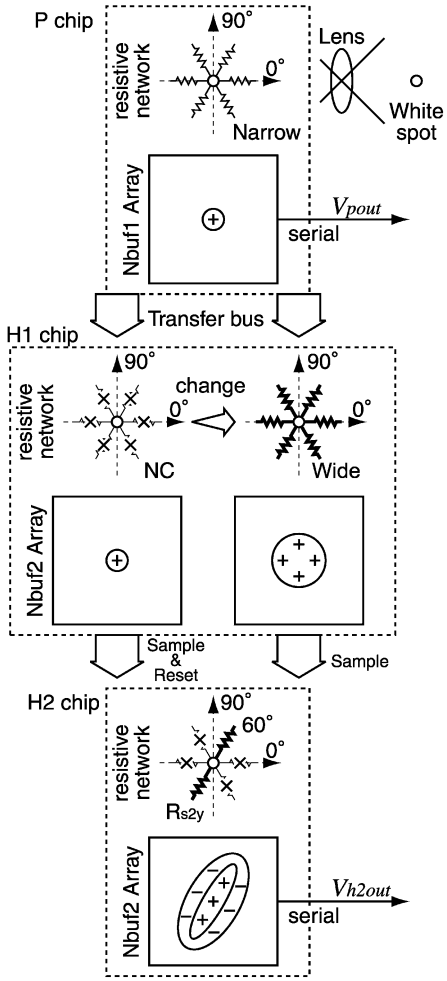

Fig. 17. System design for even-symmetric orientation selective filtering. The system consists of a P chip and two H chips. The H1 chip processes twice the image transfered from the P chip by changing the resistances, $\rm R_{s2\{x,y,z\}}$ and the processed images are transferred to the H2 chip. The H2 chip smoothes these images at one orientation and takes a difference between these elongated images.

Second, using the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred to the H1 chip through the line parallel transfer bus by vertical shift registor. Here, the bias voltage $V_{\rm bs2\{}x,y,z\}$ of the H1 chip is 0.0 V and the MOS resister, $\rm R_{s2\{x,y,z\}}$, decouples the neighboring pixels. Accordingly, the Nbuf2 array of the H1 chip stores the weakly smoothed image of the P chip.

Third, the H2 chip receives the image from the H1 chip and smoothes it at 60° by connecting the lateral MOS resistor $\rm R_{s2y}$ only. Therefore, a narrow and elongated image is produced by the H2 chip resistive network. Then, the Nbuf2 array of the H2 chip is reset while the narrow and elongated image is input by the sample and the reset operation. During the same period, and by the same operation as in Section II-B, the weakly smoothed spot image of the P chip is transferred again to the H1 chip. In this period, the image is smoothed strongly, because the receptive field of the H1 chip resistive network becomes wide due to the bias voltage $V_{\rm bs2\{}x,y,z\}$. Then, the Nbuf2 array of the H1 chip stores the strongly smoothed image.

Finally, the H2 chip receives the strongly smoothed image from the H1 chip and smoothes it at 60°. Therefore, a wide

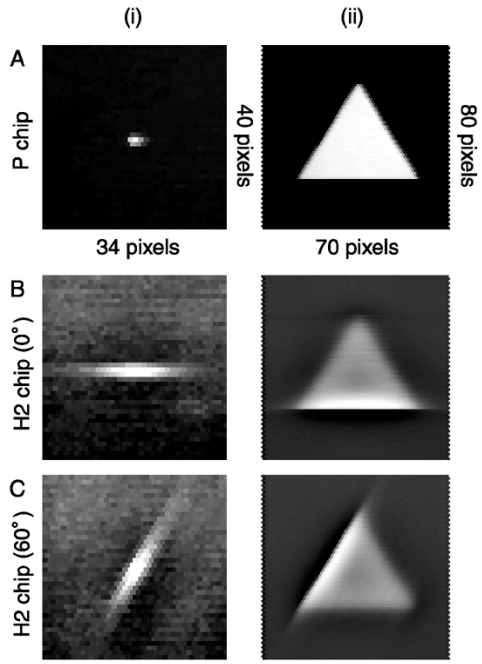

Fig. 18. Responses of the even-symmetric orientation selective filtering to (i) a white spot and (ii) an equilateral triangle. A shows the responses obtained from the P chip. B and C show the responses obtained when the H net of the H2 chip was connected at 0° and 60°.

and elongated image is produced by the H2 chip resistive network. Then, by the sample operation as the period (E) of Fig. 6, the Nbuf2 array of the H2 chip samples the wide and elongated image instead of a reference voltage. By this operation, the Nbuf2 array of the H2 chip can subtract the wide and elongated image from the narrow and elongated image under the compensation of pattern noise components. Therefore, an even-symmetric response oriented at 60° is obtained and stored in the Nbuf2 array of the H2 chip, without being influenced by the pattern noise. The processing time of the even-symmetric filtering, including the transfer time is about 3.9 ms, and is less than the accumulation time.

Fig. 18 shows orientation-selective responses by the even-symmetric filtering obtained from the P chip (A) and the H2 chip [(B) and (C)]. Fig. 18(B) and (C) shows the responses obtained when the resistive network of the H2 chip was connected at 0° and 60°, respectively. The images in column (i) were obtained when a white spot on a black background was presented. The images in column (ii) were obtained when an equilateral triangle on a black background was presented. The experiment was carried out under indoor illumination (0.48 [W/m^2]). The accumulation time was 33.3 ms. The bias voltage of the P chip $V_{\rm bs1}$ was 0.0 V. The bias voltage of the H1 chip $V_{{\rm bs2}\{x,y,z\}}$ was 0.65 V and the bias voltage of the H2 chip, $V_{{\rm bs2}x}$ or $V_{{\rm bs2}y}$, was 0.85 V. As shown in Fig. 18(B)-(i) and C-(i), even-symmetric impulse responses of the preferred orientation at 0° and 60° are exhibited, respectively, since there are positive narrow and elongated responses in the center area and negative responses in the periphery. As shown in Fig. 18(B)-(ii) and C-(ii), only one side of the triangle matching the preferred orientation is extracted, and a Mach band-like effect is seen clearly around the side, while the other sides are blurred.

V. Conclusion and Discussion

In this paper, a multichip silicon retina composed of the photoreceptor network chip and the horizontal cell network chip was fabricated. The analog outputs of the P chip were transferred to the H chip through a line-parallel data transfer bus. The multichip silicon retina realized a ∇^2G-like receptive field, which carried out smoothing and contrast-enhancement on input images with much higher spatial resolution than that fabricated in our previous study. Furthermore, odd- and even-symmetric oriented filters were obtained in real time by the multichip configuration using external control signals and a simple off-chip subtractor.

In most of the previously fabricated multichips [7]–[13], communication has been realized by AER, in which the spike output of each pixel on the sending array is encoded with a unique address [14], [15], [17]. The AER allows communication between an array of silicon neurons in one chip and another chip, with continuous time spike activity over an asynchronous digital bus [7]; it is better suited for chips employing the continuous time photoreceptor [34], [35]. Therefore, the AER emulates the communication mediated by action potentials and provides a unique methodology for studying the computational advantages with the spike representation. On the other hand, image computations are carried out with analog signals within the retinal circuit. Therefore, the analog data transfer method used in the present multichip naturally emulates the computation of the outer retinal circuit. This analog method is better suited for chips employing the sampled receptor, such as the APS, because the output of the every pixel is read successively and is synchronized with a frame period.

The AER protocol has an advantage of low power consumption. It is more efficient than the analog transfer method when the spike activity in the pixel array is sparse. For example, the motion detection chip and the orientation selective chip fabricated previously consumed only a few milliwatts [7], [9]. The power consumption, however, increases in proportion to the spike activity. It possibly becomes comparable to that of the analog transfer method when the spike activity increases to some extent, since the power consumption can be suppressed in the analog transfer method by supplying the current only to the S/H circuits that are selected by the shift resistor during the data transfer period. Furthermore, the possibility of spike collision also increases in the AER.

Recent digital signal processors can carry out simple preprocessing, such as addition, subtraction, small size mask filtering (3×3 and 5×5 for example), etc., in real-time with low power consumption. The traditional PCs can also carry out the simple preprocessing in real-time but with much higher power consumption. However, it is difficult for these conventional systems to conduct spatial filtering with large size masks that are often required in computation of natural scene [36]. The present multichip realizes large size mask filtering with the resistive networks in real-time with low power consumption. For example, in the even-symmetric filtering, the processing time was about 3.9 ms and the power consumption was about 650 mW. The power consumption will be reduced substantially if the power-saving function is embedded in the present multichip [1]. Furthermore, one can easily design a system consisting of multi-

functional modules to obtain the responses shown in Figs. 10, 14, 16, and 18 in parallel. Therefore, the present multichip architecture is able to combine different image features, i.e., edge, motion, and orientation, etc. [37], in real-time. This system is thought to be applicable to image recognition in which that various different image features are required [38]–[40].

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Seiji Kameda received the Ph.D. degree in computer science and system engineering from the Kyushu Institute of Technology, Japan, in 2001.

He was a Postdoctoral Fellow with the Japan Society for the Promotion of Science. Currently, he is a Postdoctoral Fellow with the 21st Century Center-Of-Excellence (COE), Hiroshima University, Hiroshima, Japan. His research interests include the implementation of retinomophic analog VLSI, the design of multichip system emulating visual information processings in the cortex, and their industrial applications.

Tetsuya Yagi received the Ph.D. degree in medical science from Nagoya University, Japan, in 1985, where he studied physics and physiology.

After being a Postdoctoral Fellow with the National Institute of Physiological Science, Okazaki, Japan, and the Rockefeller University, New York, he joined the Kyushu Institute of Technology, Japan, as an Associate Professor in 1990. He is now a Professor with the Department of Electronics, Osaka University. His research interests include neurophysiology of visual systems and neuromorphic engineering systems.