

A Design of Neural Signal Sensing LSI with Multi-Input-Channels

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SUMMARY A neural-signal sensing system with multi-input-channels was designed utilizing a new chopper amplifier with direct connected to a multiplexer. The proposed system consists of multiplexers, chopper amplifiers, a multi-mode analog-to-digital converter (ADC), and a wireless transmitter. It enables to measure 50-channel signals at the same time, which are selected out of 100 channels to detect useful information. The test chip including 10-channel-inputs chopper-amplifier and multi-mode ADC, that was designed and fabricated with a mixed signal 0.35- μm CMOS technology. Utilizing the proposed direct chopper input scheme and the shared chopper amplifier, the circuits was designed with a small area of 9.4 mm². High accuracy channel selecting and multiplexing operations were confirmed, and an equivalent input noise of 10-nV/root-Hz was obtained with test chip measurements. Power dissipation of the chopper amplifier and the ADC were 6.0-mW and 2.5-mW at a 3-V supply voltage, respectively.

key words: neural signal sensing LSI, multi-input-channels probe, flicker noise, chopper amplifier, multi-mode ADC

1. Introduction

The achievement of a neural sensing system with multi-input-channels will contribute to the measurement of the biological behavior of neural networks, and improve the investigation tools for physiology. During the past 30 years, the sensing systems have been implemented in discrete operational-amplifiers (OPAs) fabricated with low-noise JFETs or bipolar transistors, owing to the detection of a neural signal with a-few-kHz and several ten- μV . Usually these systems are large and are applied to a fixed investigation target. In the other approach to measurements of the neural signals under the freely behavioral condition, a telemeter using a frequency modulation (FM) is often used [1]. The system includes 4-JFET-OPAs (TL084 fabricated by Texas Instruments), an antenna coil, bipolar transistors and some passive devices for the detection of a neural signal and it has a large circuit area of 260-mm² and a power consumption of 14.8-mW at a supply voltage of ± 3 V. The analog telemeter system decreases the signal-to-noise ratio (SNR) of the detected neural signals due to the modulator/demodulator noise, such as deviation of the carrier frequency and signal distortion.

In recent years, Si based Microelectromechanical Systems (MEMS) technology has been implemented for neural recording and stimulating systems [2], [3]. The recording system included 4-probes and 4-unity-gain-buffer-amplifiers that were fabricated on the same Si substrate and the system achieved to observe multi-point neural signals simultaneously. However, the system increases in size and power dissipation when the number of probes increases, because of each probe needs a unity-gain buffer, which dissipates 330- μW at a supply voltage of 5 V.

Using mixed-signal CMOS-LSI technology, the system enables total integration of functional blocks: multiplexer (MUX), amplifiers, an analog-to-digital converter (ADC) and a wireless transmitter/receiver with a digital modulation (TX/RX) on a small chip, and reduces power consumption. Digitized measurement data is transmitted by a digital wireless communication system, such as frequency-shift-keying (FSK) and phase-shift-keying (PSK), without degradation of the measured signal quality. The CMOS-LSI technology has major problems with the CMOS amplifier, such as large flicker noise and dc offset voltage. Although these problems are reduced by low-noise circuit techniques, such as chopper stabilizing and auto zeroing [4]–[6], these techniques attenuate the input-impedance of the amplifier.

In this work, we propose the architecture for a neural signal sensing system with selectable multi-input-channels to be worn by a small animal. The proposed sensing system LSI includes a multiplexer with selector, a low-noise chopper amplifier and a multi-mode ADC, which is designed with conventional mixed-signal CMOS technology. The proposed circuit performance is evaluated by SPICE simulation and measurement results of a test chip.

2. System Architecture

Figure 1 shows a block diagram of the proposed multi-channel neural sensing system. A maximum of 100 sensing channels, consisting of 10-probes, are required to analyze the complex behavior of a large-scale neural network. To implement the system, we proposed sensing LSI that has 10 multiplexer/amplifier (MUX/AMP) blocks for the 10-probes, an ADC block and a wireless TX/RX block.

The 10-ch probe has 10-tungsten-needles in a local area of 2-mm- ϕ , it enables the system to observe waveforms of various neurons, which means a different type, size and distance. The 10-ch probe microphotograph is shown in Fig. 2.

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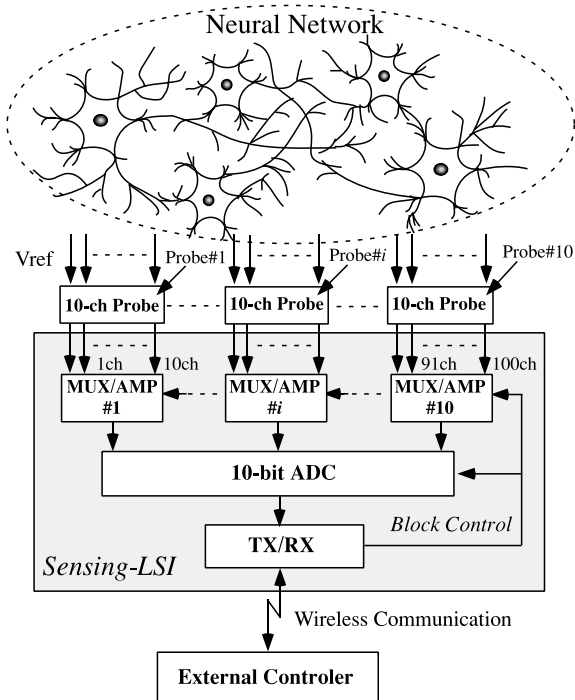


Fig. 1 Proposed neural signal sensing system.

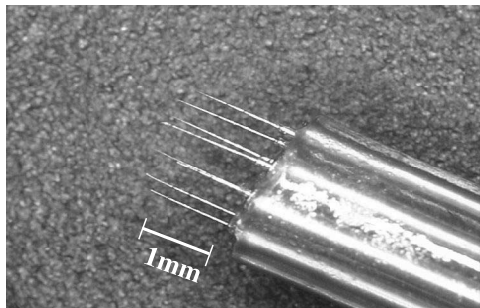


Fig. 2 Probe microphotograph.

Using packaging technology for LSI, it is possible to connect the 10-ch probe and the sensing LSI. Furthermore, recent MEMS technologies will be able to integrate the probes on a chip. A connection diagram of neurons and the 10-ch probe is illustrated in Fig. 3. The needles near the focused neuron are selected by the MUX/AMP block with a selector circuit. A reference voltage (V_{ref}) defines the voltage of cell liquid far from the observation neuron cell. Impedance caused by the polarized charge appears between a cell liquid and needle; this problem will be addressed in Chapter 3.

The neural signals are typically weak (a few ten- μV) and slow (a few kHz). An MUX/AMP block amplifies the difference between a detected voltage near the focused neuron and the V_{ref} . The MUX/AMP needs about 80-dB DC-gain and a reduction of flicker noise and a voltage offset in order to detect weak neural signals. Moreover, the MUX/AMP chooses 5-channels from the 10-ch probe by a block control signal and multiplexes the selected signals

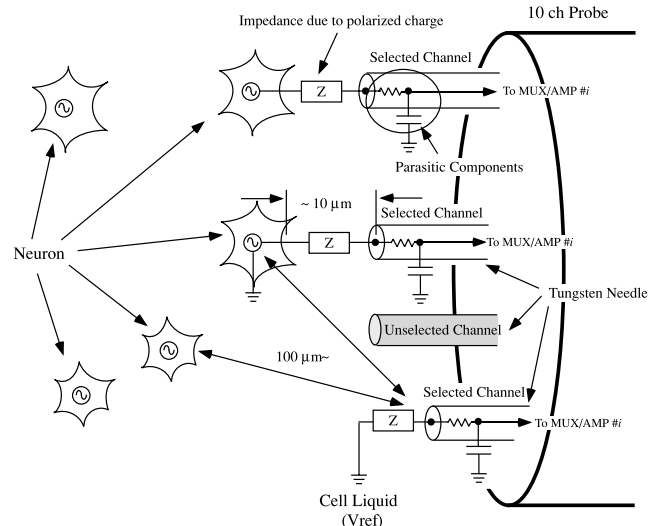


Fig. 3 A connection diagram of neurons and 10-ch probe.

at a pulse width of 20 μs , due to the achievement of 10-k-sampling-per-second (ksps) per channel for ADC block. The proposed system with 10-MUX/AMP-blocks is possible to measure 50-ch neural signals simultaneously.

Applying the digital communication system, the ADC block digitizes the multiplexed 50-ch signal provided by 10-MUX/AMP blocks. Therefore, the maximum sampling frequency of ADC is 500-k-sampling-per-second (ksps). The detected neural signals have various waveforms, such as a value of peak-to-peak and pulse-width, because of the various neuron types and the behavior. We have already implemented in a neural signal observation system using an existing 8-bit ADC. The system enables comparison of a detected waveform and a reference waveform, and identifies the kind of neurons on PC software. From the experimental results, the ADC requires an accuracy above 8-bit for analyzing various neural waveforms. Furthermore, the system includes a high-accuracy ADC, enabling application of a varied sensing system. The ADC also operates with three-modes to achieve effective measurements. (1) In the low-resolution mode, the neuron's firing rate is observed at 5-bit resolution 10-ksps per channel. (2) In the high-resolution mode, 5-accurate-waveforms are measured at 10-bit resolution and 10-ksps per channel. (3) In the high-speed-sampling mode, an accurate waveform is analyzed with 10-bit resolution and 50-ksps per channel.

The TX/RX block transmits an output data of the ADC block and system information data to confirm the operating system condition. In addition, it receives external system control data, such as the probe control signal and ADC mode select signal.

In the next chapter, we describe the circuit design of the MUX/AMP block and the ADC block, although the TX/RX block is not discussed in this paper.

3. Circuit Design

We designed a neural sensing LSI with multi-input-channels in a 0.35- μm CMOS technology and evaluated the performance of signal processing by SPICE simulation.

3.1 MUX/AMP Block

An amplifier of the MUX/AMP block requires about 80-dB DC-gain, an in-band noise voltage and an offset voltage below 10- μV in order to amplify very low level ($\sim 100\mu\text{V}$) and low frequency ($\sim 10\text{kHz}$) neural signals. Since the output resistance of a probe inserted into a brain is as high as a few $\text{M}\Omega$, the input-impedance of the amplifier requires higher than the output resistance. However, usual CMOS-OPA is not applicable to amplification of 100- μV signals owing to a large flicker-noise of a CMOS transistor. To reduce the flicker noise, an amplifier using a chopper and/or auto-zeroing technique was developed.

We proposed the MUX/AMP block which consists of a cascade connection of a selector/multiplexer (SEL/MUX) with 10 input channels, a first chopper for modulation, a source follower buffer (SFB), fully differential amplifier (FDA), a second chopper for demodulation and a second-order low pass filter (LPF), which is implemented in on-chip resistors and capacitors. The block diagram is shown in Fig. 4. The block has to be designed with a small chip area and low-power consumption. For that purpose, we developed the multiplexer with 10-input-channels and shared the low noise chopper amplifier. The scheme reduced a number of interface buffer amplifier, and also realized a direct connection of the first chopper to the multiplexer.

The operation principle of the chopper amplifier is as follows. The first chopper-modulator modulates the input signal at the chopping frequency. The FDA amplifies the modulated signal, flicker noise and offset voltage. Then, the second chopper demodulates the modulated signal with the same chopping frequency. The flicker noise and offset voltage are only modulated by the second chopper modulator, thus the chopper amplifier separates the bandwidth of the

signal from these modulated noises at a chopping frequency. Finally, these noises are reduced by the LPF. In addition to these merits, the proposed chopper amplifier completely cancels the offset voltage of SFB and first FDA, because of a high-pass filter implemented by the feedback capacitor and resistor of FDA.

Generally, the chopper amplifier reduces the input impedance, due to the charge/discharge of chopper modulator stray capacitance operated at a rather high modulation frequency. Therefore, a pre-buffer-amplifier is required to maintain high input impedance. Since a noise generated at the buffer amplifier is not modulated, it is not reduced. To solve the problem, we propose a direct chopper input scheme as shown in Fig. 5. The circuit ground connects with the reference needle on the chip. We confirmed that the direct chopper input scheme could be applied to a practical neural system environment by the following experiments and consideration. An equivalent circuit of the neuron-needle interface is also shown in the same figure. A nucleus of neuron outputs about 100-mVpp voltage pulses [7]. A tungsten-needle detects the pulses through a cell membrane that has an equivalent impedance of parallel connection of 3-M Ω resistance and 3-pF capacitance. The detectable signal amplitude is reduced to 100- μV pp, because of an attenuation ratio of cell liquid resistance (3 k Ω) versus the membrane resistance (3 M Ω).

The probe also has Liquid/Needle interface impedance owing to the existence of a polarized charge. We measured the impedance with a 17- μm - ϕ -tungsten-needle in saline. The impedance is a series connection of a large capacitance of 1.7-nF due to the polarization and 10-k Ω needle resistance. A parasitic capacitance (17 pF) of the needle is charged with a neural signal of about 5-kHz, through the 1.7-nF Liquid/Needle interface impedance. A charge on the parasitic capacitance is transferred to the SFB input parasitic capacitance by the chopping frequency; the time constant of the chopper operation is faster than that of the MUX operation. A result of the simulation is shown in Fig. 6; the output voltage of the proposed circuit is only 4% smaller than the conventional chopper amplifier, because the para-

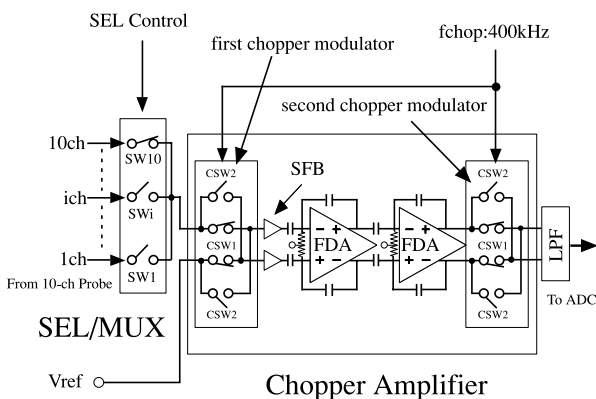


Fig. 4 Block diagram of a MUX/AMP.

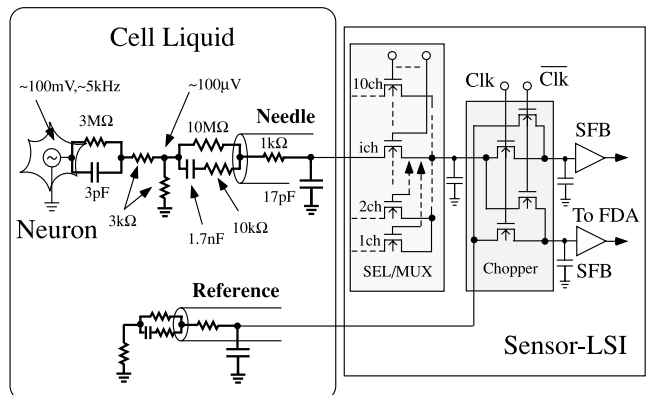


Fig. 5 Proposed direct chopper input scheme and neuron probing equivalent circuit.

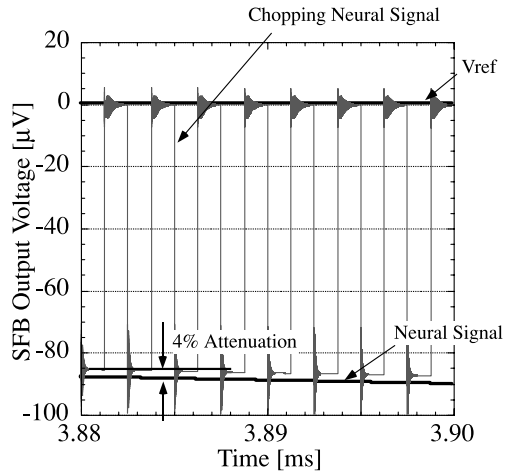


Fig. 6 An Input waveform of the chopper amplifier (simulation).

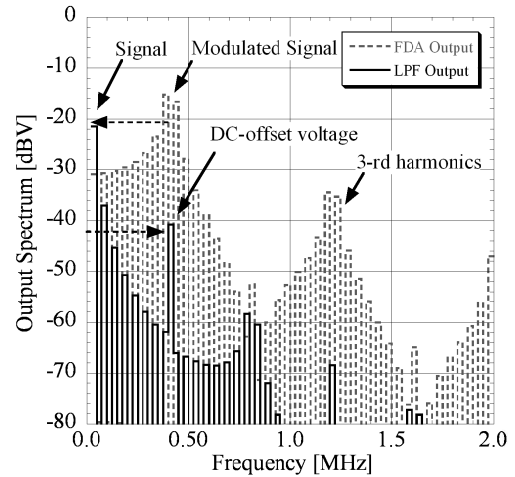


Fig. 8 Output spectrum of the chopper amplifier (simulation).

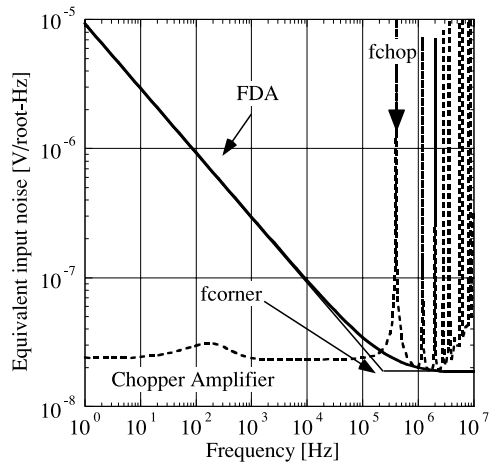


Fig. 7 Simulated noise spectral density.

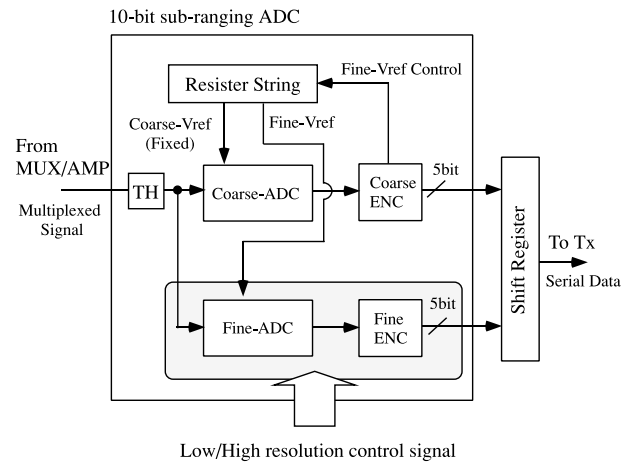


Fig. 9 Multi-mode sub-ranging ADC block diagram.

sitic capacitance of the probe is about 20-times larger than the MUX/chopper/SFB parasitic one. Therefore, the proposed circuit is able to detect the small neural signals; nevertheless the neuron drives the chopper modulator directly. Using the proposed scheme, the block enables implementation in only 2-FDAs despite 10-input-channels, and it accomplishes an 80% reduction in layout area and power consumption of amplifiers.

Simulation results of noise characteristics of the amplifier using device noise parameters are described. A noise spectral density of the FDA and chopper amplifier is shown in Fig. 7. The flicker noise moves the odd harmonics of chopper frequency at 400 kHz, and the chopper amplifier achieves the equivalent input noise of 23 nV/root-Hz. The total in-band noise (~100 kHz) of the chopper amplifier is 7.2 µV, which is smaller than the 32.9 µV of the FDA. Implemented FDA has a corner frequency, where the flicker noise equals the white noise, of 250-kHz, about 80-dB DC-gain and a 40-MHz unity-gain bandwidth.

Figure 8 shows the simulated output spectra of the chopper-amplifier with an 80-dB DC-gain and a DC-offset

voltage of 5 mV. The input signal has an amplitude of 10-µVpp and a pulse width of 40 µs. The LPF has a 75-kHz bandwidth. The output spectrum at 400-kHz shows the suppression of the DC offset voltage of FDA. The chopper amplifier compressed a 5-mV offset voltage to 1 µV.

3.2 ADC Block

The ADC requires accuracy of more than 8-bit and a maximum sampling rate of 500-kSPS for digitizing a multiplexed output 10-MUX/AMP. Furthermore, the ADC block requires efficient detection of various information, such as firing rates, timing and/or an accurate waveform of neurons. Therefore, we designed a 10-bit sub-ranging ADC, which enables the 3 operation modes. The ADC block is illustrated in Fig. 9. The block includes a 10-bit sub-ranging ADC [8], [9], track-and-hold circuit (TH) and a shift register. The sub-ranging ADC consists of a 1024-resister-string (R-string), two 5-bit-encoders and two 5-bit-flash-ADCs for coarse-and-fine conversions. Each flash ADC is implemented using 32 inverter chopper comparators (ICC). The R-string

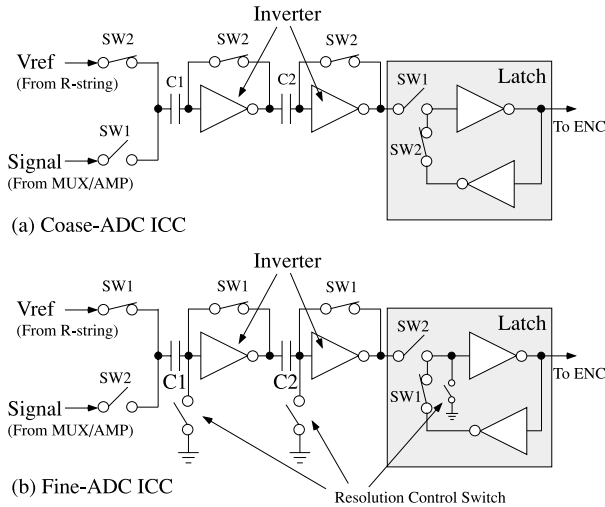


Fig. 10 Inverter chopper comparators (ICCs) diagram of (a) Coarse-ADC and (b) Fine-ADC.

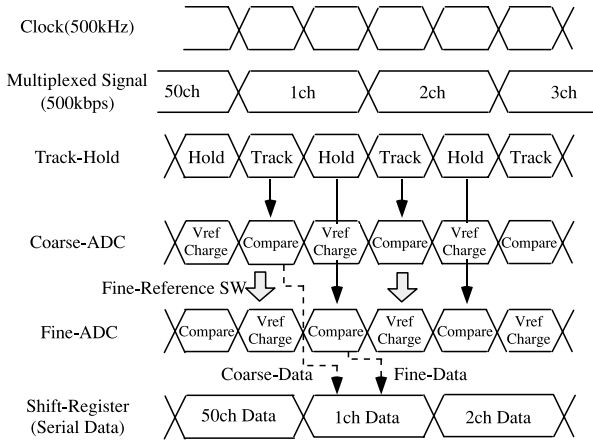


Fig. 11 Timing chart of the sub-ranging ADC block.

provides reference voltages to the comparators for coarse and fine conversions. In the low-resolution mode, only the coarse-ADC is operated.

The comparator circuits for coarse and fine ADCs are illustrated in Fig. 10. The same ICC is used for Coarse-ADC and Fine-ADC. The ICC is able to cancel an offset voltage of the inverters by charging it to the capacitors, C1 and C2. In the low-resolution mode, the resolution control switches added to the fine ADC ICC are turned on and reduce power dissipation of the fine-ADC to almost zero.

A timing chart of the proposed sub-ranging ADC is shown in Fig. 11. The coarse-ADC digitizes the tracked input signal to the 5-bit digital data, which switches the reference voltage of the fine-ADC. While the coarse-ADC compares the input voltage and the reference voltage, the fine-ADC samples the reference voltage determined by the coarse-ADC results. Then the fine-ADC digitizes the input signal held by TH to the 5-bit data. Finally, the sub-ranging ADC outputs a serial 10-bit data at the next phase. Using a pipeline operation, the ADC is accomplished with a con-

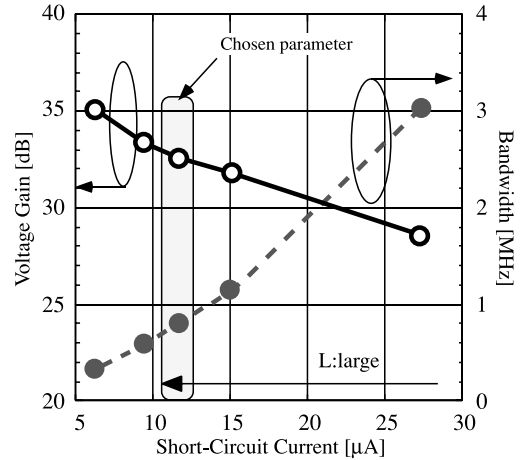


Fig. 12 Voltage gain and bandwidth versus short-circuit current of the ICC.

version of 500-kbps at a clock frequency of 500-kHz; the frequency is one-half of the conventional non-pipeline sub-ranging ADC. It is possible to reduce power dissipation of the TH and ICC because requirements of circuit specification, such as a settling time and a bandwidth, are relaxed.

The trade-off between short-circuit-current and gain/bandwidth of the ICC is shown in Fig. 12, where the sampling capacitance and the channel width of transistors is a constant. A short-circuit current of the ICC dominates the power consumption of the sub-ranging ADC. A reduction of the short-circuit current, which is accomplished by the large channel length of transistors, induces a voltage-gain increase and bandwidth degradation of the ICC owing to an increase of drain-source conductance g_{ds} and a reduction of gate transconductance g_m . The ICC requires a high-gain and a reasonable bandwidth larger than 60-dB and 500 kHz, respectively. Hence, we decided on a two-stage ICC and optimum transistor parameters that are shown in Fig. 12. We simulated the ADC with extracted parasitic components, but deviation of each component was not considered. The power dissipation at a 3-V 500-kbps operation is 3.3-mW in a high-resolution mode and 1.7-mW in a low-resolution mode.

4. Experimental Results

The proposed sensing system was designed and fabricated with a 0.35- μm double-poly triple-metal CMOS technology. The test chip includes an MUX/AMP block and an ADC block as shown in Fig. 13, and the chip area is 9.4- mm^2 ($=2.0 \times 4.7 \text{ mm}^2$).

The measured noise spectrum density of the chopper amplifier and FDA is shown in Fig. 14. The chopper frequency is 400 kHz, and the input terminals are connected to a ground of an evaluation board. The FDA has a corner frequency of 250-kHz and a total in-band noise of 17.0 μV ($\sim 100 \text{ kHz}$). On the other hand, the chopper amplifier has achieved the equivalent input noise of 10-nV/root-Hz and the total in-band noise of 3.2 μV . Figure 14 shows that the

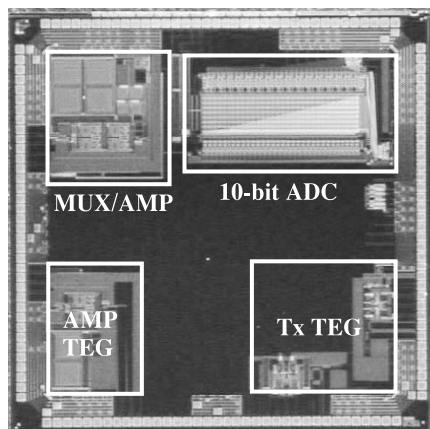


Fig. 13 A test chip of the proposed neural sensing system.

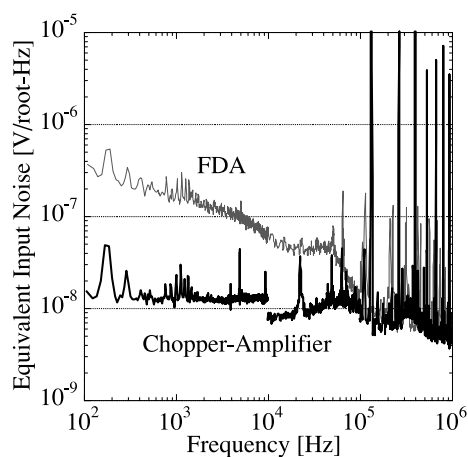


Fig. 14 Measured noise spectrum density.

chopper amplifier reduces low-frequency noise of FDA and the noise is modulated at a chopper frequency. The spectrum peaks appear around the chopper frequency due to distortion of the chopper waveform, therefore the post LPF attenuates the noise higher than 100 kHz.

The measured differential and integral non-linearities (DNL and INL) of the ADC are shown in Fig. 15. The ADC reference voltage is fixed at a supply voltage of 2 V. The maximum value of INL is 4 LSB, because an operational amplifier of the TH does not output lower than about 10 mV. The maximum DNL is 1 LSB, which is generated at a point where the range of the coarse-ADC comparators is changed. The degradation is due to a voltage drop of the ICC ground line. We confirmed that simulation of the offset voltage of ICC appears about 1-mV at both ends of the sub-ranging ADC.

Figure 16 demonstrates the measured signal-to-noise-and-distortion ratio (SNDR) versus frequency of the input signal, where the amplitude of input sinusoid is a 2-V_{pp} (full-range). The SNDR depends on the input frequency of the ADC; it was observed that the SNDR at a sampling frequency of 500-kHz is improved from 50 kHz. The SNDR requires more than 50-dB which corresponds to 8-bit accu-

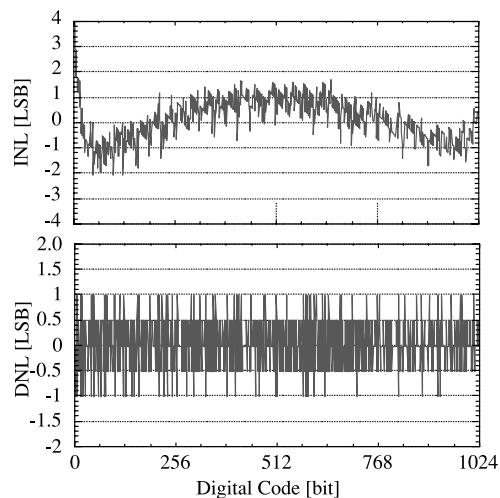


Fig. 15 Measured DNL and INL.

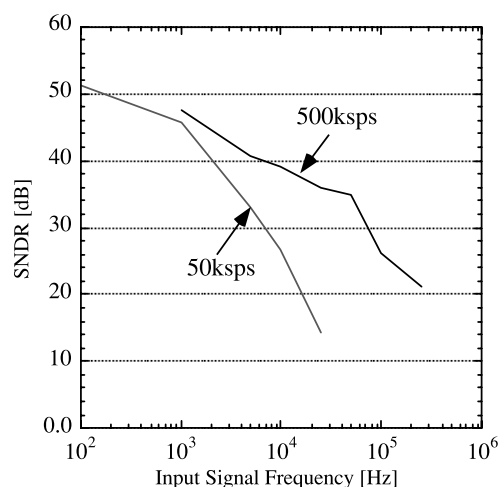


Fig. 16 Measured SNDR.

racy at a 5-kHz input signal. However, the measured SNDR is 42-dB, because the ADC has large DNL and INL, which are shown in Fig. 15. We confirmed that the degradation of SNDR is improved to 50-dB by reducing the voltage drop of the ICC power-line and by adapting terminal resistors of the R-string.

Figure 17 shows an output waveform of the MUX/AMP-block and ADC block, which converts the MUX/AMP output. The output waveform of ADC is transformed by a 12-bit Digital-to-Analog Converter. The MUX/AMP block multiplexes 5 input signals at a rate of 50-kch/s. In Fig. 17, the input signals include less than 1-mV sine wave at one-channel and no signal at the other four channels. The multiplexed signal is amplified by 80 dB. The ADC digitizes it to 10-bit digital data at 50 kps. Hence, we confirmed that very small signals with a few ten- μ V amplitude are processed by the proposed circuits.

The measured power dissipation of the MUX/AMP and ADC at a supply voltage of 3-V is 6.0-mW and 2.5-mW respectively.

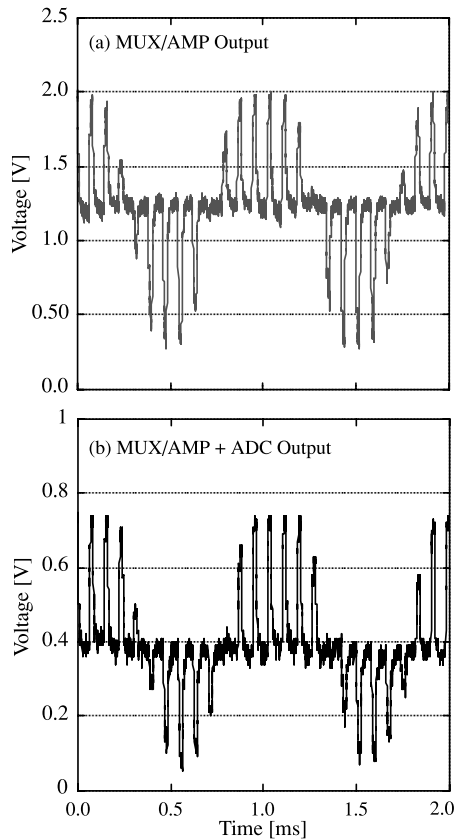


Fig. 17 Measured waveform of (a) the MUX/AMP output and (b) the ADC output reconstructed by 12-bit DAC.

5. Conclusion

We proposed the architecture of a neural signal sensing system and low-noise signal processing circuits for multi-input-channel neural signal measurement. The proposed one-chip system enables measurement of a multiplexed neural signal with low-noise and high accuracy. We measured the impedance of tungsten needles in saline and confirmed that the needle was directly connected to the chopper without large loss. Using the direct chopper input scheme, the proposed system reduced the size and the power consumption. As measurement results of the test chip, the proposed system accomplished a $3.2\text{-}\mu\text{V}$ in-band noise and a 500-kbps operation of 10-bit ADC at a supply voltage of 3 V.

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