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A 1 V Low-Noise CMOS Amplifier Using Autozeroing and Chopper Stabilization Technique

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SUMMARY A low-noise CMOS amplifier operating at a low supply voltage is developed using the two noise reduction techniques of autozeroing and chopper stabilization. The proposed amplifier utilizes a feedback with virtual grounded input-switches and a multiple-output switched op-amp. The low-noise amplifier fabricated in a 0.18-μm CMOS technology achieved 50-nV/$\sqrt{}$Hz input noise at 1-MHz chopping and 0.5-mW power consumption at 1-V supply voltage.

key words: *low-noise amplifier, autozeroing, chopper stabilization, low-voltage operation, switched op-amp, CMOS*

1. Introduction

Recently, sensor chips with CMOS mixed signal interface circuits have been used for sensing and monitoring biological functions [1], [2]. A low-noise amplifier for detecting very small signals with μV range is one of the most significant circuits in the sensor chip. However, decreasing the supply voltage and increasing the dc offset voltage and low-frequency (1/f) noise becomes a serious problem in future submicron CMOS technologies [3].

The autozeroing and chopper stabilization techniques are widely used for reducing these noises [4]–[7]. The principle of the autozeroing technique is illustrated in Fig. 1. The autozeroing technique is sampling the noise of the op-amp, such as the dc offset Voff and 1/f noise Vfn, at a null input; and then subtracting the effect of noise from the input signal using a sample-and-hold (S&H) circuit. Thus, the autozeroing technique can reduce the low-frequency noise of the amplifier. One disadvantage of autozeroing is an increase of the baseband noise floor, which is caused by the aliasing of the wideband noise that is inherent to the sampling process.

The principle of the chopper stabilization technique is shown in Fig. 2. Chopper stabilization, based on a modulation technique, converts the frequency range of an input signal to the higher frequency range of a chopping frequency fc where the dominant noise is a white noise, and then demodulates it back to the baseband after amplification. To remove the noise demodulated within higher frequency range than the chopper frequency and to obtain a low spurious signal, the high order low pass filter (LPF) is required.

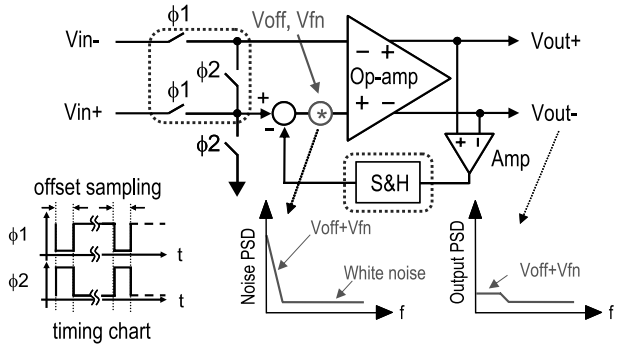

Fig. 1 Principle of autozeroing technique.

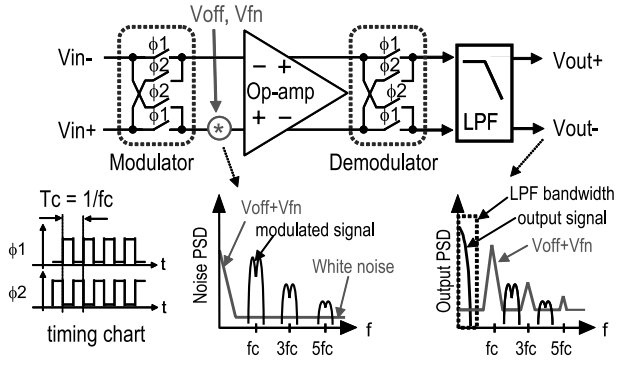

Fig. 2 Principle of chopper stabilization technique.

Using both autozeroing and chopper stabilization techniques together contributes to a reduction of both the baseband noise floor and the modulated noise at the chopper frequency [4], [5] because the autozeroing removes the dc-offset, and the chopper stabilization decreases the baseband noise. The low-noise amplifier operating at a low supply voltage requires both techniques; however they are hardly implemented with normal analog switches.

The reason is that the analog switches cannot transmit an intermediate voltage level at a low supply voltage. To solve the analog switch issue, a clock signal boosting technique was developed [8]. However the technique can no longer be used in several-ten-nm CMOS technologies due to voltage scaling. Other solutions are switched-capacitor techniques based on the switched op-amp [9]–[11] that can provide the switch function without analog switches; the autozeroing operation is performed by the switched op-amp

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[11] in order to compensate a gain error in a switched-capacitor integrator caused by offset voltage of the op-amp. This paper proposes a low-noise amplifier based on a switched op-amp employing techniques of both autozeroing and chopper stabilization for reducing the 1/f noise and the dc-offset voltage of the amplifier.

2. System Architecture

A conceptual diagram of the proposed low-noise amplifier, based on a switched-capacitor amplifier, employing the techniques of autozeroing and chopper stabilization is shown in Fig. 3(a). In the low-voltage operation of chopper stabilization, a conventional chopper modulator and demodulator could not be implemented by floating analog switches due to an indeterminable voltage level of input and output. In order to overcome the above problem, the switched-capacitor amplifier was implemented by a multi-output switched op-amp.

The chopper modulators (CHP1, CHP2) with the virtual grounds are implemented by simple CMOS analog switches as shown in Fig. 3(b), because a voltage level of virtual ground is possible to set to any level and the input signal amplitude is small. The proposed architecture requires inserting the extra modulator (CHP2) into the feedback loop to modulate the output signal previously demodulated by the CHP3, however the incremental area of the CHP2 is almost negligible. On the other hand, the CHP3 demodulator placed outside the virtual ground cannot be formed with analog switches because of a large output amplitude. The CHP3 is therefore implemented by a switched op-amp. The CHP1, CHP2 and CHP3 are switched by the complementary clock signals of $\phi 1$ and $\phi 2$.

The multi-output switched op-amp is also able to configure the autozeroing scheme. During the $\phi 0$ phase, the output of the switched op-amp are connected to their input using dotted lines as shown in Fig. 3(b), forming a voltage follower. The paths are activated on the initial $\phi 0$ phase and the detected dc offset voltage is stored into a hold capacitor C2; accordingly, the autozeroing operation cancels the dc offset. If the offset sampling is periodically carried out, low-frequency noise can also be reduced.

The output common-mode stabilization of the multi-output switched op-amp was achieved by a common mode feedback (CMFB) circuit. The CMFB circuit fixes the virtual ground common mode level and the output common mode level of the CHP3 during autozeroing and chopper stabilization, respectively.

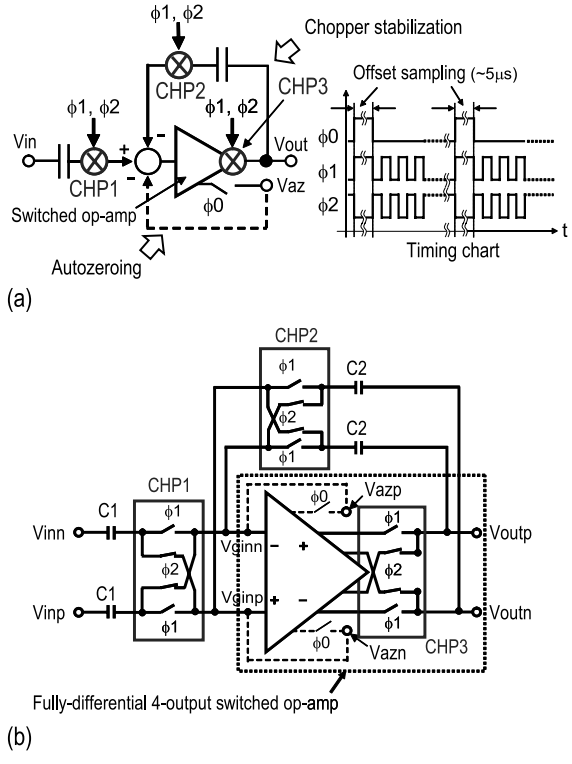

Fig. 3 (a) Conceptual block diagram of the low-noise amplifier based on the techniques of autozeroing and chopper stabilization, and (b) the circuit schematic implemented by the fully-differential switched op-amp.

3. Circuit Design

3.1 Switched Op-amp

The circuit schematic of the fully-differential four-output switched op-amp without a CMFB circuit is shown in Fig. 4. The switched op-amp equips with the CHP3 demodulator and autozeroing output nodes. The autozeroing output nodes are Vazp and Vazn. They are used to sample their own dc offset voltage, during the $\phi 0$ phase. The CHP3 implemented by four output-buffers has two output nodes of Voutp and Voutn. Their outputs are switched using the clock signals $\phi 1$ and $\phi 2$, thus achieving demodulation.

The switched op-amp consists of 3 stages. The input stage is implemented with a PMOS source-coupled pair. The second stage consists of two parallel common-source gain stages and they drive separately PMOS and NMOS in the final buffer stage. The separation makes it possible to independently set the bias points for PMOS and NMOS. The final stage consists of push-pull output buffers with grounded switches. Each bias-voltage for the push-pull buffers, Vbp1 and Vbn1, is supplied from an on-chip bias circuit implemented by a replica circuit of the buffer, so that the output buffer operates in class AB. It results in low power consumption and low distortion, even though at a low supply voltage.

The two parallel second stage paths also contribute to phase compensation [12]. As shown in Fig. 4, both gain stages have RC series feedback paths for phase compensation. The parallel paths yield multiple left half plane zeros in the open loop transfer function. The additional zeros facilitate the phase compensation for the three-stage amplifier. Simulation results have shown a 90-dB dc gain, a 53-degree phase margin and a 50-MHz unity-gain bandwidth.

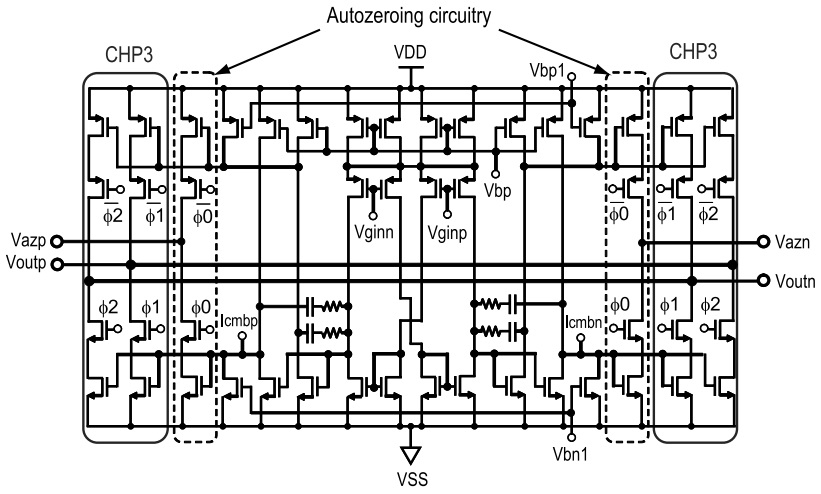

Fig. 4 Schematic of the fully-differential 4-output switched op-amp.

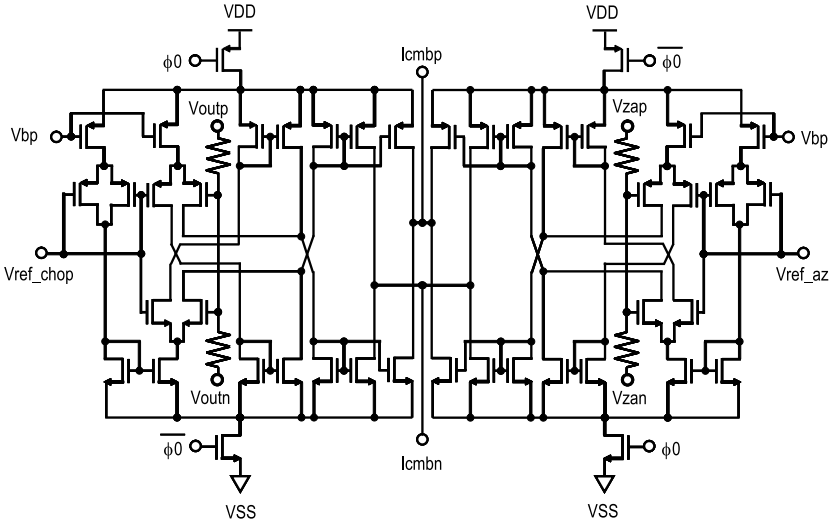

Fig. 5 Common mode feedback circuit.

3.2 Common Mode Feedback Circuit

The circuit diagram of the CMFB circuit is given in Fig. 5. The output common mode level of the switched op-amp is detected using a resistive divider, and compared with the reference voltage. It is then returned to the feedback nodes of the Icmbp and Icmbn. During the autozeroing operation ($\phi 0$ is high), the common mode level of virtual ground, which is the average of Vazp and Vazn, is set to the reference voltage of Vref_az by the right side circuit of the CMFB circuit. The left side circuit of the CMFB circuit is held the output common mode level of Voutp and Voutn to the reference voltage of Vref_chop, while the chopper stabilization operation ($\phi 0$ is low).

4. Experimental Results

A test chip of the low-noise amplifier, based on the chopper stabilization and autozeroing techniques, is fabricated in a 0.18-μm CMOS process, with nominal NMOS and PMOS threshold voltages of about 0.42-V and 0.5-V, respectively. The micrograph of the test chip is shown in Fig. 6. The chip

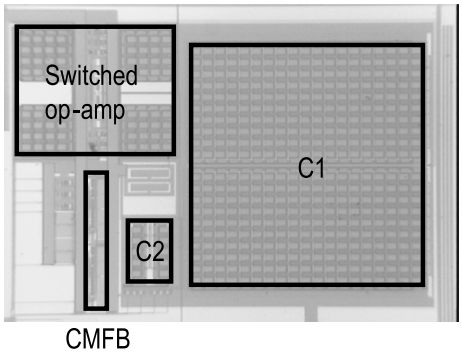

Fig. 6 Proposed direct chopper input scheme and neuron probing equivalent circuit.

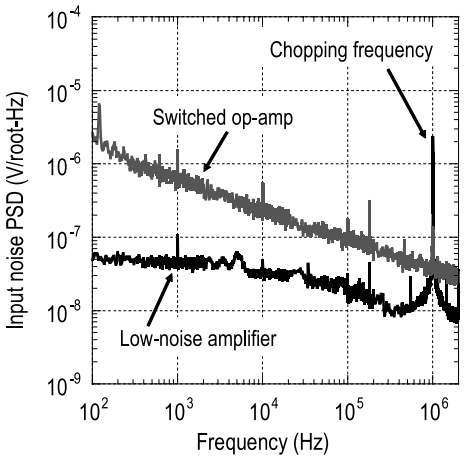

Fig. 7 Measured input noise PSD versus frequency of the switched op-amp and the low-noise amplifier with autozeroing and chopping operation.

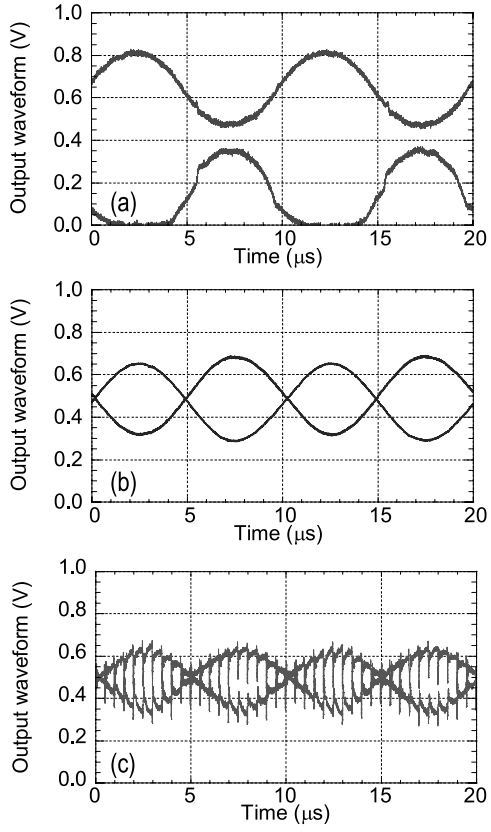

Fig. 8 Measured output waveforms of the low-noise amplifier: (a) without autozeroing and chopper stabilization, (b) with autozeroing and (c) with autozeroing and chopper stabilization.

area is $1100 \times 800\,\mu m^2$. In order to reduce an operation frequency of the autozeroing, the large feedback capacitors C1 and C2 are designed with 80-pF and 2-pF, respectively.

The input noise PSDs of the switched op-amp and the low-noise amplifier are shown in Fig. 7. The low-noise amplifier was operated with a 1-MHz chopping frequency, a 0.01-Hz autozeroing frequency and a 5-μs autozeroing time,

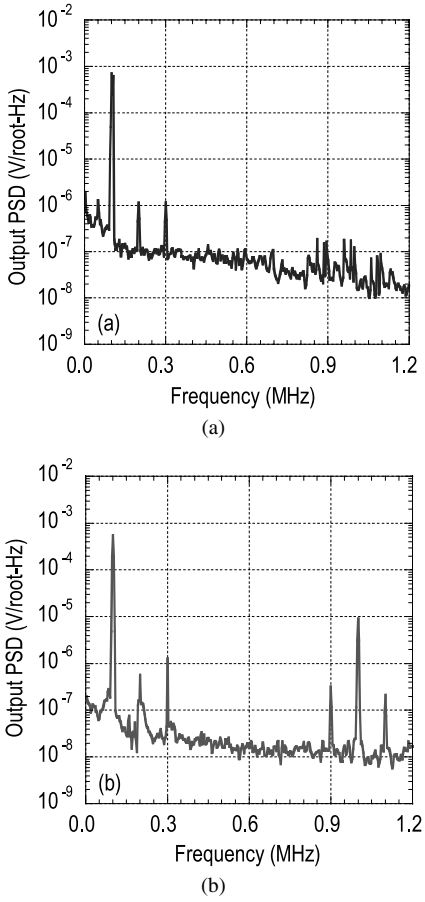

Fig. 9 Measured output spectra of the low-noise amplifier: (a) with autozeroing and (b) with autozeroing and chopper stabilization.

at a supply voltage of 1 V. The input noise of switched op-amp shows a typical 1/f noise spectrum, and the noise PSD is 2.5-μV/$\sqrt{\text{Hz}}$ at 100 Hz. The proposed low-noise amplifier suppressed the noise PSD to less than 50 nV/$\sqrt{\text{Hz}}$.

Figure 8(a) shows output waveform of the low-noise amplifier without autozeroing and chopper stabilization at a 100-kHz 10-mVpp input; the waveform is distorted by the input offset voltage of the switched op-amp. That of the low-noise amplifier with a 0.01-Hz autozeroing frequency at the same input is shown in Fig. 8(b). The input offset voltage of the switched op-amp is reduced by the autozeroing. The autozeroed amplifier continued to output the waveform more than 1 hour at room temperature, because the offset voltage is stored on the large capacitors C1 and C2. The offset voltage would drift when the low-noise amplifier is operated at a high temperature and/or because of small feedback capacitors designed to reduce a chip's area. Thus, in such cases, it requires a higher autozeroing frequency. Figure 8(c) shows the output waveform of the low-noise amplifier with the autozeroing and 1-MHz chopping operation at the same input, the remained input offset voltage and 1/f noise are removed by chopping. The input offset voltage caused by the difference between output offset voltages of buffer stage is 290-μV. It can be compressed, therefore, by increasing the

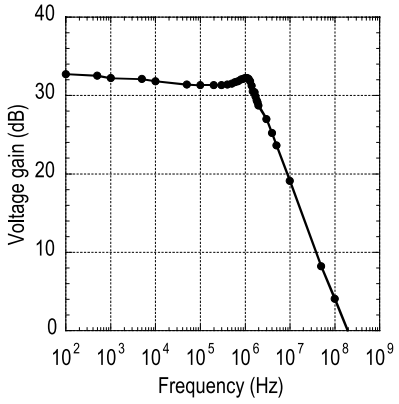

Fig. 10 Measured frequency response of voltage gain.

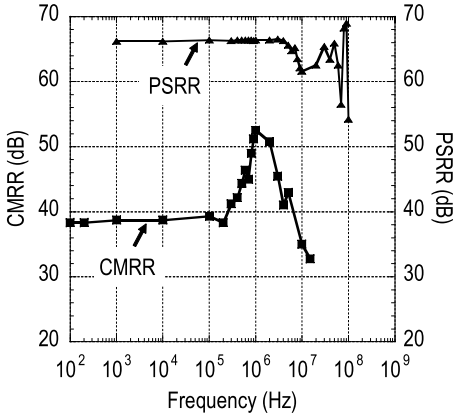

Fig. 11 Measured frequency response of CMRR and PSRR.

low-noise amplifier gain. The charge injection noise appears in the output waveform, as shown in Fig. 8(c); however the chopper amplifier is possible to reduce the noise by applying a ping-pong configuration [5] or a chopper modulation with guard time [6].

Figures 9(a) and (b) illustrate the output PSD of the low-noise amplifier operated with autozeroing and chopper stabilization at a 100-kHz 10-mVpp input. The autozeroing improves the THD of the low-noise amplifier, as shown in Fig. 9(a); and the chopping achieves a high dynamic range due to 1/f noise reduction. The THD of low-noise amplifier, with the autozeroing and chopping operations, is 52 dB (Fig. 9(b)). The output signal and the total integrated noise up to 100-kHz were 500-mVpp and 15-μV respectively. The prototype low-noise amplifier thus achieved a dynamic range of 88-dB on this condition.

The measured frequency response of voltage gain is shown in Fig. 10. The amplifier achieved a 32-dB voltage gain and a 2-MHz cut-off frequency at 1-MHz chopping operation. The unity gain frequency was more than 100 MHz. Figure 11 is plotted with the measured frequency response of both CMRR and PSRR. The CMRR and PSRR were 38-dB up to 200 kHz and 66-dB up to 500 kHz, respectively.

The performance comparison of the referred amplifiers and the proposed amplifier is summarized in Table 1. In this

Table 1 Comparison of the reference op-amps and this work.

	This work	Ref. [5]	Ref. [13]
Supply voltage (V)	1.0	5.0	1.0
Autozeroing freq. (kHz)	<0.001	7.5	-
Chopping freq. (kHz)	1000	15	-
Input offset voltage (μV)	290	3	3000
Input noise PSD (nV/$\sqrt{\text{Hz}}$)	50	20	360
Power consumption (mW)	0.5	4.0	0.2
Chip area (mm^2)	0.88	0.67	0.81
FOM $\times 10^3$	45	18.7	17.1

experiment, the proposed amplifier, which was compensated for the offset voltage by the autozeroing, continued to operate more than 1 hour. Thus we described that the autozeroing frequency is less than 1 Hz. The referred amplifiers focused on a noise reduction or a low voltage operation. We defined the figure of merit (FOM) focused on noise, power and area; the equation is as follows:

$$FOM = 1/N \times S \times P, \tag{1}$$

where N is the noise density, P is the power dissipation and S is the chip area. The FOM of proposed amplifier achieved a result 2.4-times larger than the referred amplifiers [5], [13].

5. Conclusion

A 1-V supply low-noise amplifier based on autozeroing and chopper stabilization techniques is presented. The key techniques of noise reduction at a low supply voltage are the multi-output switched op-amp using grounded switches, and the chopper modulator operating at the virtual ground level. The amplifier fabricated with a normal Vth 0.18-μm CMOS process has achieved 50-nV/$\sqrt{\text{Hz}}$ noise PSD, 52-dB THD, 88-dB dynamic range at 1-V supply voltage.

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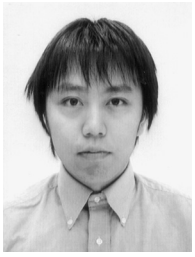

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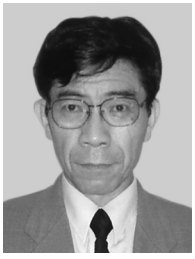

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