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Completely Surface-Potential-Based Compact Model of the Fully Depleted SOI-MOSFET Including Short-Channel Effects

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***Abstract*—The reported circuit simulation model Hiroshima University semiconductor technology academic research center IGFET model silicon-on-insulator (HiSIM-SOI) for the fully depleted SOI-MOSFET is based on a complete surface-potential description. Not only the surface potential in the MOSFET channel, but also the potentials at both surfaces of the buried oxide are solved iteratively, which allows including of all relevant device features of the SOI-MOSFET explicitly and in a physically correct way. In particular, an additional parasitic electric field, induced by the surface-potential distribution at the buried oxide, has to be included for accurate modeling of the short-channel effects. The total iteration time for surface potential calculation with HiSIM-SOI is under most bias conditions only a factor 2.0 (up to a factor 3.0 for some bias conditions) longer than for the bulk-MOSFET HiSIM model, where just the channel surface potential is involved. It is verified that HiSIM-SOI reproduces measured current–voltage (I–V) and $1/f$ noise characteristics of a 250-nm fully depleted SOI technology in the complete operating range with an average error of 1% and 15%, respectively. Stable convergence of HiSIM-SOI in the circuit simulation is confirmed.**

***Index Terms*—Inverter, iteration solution, short-channel effect (SCE), surface potentials, $1/f$ noise.**

I. Introduction

THE silicon-on-insulator (SOI)-MOSFET is one of the candidates for the next generation of mainstream integrated circuit technologies, because it reduces junction capacitances and improves subthreshold swing, thus realizing a high-speed device operation [1]. Circuit-simulation models for the SOI-MOSFET have been developed to enable a reliable circuit design for utilization of these advantages. Two major existing models, Berkeley short-channel IGFET model-SOI (BSIM-SOI) [2] and University of Florida SOI (UFSOI) [3]–[5], have been applied for the practical circuit simulation. Both models include important features specific for the SOI-MOSFET, such as the parasitic bipolar effect and the generation-recombination current. Smooth transition between the partially depleted and the fully depletion condition during circuit operation is also considered. However, both models suffer from nonconvergence problems in the circuit simulation. Both models have been developed as an extension of the bulk-MOSFET, and thus the main reason for these convergence problems may be attributed to a violation of the charge conservation [6], [7]. Here, we report a compact model for the fully depleted SOI-MOSFET, which considers relevant device features explicitly and also preserves charge conservation. For this purpose, the model is developed based on a complete surface-potential description for all relevant oxide surfaces in a similar manner as Hiroshima University semiconductor technology academic research center (STARC) IGFET model (HiSIM) for the case of the bulk-MOSFET [8]–[10].

The reported SOI-MOSFET model is the first based on a completely surface-potential-based description solving the Poisson equation explicitly. The potential distribution is solved not only in the SOI layer but also in the complete SOI structure down to the substrate contact, and is named HiSIM STARC IGFET model-SOI (HiSIM-SOI). The number of iteration steps for solving the Poisson equation, required to calculate surface potentials, is in average a factor 2 larger than for the bulk-MOSFET case, solving only one surface potential at the interface of gate oxide and substrate. Since the simulation time with HiSIM for the bulk-MOSFET is comparable to BSIM3 [11], the simulation speed achievable with HiSIM-SOI is realistic for the practical circuit simulation.

Among specific features of the SOI-MOSFET, the self-heating effect and the history effect are known to be important issues [2], [4]. The self-heating effect is solved with a subcircuit including a thermal resistance and capacitance up to now. The history effect is caused by the impact ionization, for which the compact-model formulation is presently under development and which is therefore not included in the present report.

II. Theoretical Model Formulation

Fig. 1(a) and (b) shows a schematic of the SOI-MOSFET and its energy-band diagram along the direction vertical to the channel, respectively. Three surface potentials are distinguished: $\phi_{s,SOI}$ is the surface potential at the front oxide (FOX), $\phi_{b,SOI}$ is the surface potential at the backside of the SOI layer, and $\phi_{s,bulk}$ is the surface potential of the bulk substrate. Under the normal operating condition, the drain–current flows in the inversion layer of the MOSFET channel with the surface potential $\phi_{s,SOI}$. A basic equation of the SOI-MOSFET,

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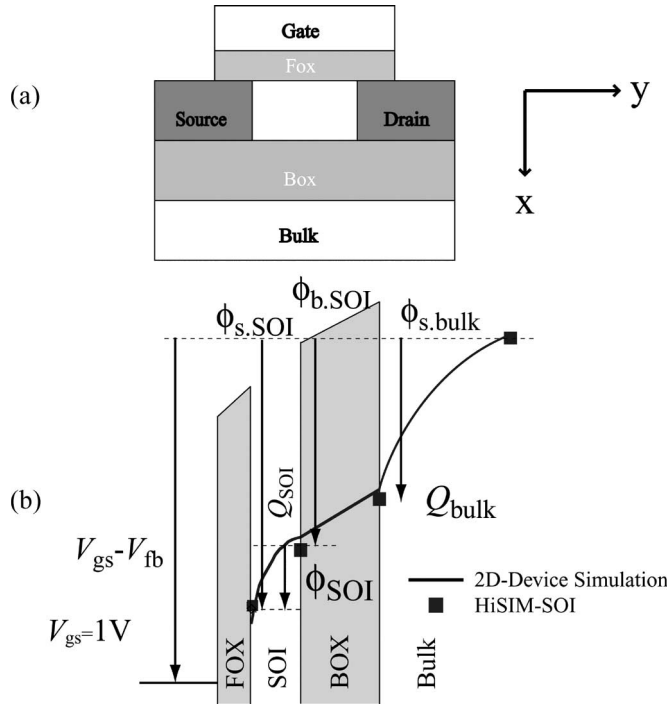

Fig. 1. (a) Schematic of the SOI-MOSFET and its (b) band diagram along the vertical direction to the channel, where the used terminology for the potentials is also depicted. The solid line shows a 2-D device simulation result and the symbols are the calculation results with the HiSIM-SOI model. The gate voltage of 1 V is applied for the gate length of 10 μm.

describing its features for the applied gate voltage ($V_{\rm gs}$), is derived as [6], [7]

$$V_{\rm gs}-V_{\rm fb}-\Delta V_{\rm th}=\phi_{\rm s,bulk}-\frac{Q_{\rm bulk}}{C_{\rm BOX}} + \phi_{\rm SOI}-\frac{Q_{\rm bulk}+Q_{\rm SOI}}{C_{\rm FOX}} \quad (1)$$

$$\phi_{\rm SOI}=\phi_{\rm s,SOI}-\phi_{\rm b,SOI} \quad (2)$$

from the Poisson equation together with the Gauss law. $V_{\rm fb}$ and $\Delta V_{\rm th}$ are the flat band voltage and the threshold voltage shift from the long-channel transistor $V_{\rm th}$, respectively. $C_{\rm BOX}$ and $C_{\rm FOX}$, are the buried oxide (BOX) capacitance and the gate-oxide capacitance, respectively. $Q_{\rm bulk}$ and $Q_{\rm SOI}$ are the induced charges in the bulk and in the SOI layer, respectively. To calculate $Q_{\rm bulk}$ and $Q_{\rm SOI}$, the three surfaces potential values ($\phi_{\rm s,SOI}$, $\phi_{\rm b,SOI}$, and $\phi_{\rm s,bulk}$) depicted in Fig. 1(b) have to be known.

To develop an analytical surface-potential-based SOI-MOSFET model four tasks have to be achieved.

1) Accurate calculation of the three different surface potentials.
2) Consistent calculation of the charges without violating charge conservation.
3) Modeling of the short-channel effects (SCEs).
4) Extraction of three additional basic device parameter values, namely the thickness of the SOI layer ($t_{\rm SOI}$), the thickness of the BOX layer ($t_{\rm BOX}$), and the impurity concentration of the bulk ($N_{\rm sub,bulk}$).

Completion of all four tasks is inevitable for realizing a compact SOI-MOSFET model for circuit applications. Initial results for task 1) and 4) have been reported previously [7], so that the main focus here is on tasks 2) and 3).

A. Calculation of Charges and Surface Potentials

Descriptions for $Q_{\rm bulk}$ and $Q_{\rm SOI}$ in (1) are rather complicated due to the three independent surface potentials, which vary differently for different bias conditions. To derive a closed form of the Poisson equation and for minimizing the calculation cost, simplifications have been introduced [6], [7]. One of the reasonable simplifications is that the inversion condition never occurs at the SOI-layer surface of the BOX layer under normal operating conditions, thus

$$Q_{\rm bulk}=\sqrt{\frac{2q\varepsilon_{\rm Si}N_{\rm sub,bulk}}{\beta}\left(e^{-\beta\phi_{\rm s,bulk}}+\beta\phi_{\rm s,bulk}-1\right)} \quad (3)$$

is reduced to

$$Q_{\rm bulk}=-\sqrt{\frac{2qN_{\rm sub,bulk}\varepsilon_{\rm Si}}{\beta}}\sqrt{\beta\phi_{\rm s,bulk}-1} \quad (4)$$

with

$$\beta=\frac{q}{k\cdot T} \quad (5)$$

where q and $\varepsilon_{\rm Si}$ are the electron charge and the permittivity of the silicon substrate, respectively, and T and $N_{\rm sub,bulk}$ are the temperature and the impurity concentration in the bulk, respectively. Another appropriate simplification is that the depletion charge in the SOI layer ($Q_{\rm dep,SOI}$) is approximated to be $t_{\rm SOI}$ times $N_{\rm sub,SOI}$ for the fully depleted SOI-MOSFET

$$Q_{\rm dep,SOI}=-qN_{\rm sub,SOI}t_{\rm SOI} \quad (6)$$

where $N_{\rm sub,SOI}$ is the impurity concentration in the SOI layer. The total depletion charge in the SOI-MOSFET is the sum of these two charges

$$Q_{\rm dep}=Q_{\rm dep,SOI}+Q_{\rm bulk}. \quad (7)$$

The inversion charge at the SOI surface $Q_{\rm n,SOI}$ is derived in the same way as for the bulk-MOSFET with the charge-sheet approximation [8]–[10], where the total depletion charge is considered in (8), shown at the bottom of the next page,which is derived by integrating the Poisson equation vertical to the surface direction. ϕ_f is the quasi-Fermi potential varying from source ($\phi_f=0$) to drain ($\phi_f=V_{\rm ds}$). The total charge in the SOI layer is written

$$Q_{\rm SOI}=Q_{\rm n,SOI}+Q_{\rm dep,SOI}. \quad (9)$$

The above described charge equations are substituted into (1) and surface potentials are calculated, iteratively. By applying the charge-sheet approximation, all device characteristics are described as a function of the surface potentials at the source

side and the drain side. Boundary conditions are given by applying the Gauss low

$$\varepsilon_{\rm Si} E_S = \varepsilon_{\rm ox} E_{\rm ox} \tag{10}$$

which derives a relationship

$$\phi_{\rm s,bulk} = \frac{Q_{\rm bulk}}{C_{\rm BOX}} = \phi_{\rm b,SOI} \tag{11}$$

where

$$C_{\rm BOX} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm BOX}}. \tag{12}$$

Presently, the iteration procedure requires normally two times and for some bias conditions up to three times more iteration steps than the bulk MOSFET model HiSIM [10]. Fig. 2 shows the iteration-step number of HiSIM-SOI as a function of $V_{\rm gs}$ for fixed $V_{\rm ds} = 1.5$ V.

As can be seen from Fig. 1(b), the SOI-MOSFET induces charges in different locations, which makes it difficult to preserve the charge conservation in the compact modeling. Therefore, calculation of all these charges based on the surface potentials, derived only from (1), is a key to enable maintainability of the charge conservation. Calculated surface potentials are compared in Fig. 1(b) with two-dimensional (2-D) device simulation results. Fig. 3 shows the compact-model calculated $\phi_{\rm s,SOI}$ as a function of $V_{\rm gs}$, which compares well with 2-D device simulation results.

The charges on the terminals required for the circuit simulation are determined from the surface potentials by integrating along the channel from the source (0) to the drain side ($L_{\rm eff}$)

$$Q_G = -(Q_B + Q_I) \tag{13}$$

$$Q_B = W_{\rm eff} \int_0^{L_{\rm eff}} Q_{\rm dep} dy = -W_{\rm eff} q N_{\rm sub,SOI} t_{\rm SOI} \tag{14}$$

$$Q_I = W_{\rm eff} \int_0^{L_{\rm eff}} Q_{\rm n,SOI} dy \tag{15}$$

$$Q_D = W_{\rm eff} \int_0^{L_{\rm eff}} \frac{y}{L_{\rm eff}} Q_{\rm n,SOI} dy \tag{16}$$

$$Q_S = Q_I - Q_D. \tag{17}$$

Here, Q_G, Q_B, Q_I, Q_D, and Q_S are gate charge, bulk charge, inversion charge, drain charge, and source charge, respectively, and $L_{\rm eff}$ is the channel length

$$L_{\rm eff} = L_{\rm gate} - 2 \cdot {\rm XLD} \tag{18}$$

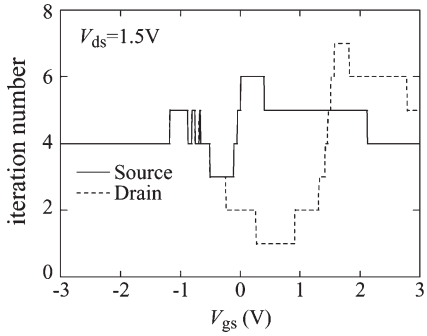

Fig. 2. Number of iteration steps of HiSIM-SOI to calculate surface potentials as a function of $V_{\rm gs}$.

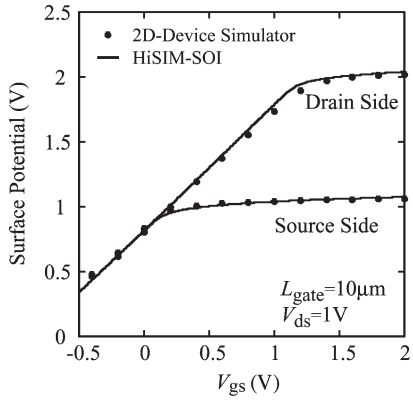

Fig. 3. Calculated surface potentials with the compact HiSIM-SOI-MOSFET model in comparison to 2-D device simulation results.

where $L_{\rm gate}$ length and XLD is the under diffusion length beneath the gate oxide. Fig. 4 compares calculated inversion charge Q_I with 2-D device simulation results for silicon layer thicknesses $t_{\rm SOI}$ of 1) 50 and 2) 25 nm. Good agreement with the 2-D device simulation results down to $t_{\rm SOI}$ of 25 nm proves reliability of the developed model. The deviation of the model result from the 2-D device simulation result is 2% under the strong inversion condition. Analytical equations for capacitances are obtained by the derivatives of the charges with respect to node potentials. Fig. 5 shows the calculated gate capacitance $C_{\rm gg}$ in comparison to 2-D device simulation results. A 2-D device simulation result of the bulk MOSFET is depicted together. The reduction of $C_{\rm gg}$ for the SOI-MOSFET is due to the contribution of the additional capacitance of $C_{\rm BOX}$.

B. Modeling of SCEs

The SCEs are of serious concern for scaled devices, and to model these effects accurately is indispensable for the reliable circuit simulation. The main SCE is conventionally observed as a threshold voltage shift ($\Delta V_{\rm th}$), which is included in the bulk-MOSFET model HiSIM by considering the contribution of the

$$Q_{\rm n,SOI}(\phi_{\rm s,SOI}) = -\sqrt{\frac{2q\varepsilon_{\rm Si}N_{\rm sub}}{\beta}\left[e^{-\beta\phi_{\rm s,SOI}} + \beta\phi_{\rm s,SOI} - 1 + \frac{n_i^2}{N_{\rm sub}^2}\left(e^{\beta(\phi_{\rm s,SOI}-\phi_f)} - e^{-\beta\phi_f}\right)\right]} - Q_{\rm dep} \tag{8}$$

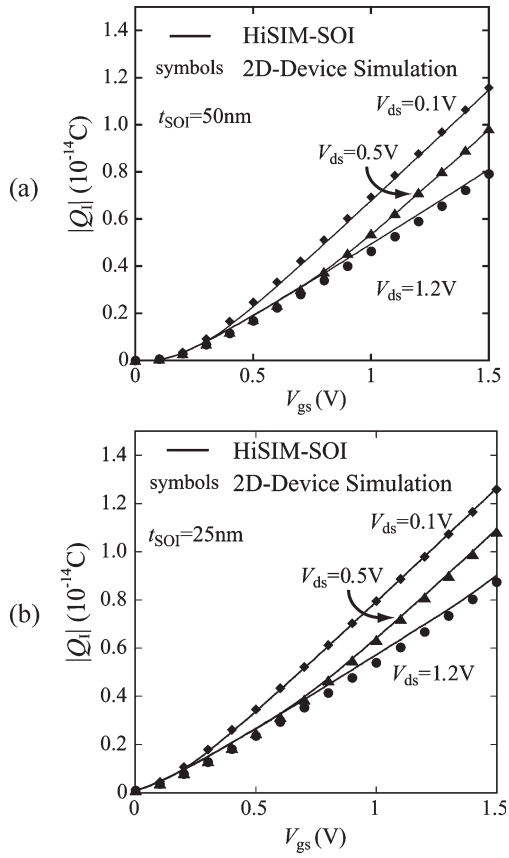

Fig. 4. Calculated inversion charge as a function of the gate voltage $V_{\rm gs}$ for various drain voltages $V_{\rm ds}$, (a) for $t_{\rm SOI} = 50$ nm and (b) for $t_{\rm SOI} = 25$ nm. 2-D device simulation results are depicted for comparison. The deviation between the model results and those of the 2-D device simulation is about 2% under the strong inversion condition.

lateral electric field [12], [13]. As shown in Fig. 6, a rectangle ABCD is considered for the SOI-MOSFET in the depletion region. With the Gauss law, integration of the field along the surface of the rectangle ABCD is equal to the charge inside, as represented by (19)

$$-\int_A^B E_{y1}dx - \int_B^C E_{\rm b,SOI}dy + \int_C^D E_{y2}dx + \int_D^A E_{\rm s,SOI}dy = \int \frac{Q_{\rm SOI}}{\varepsilon_{\rm si}}dy \quad (19)$$

where x and y are the directions vertical and parallel to the channel, respectively. Equation (19) is simplified by the approximation that the lateral electric field is uniform in the vertical direction, i.e., independent of x

$$(-E_{y1} + E_{y2})t_{\rm SOI} + (E_{\rm s,SOI} - E_{\rm b,SOI})dy = -\frac{Q_{\rm dep,SOI}}{\varepsilon_{\rm si}}dy. \quad (20)$$

By applying the Gauss law, we derive the relationship between $V_{\rm gs}$ and the induced charge in the rectangle

$$E_{\rm s,SOI} = \frac{C_{\rm FOX}}{\varepsilon_{\rm si}}\left(V_{\rm gs} - V_{\rm fb} - \phi_{\rm s,SOI} - \frac{\varepsilon_{\rm si}}{C_{\rm FOX}}\frac{E_{y2} - E_{y1}}{dy}t_{\rm SOI}\right) + E_{\rm b,SOI}. \quad (21)$$

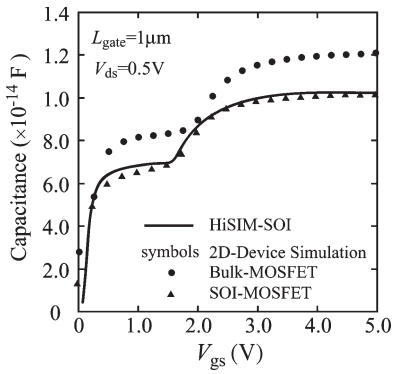

Fig. 5. Calculated gate capacitance with HiSIM-SOI as compared with 2-D device simulation results.

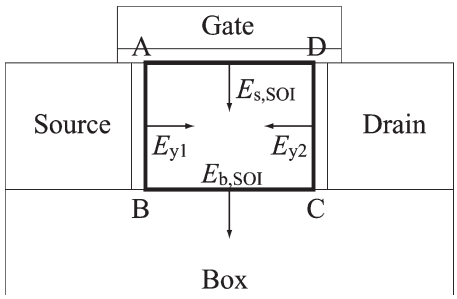

Fig. 6. Electric fields in the SOI depletion region under consideration to model SCEs.

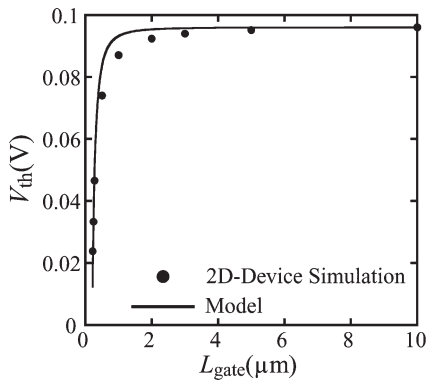

Fig. 7. Calculated threshold voltage only with the conventional SCE modeling approach in comparison to a 2-D device simulation result.

With reduced gate length, the second term of the right-hand side of (21) is no longer negligible and causes the threshold voltage shift

$$\Delta V_{\rm th} = \frac{\varepsilon_{\rm si}}{C_{\rm FOX}}t_{\rm SOI}\frac{dE_y}{dy}. \quad (22)$$

Fig. 7 compares the threshold voltage $V_{\rm th}$ obtained by the developed compact model of (19)–(22) with a 2-D device simulation as a function of $L_{\rm gate}$. A clear difference is that the $V_{\rm th}$ reduction starts from longer $L_{\rm gate}$ in the 2-D numerical simulation than with the compact model. This enhanced SCE in the SOI-MOSFET cannot be reproduced by the conventional approach to SCE modeling and requires further model improvements.

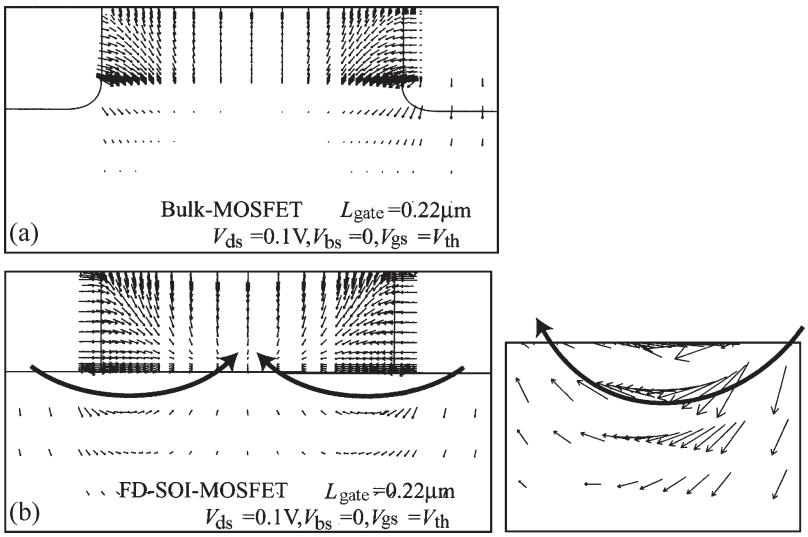

Fig. 8. Field distributions (a) in the bulk-channel region and (b) in the SOI-channel region together with an enlargement of the right side part.

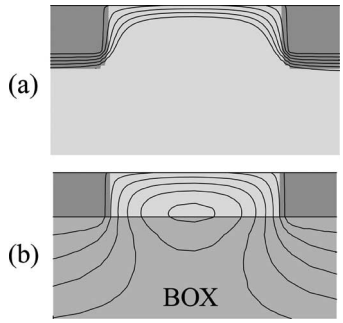

Fig. 9. Potential distribution in the channel region (a) of a bulk MOSFET and (b) of an SOI-MOSFET.

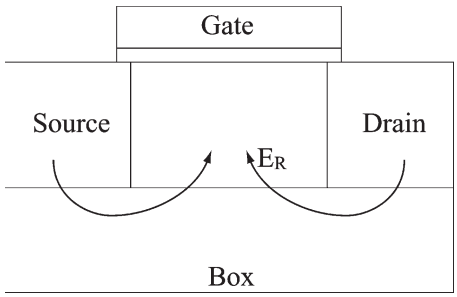

Fig. 10. Schematic of the parasitic electric "detour" field via the buried oxide.

Fig. 8 shows a 2-D device simulation result of the field distribution in the SOI-channel region. An extra field from source/drain contacts to the channel via the buried oxide, which we call "detour field," can be clearly seen. For comparison, the distribution of the bulk case is depicted as well. The origin of the extra field is understood from the potential distribution shown in Fig. 9. The potential drop within the buried oxide is influenced by the contact potentials and shows a 2-D distribution. Fig. 10 shows a schematic of the field distribution in the BOX region. This 2-D detour field from the contacts to the SOI-MOSFET channel through the BOX layer has to be modeled. To obtain a closed form for the parasitic detour field some simplifications are introduced, as shown in Fig. 11. The

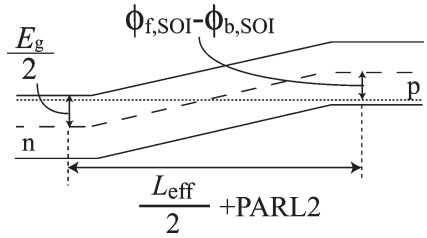

Fig. 11. Considered potential distribution along the arrows in Fig. 10.

potential difference between the source/drain contacts and that in the channel is written as

$$\phi_R = \frac{E_g}{2} + \phi_{\mathrm{f,SOI}} - \phi_{\mathrm{b,SOI}} \tag{23}$$

where E_g is the band gap and $\phi_{\mathrm{f,SOI}}$ is the Fermi potential. This potential difference ϕ_R is assumed to disappear within the channel. If the starting position of the detour field is away from the contact edge by PARL2, the detour-field E_R can be written in the form

$$E_R = \frac{(E_g + 2\phi_{\mathrm{f,SOI}} - 2\phi_{\mathrm{b,SOI}} + V_{\mathrm{ds}})}{\frac{L_{\mathrm{eff}}}{2} + \mathrm{PARL2}} \tag{24}$$

where $\phi_{\mathrm{f,SOI}}$ at threshold condition is written as

$$\phi_{\mathrm{f,SOI}} = \frac{kT}{q} \ln \frac{N_{\mathrm{sub,SOI}}}{n_i}. \tag{25}$$

However, analytical description of $\phi_{\mathrm{b,SOI}}$ is not possible. Thus, we used the 2-D device simulation result of 0.3 V. The final threshold voltage shift due to the parasitic detour field is written as

$$\Delta V_{\mathrm{thR}} = \mathrm{ESOI} \times t_{\mathrm{FOX}} \times E_R \tag{26}$$

where ESOI and PARL2 are parameters modifying the magnitude of the detour field to compensate for errors induced by the introduced simplifications. Thus, the enhanced SCE of the

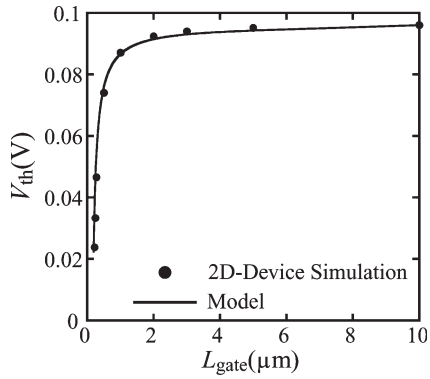

Fig. 12. Fitted $V_{\rm th}-L_{\rm gate}$ characteristic for $V_{\rm ds}=0.1$ V and $V_{\rm bs}=0$ V, which includes the modeling of the additional SCEs from the "detour" field of Fig. 10.

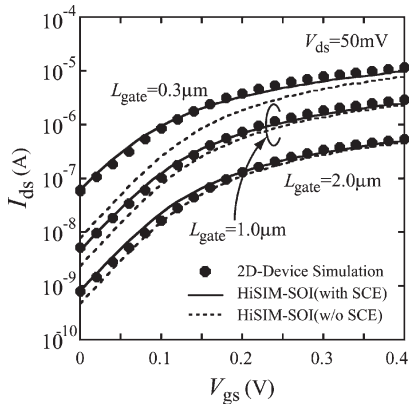

Fig. 13. Comparison of compact-model calculated drain–current ($I_{\rm ds}$) with 2-D device simulator results as a function of the gate voltage ($V_{\rm gs}$) for different gate lengths with and without the SCEs.

SOI-MOSFET is modeled as a further threshold modification, and this $V_{\rm th}$ shift is implemented into HiSIM-SOI as

$$V_{\rm th} = V_{\rm th(LONG)} - \Delta V_{\rm th} - \Delta V_{\rm thR}$$
$$V'_{\rm gs} = V_{\rm gs} - V_{\rm fb} - \Delta V_{\rm th} - \Delta V_{\rm thR}. \quad (27)$$

The calculated $V'_{\rm gs}$ with the SCEs is incorporated in the Poisson equation for calculating the surface potentials. A good agreement of the compact-model calculated $V_{\rm th}-L_{\rm gate}$ characteristic with the 2-D device simulation result down to 0.22 μm is thus achieved for the 0.25-μm CMOS technology, as verified in Fig. 12.

III. Calculation Results

The drain–current equation is derived by integrating the current–density equation along the channel in the same manner as for the bulk MOSFET [8], [14]. Calculated current–voltage characteristics are compared in Fig. 13 with 2-D device simulation results for different $L_{\rm gate}$. For the calculation, parameter values relating to the mobility are fitted to the simulation results. The conventional universal mobility description for the bulk-MOSFET [15] was applicable without any modification. Calculated inverter characteristics for different $L_{\rm gate}$ are shown in Fig. 14.

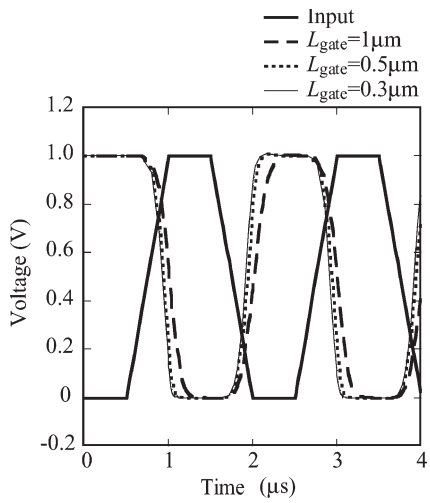

Fig. 14. Calculated transient characteristics of an inverter with HiSIM-SOI for different gate lengths.

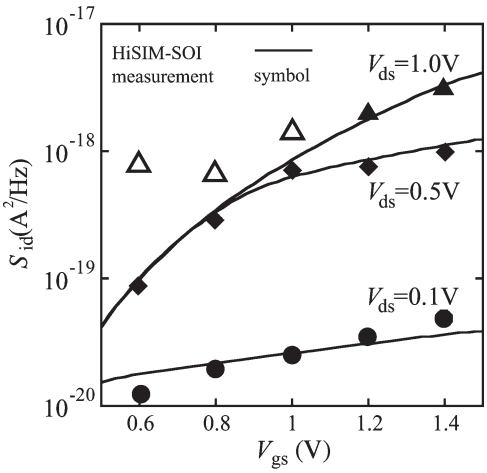

Fig. 15. Measured and calculated $1/f$ noise characteristics at the frequency of 100 Hz. The deviating points shown by the three open triangles are due to due to additional impact-ionization effects, which are not yet included in HiSIM-SOI.

For further evaluation of the developed model, $1/f$ noise characteristics are verified with HiSIM-SOI. This is because the $1/f$ noise is sensitive not only to the drain–current, but also to the charge distribution in the channel [16], [17]. Fig. 15 shows the comparison of the calculated noise characteristics with measurements, where each measurement point is the averaged noise intensity $S_{\rm id}$ out of ten measurements. For the simulation two model parameters are fitted: NFTRP determining the magnitude of the $1/f$ noise and NFALP determining the contribution of the mobility fluctuation due to carrier trap/detrap [18]. The fitted NFTRP value is the nearly the same as that of the bulk-MOSFET, and NFALP is about ten times larger than for the bulk-MOSFET. Good agreement of the measured and simulated noise–voltage characteristics is the proof of an accurate calculation of the carrier concentration and its distribution along the channel. Three measurement points depicted by open triangles for $V_{\rm ds}=1$ V show a clear deviation from expected noise characteristics. The deviation is enhanced with reduced $V_{\rm gs}$. The reason for the deviation is attributed to impact ionization, which is not yet included in the HiSIM-SOI model.

IV. Conclusion

In summary, a major contribution over the existing SOI-MOSFET models [2]–[5] is the completely surface-potential-based formulation of the reported compact SOI-MOSFET model and its consistent charge calculation so that charge conservation is not violated. Further major contributions are the description of the SCEs, resulting from the horizontal electric field in the MOSFET channel and the inclusion of additional SCEs related to the "detour" field from the source/drain contacts through the buried oxide. In particular, the inclusion of the "detour" field is found to be necessary to quantitatively reproduce the SCEs.

The developed compact surface-potential model for the SOI-MOSFET is named HiSIM-SOI and is verified to reproduce measured I–V characteristics as well as $1/f$ noise data. A HiSIM-SOI implementation into the circuit simulator simulation program with integrated circuit emphasis (SPICE) 3F5 [19] has been used to verify the stable circuit simulation.

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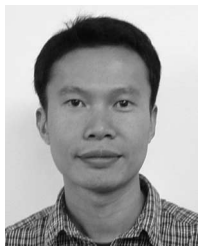

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