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Abstract

Besides further scaling of the metal-oxide-semiconductor transistor, which has continuously been achieved for these 35 years in large-scale integration, three-dimensional transistors having fin-type silicon substrate have been increasingly important for its promising potential to ultimately scaled ones. In this research, a beam-channel transistor featuring very-tall silicon beam has been proposed and its structure formation techniques are summarized in this article. They are tall beam formation, conformal gate formation, uniform source/drain formation, and conformal metal contact.
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Keywords: Metal-oxide-semiconductor transistor; Three-dimension; Beam channel; High-aspect ratio; Plasma doping

1. Introduction

To overcome performance degradation in further-scaled MOS transistors, three-dimensional (3-D) structures such as double-gate [1] and FINFET [2] have been proposed. As a different approach, a beam-channel transistor, BCT [3] has been proposed by the authors featuring higher-drive current in small planar area. These device structures are shown in Fig. 1. Since the height of silicon beam of the BCT is designed to be 1 μm, almost 20-times larger drive current can be expected in same planar area as compared to that of FINFET of which height is around 50 nm.

Potential applications of the BCT are a pull-down power transistor, as shown in Fig. 2, which is connected in series to a circuit block providing ultra-low stand-by current and a monolithically integrated RF power transistor, etc. To make the transistor as small as possible, a corrugated-channel transistor, CCT [3] which has multi-silicon beams has been proposed. The corrugated multi-channels provides further reduced planar area.

While, several three-dimensional, 3-D device structures have been proposed as shown in Fig. 3, such as sidewall-channel MOS transistor (a), tri-gate MOS transistor (b), beam sidewall-channel MOS transistor (c), and vertical-channel CMOS transistor (d) together with trench-capacitor DRAM cell [4,5].

Targets of this research and development are shown in Fig. 4 aiming higher performance in terms of current drivability.

2. Experimental

Key techniques to realize BCT are (a) high-aspect ratio lithography and etching, (b) 3-D gate formation, (c) 3-D impurity doping, and (d) conformal source and drain, S/D electrode formation.

2.1. High-aspect ratio lithography and etching

Direct electron beam exposure system is employed to delineate up to 2-μm thick photoresist. Orientation-dependent preferential etching with tetra-methyl-ammonium-hydroxide, TMAH is used to form silicon beams on (110) substrate. Aspect ratios of greater than 10 can readily be

* Corresponding author. Tel.: +81 824246269; fax: +81 824227185.
E-mail address: sunami@sxsys.hiroshima-u.ac.jp (H. Sunami).

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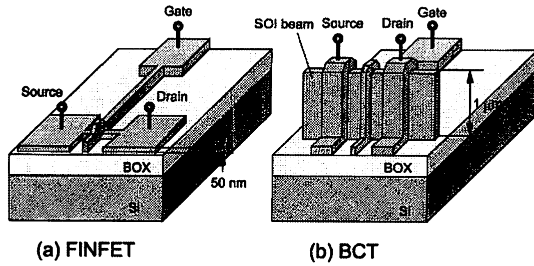

Fig. 1. Proposed 3-D MOS transistors such as FINFET (a) and beam-channel transistor, BCT (b).

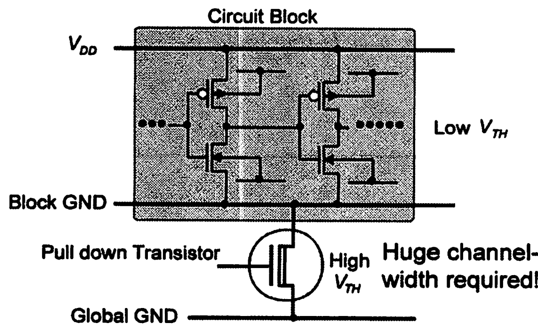

Fig. 2. A potential application of BCT for a pull-down transistor for a circuit block to control power consumption and stand-by current.

obtained in this etching. Fig. 5 indicates 31-multi-channel silicon beams on (1 1 0) silicon substrate. Details of the formation techniques were described in the previous paper [3].

Using this multi-channel beams, corrugated-channel transistor, CCT are realized. Obtained drain currents are shown in Fig. 6 clearly showing more than 5-fold increase in the current.

2.2. 3-D gate formation

Conformal gate delineation on tall silicon beam is also a key to realize sub-μm gate length, however, there may be no choice but to utilize isotropic etching at present. A less-directional plasma etching technique can realize the gate length almost equal to the height of the silicon beam at present. Fig. 7 shows an imagined failure of side-wall residue generation with anisotropic etching.

For side-wall spacer formation for the gate shown in Fig. 7 (b), impurity-enhanced oxidation is applied [6]. With this technique the polysilicon gate is covered with its own oxide in self-aligned manner. Obtained structure is shown in Fig. 8.

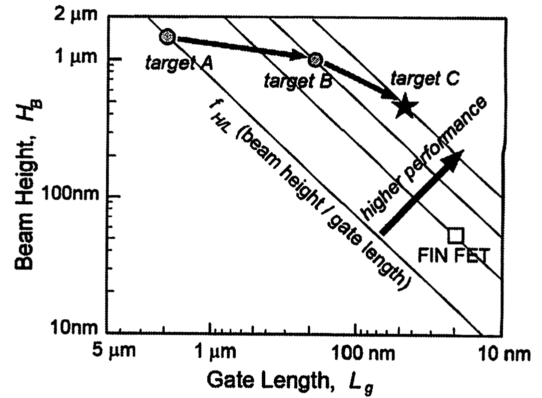

Fig. 4. Device targets of this study.

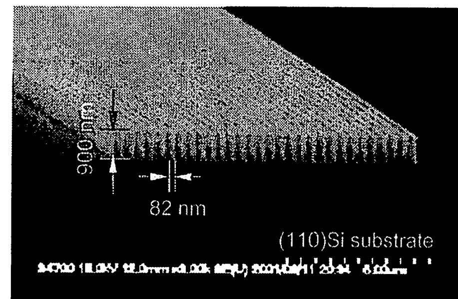

Fig. 5. Realized 31-multi-channel silicon beams of which height and width are 900 nm and 82 nm, respectively.

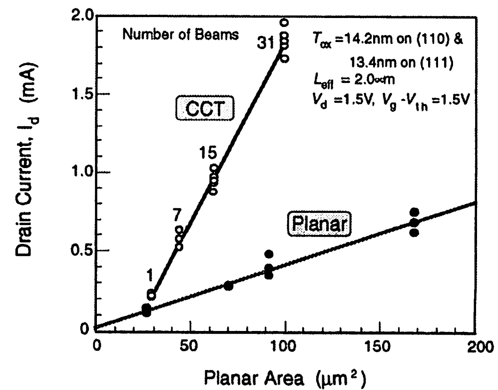

Fig. 6. Obtained drain currents of a CCT (target A) of which channels are already shown in Fig. 5. Both transistors are fabricated on a same wafer.

2.3. 3-D impurity doping

Since strongly directional ion implantation may not be adequate to achieve uniform doping to tall comb-shaped

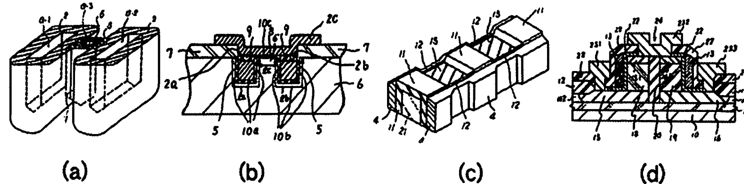

Fig. 3. Proposed three-dimensional device structures utilizing side-wall channel of silicon beam.

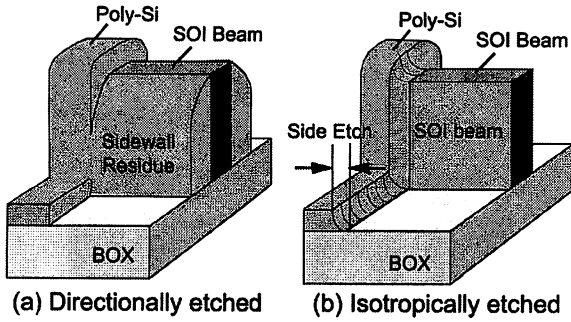

Fig. 7. Presumed hazardous residue generation along silicon beam at gate formation step.

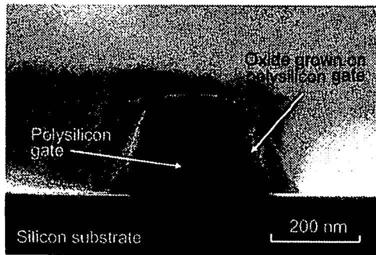

Fig. 8. Self-aligned side-wall oxide formation with impurity-enhanced oxidation.

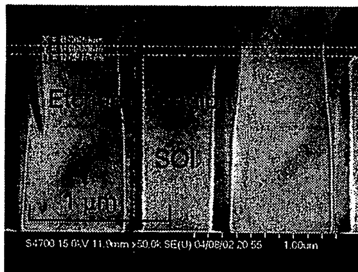

Fig. 9. Arsenic plasma doped layer along a beam surface delineated with preferential wet etching.

silicon beams, plasma doping with AsH_3 + Ar is utilized to form lightly doped region along the beam surface. Fig. 9 shows an example of the plasma doping along a beam surface [7]. An obtained typical sheet resistance value is about 500 Ω/sq.

This plasma doping is adequate for formation of extension of source and drain in terms of resistivity. SIMS profiles are shown in Fig. 10. Resistivity and profile are adequate, however, induced plasma damages obviously degrade gate oxide integrity at present causing degraded transistor performance.

An obtained device structure is shown in Fig. 11 with plasma doping. Rounded corners of the silicon beam was caused by sputtering during the plasma doping. This also caused severe degradation of device performance in terms of transconductance and off current as shown in Fig. 12. Further investigation and the improvement are inevitable to obtain satisfactory device performance.

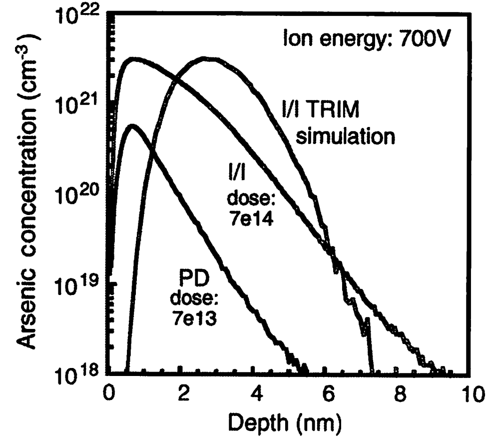

Fig. 10. SIMS profiles for ion implantation, I/I and plasma doping. PD. At most 1% of arsenic atoms is electrically active. The rest of 99% flow into substrate except the wafer.

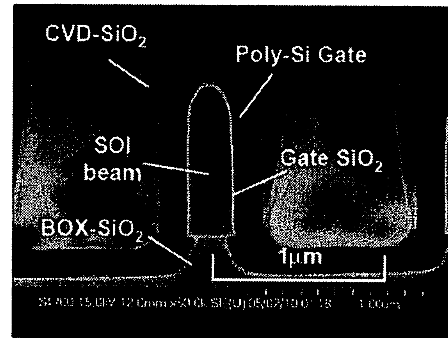

Fig. 11. An SEM cross section of realized beam-channel transistor with plasma doping. Rounded top corners were caused by plasma sputtering.

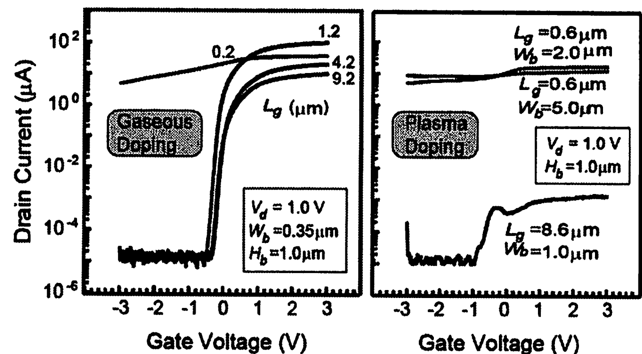

Fig. 12. An example of plasma damage which caused decreased on-current and increased off-current.

2.4. Conformal S/D electrode formation

While, very low resistance of source and drain (S/D) regions are also inevitable not to sacrifice transistor drivability. Ni-silicided S/D beam, of which cross section is shown in Fig. 13, achieves a resistivity of 2.5×10^{-5} Ω cm, while phosphorus-doped beam, 4.2×10^{-4} Ω cm. To make electrode contact to tall S/D, TiN CVD method can be

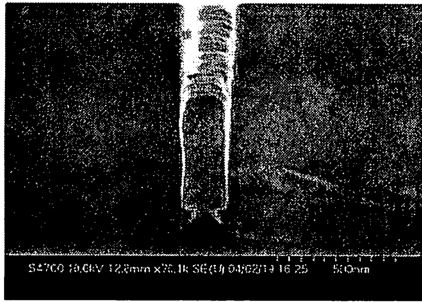

Fig. 13. Ni-silicided silicon beam to be used for low resistive source and drain regions.

used. Conventional aluminum sputtering technique is not adequate due to its poor conformability.

Obtained resistance with Ni silicidation is shown in Fig. 14 as compared to phosphorus-doped n^+ region. Almost 1/10 resistance value is realized.

A cross section and performance of the target B of CCT are shown in Figs. 15 and 16. Increased drain currents are realized in proportion to the number of the beams.

A ratio of on-drain curin current is shown in Fig. 17 for this BCT. These characteristics suggest that gate controllability strongly increases with decreasing beam width. This implies that channel regions which expand from both sidewall of the beam coincide each other in beam width region of less than around 200 nm resulting in strong subthreshold current suppression.

2.5. Emerging techniques for highly self-aligned 3-D MOS transistor structure

In addition to these techniques to obtain 3-D MOS transistor cited above, a novel technique to realize highly

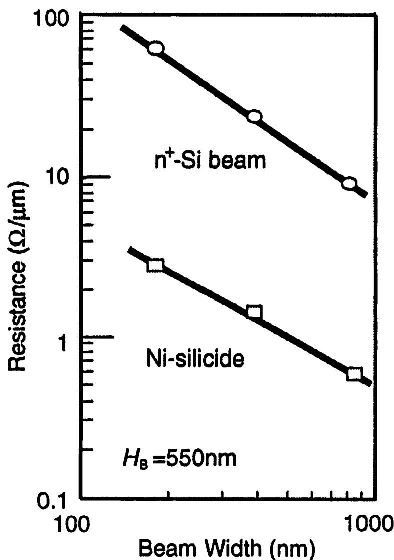

Fig. 14. Realized resistance of Ni-silicided and phosphorus-doped silicon beams of which height is 550 nm.

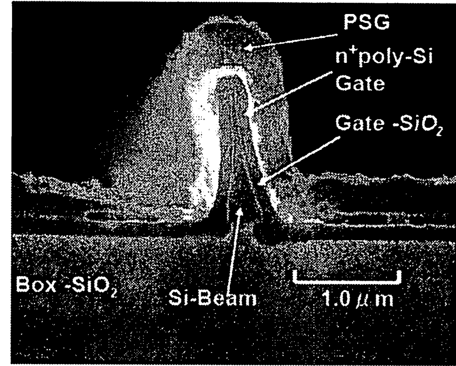

Fig. 15. An SEM cross section of the target B of CCT fabricated on (1 0 0) SOI wafer.

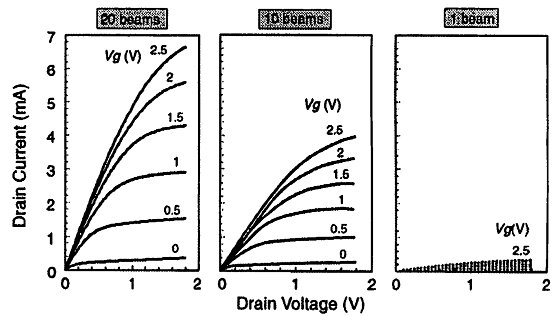

Fig. 16. Obtained drain currents of the target B of CCT fabricated on (1 0 0) SOI.

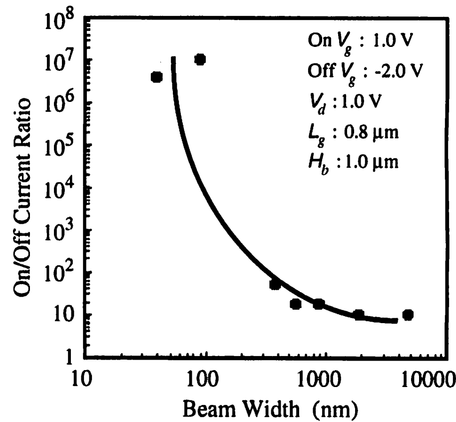

Fig. 17. Obtained on/off current ratio for BCT fabricated on (1 0 0) SOI.

self-aligned structure is proposed as shown in Fig. 18 together with its equivalent circuit. By etching Gates-1 and 2 with overlaying Gate-3, gate lengths of the three gates are same in principle. The key etching utilizes the same technique previously shown in Fig. 8. During the etching Gate-3 is covered with its own oxide.

Device performance of this self-aligned triple-gate MOS transistor is satisfactory. Gate controllability in terms of drain current and transconductance for these triple gates is shown in Fig. 19. Performance of single gate and connected triple gate is obvious. This highly self-aligned

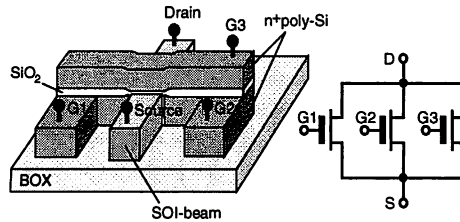

Fig. 18. A proposed highly self-aligned triple-gate structure and its equivalent circuit.

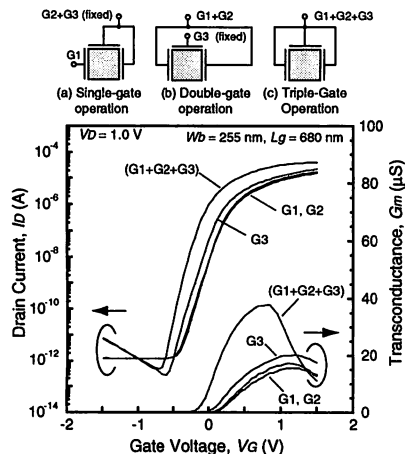

Fig. 19. Drain current vs. gate voltage characteristics of the highly self-aligned triple-gate MOS transistor.

structure has a strong potential to further reduce planar area on a silicon chip.

Presumed shortcomings may be (a) increased stray capacitance among three gates and (b) only one configuration of parallel triple gates however, they will be overcome with an appropriate application in LSI circuits.

3. Conclusion

Key techniques to realize 3-D MOS transistor such as the CCT are addressed. They are successfully carried out, however, the channel length which is smaller than the beam height is still difficult to get with sufficient reproducibility caused by high-aspect-ratio pattern formation. Furthermore plasma doping should be improved to some extent regarding plasma damage generation.

Since BCT/CCT have achieved excellent device performance corresponding to their tall and multi-beam structure, they provide strong potential for applying themselves to area-conscious, i.e., cost-conscious LSI integrating on-chip power transistor. While, even if sub-half-μm gate length has already been obtained on 0.5-μm tall silicon beam, further scalability beyond sub-100 nm is not yet achieved.

In addition to these techniques, a novel method to realize highly self-aligned triple-gate MOS transistor is proposed. In preliminary experiments, device performance is satisfactory. This structure is expected to be very promising for planar-area reduction in certain applications in LSI circuits.

Acknowledgements

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