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Influence of thermal annealing on compositional mixing and crystallinity of highly selective grown Si dots with Ge core

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Abstract

We have studied the compositional mixing and the crystallinity of Si dots with Ge core (~20 nm in average dot diameter), which were prepared on thermally grown SiO_2 by highly selective low-pressure chemical vapor deposition (LPCVD), as a function of annealing temperature in the range of 540–1000 °C. Raman scattering spectra of multiply stacked structures consisting of dots with Ge core and 2 nm-thick SiO_2 interlayers indicate that compositional mixing occurs partly at Si/Ge interface during the sample preparation, where the sample was heated up to 600 °C. Also, 800 °C annealing promotes Si–Ge alloying between Si clad and Ge core, and degrades the crystallinity. By 950 °C annealing, SiO_2 reduction with diffused Ge atoms to form volatile GeO_x units becomes significant, resulting in the generation of Si–Si bonds. Additionally, XPS analysis of annealed single layer structures confirms the incorporation of Ge atoms into Si clad from Ge core and the formation of GeO_x at the Si clad surface.

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Keywords: Compositional mixing; Spherical Si dots; Ge core; Thermal stability; SiO_2 reduction; LPCVD

1. Introduction

Nanometer size dots with a Si/Ge stacking structure have attracted extensive interest because of their unique properties associated with carrier confinement [1]. The thermal stability of SiGe/Si and Ge/Si interfaces, has so far been studied in $Si_{1-x}Ge_x$/Si superlattices [2], SiGe nano-islands embedded in Si [3] and Ge nano-islands on Si [4]. It has been reported that the interdiffusion coefficient of the nano-islands was much higher than that of layered structures and also atomic interdiffusion can decrease the strain energy.

For precise control of the three-dimensional size effect in the dots, annealing temperature dependence of the intermixing and crystallinity has yet to be studied in detail. We have studied self-assembling of nanometer Si dots on SiO_2 by controlling the early stages of LPCVD of monosilane and also demonstrated the spatial arrangement and positioning of Si dots on SiO_2 [5]. We have extended our research to the formation of Si dots with Ge core by alternately controlling the selective growth conditions in LPCVD using pure SiH_4 and GeH_4, and we found the highly selective growth of Ge on the pregrown Si dots and subsequent complete coverage of Si cap [6]. Introduction of Ge core to Si dot enables us to enhance the carrier confinement and to improve

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retention characteristics of Si dot floating gate memory devices.

In this paper, we focus the characterization of compositional intermixing in the Si dots with Ge core and the crystallinity as a function of annealing temperature.

2. Experimental

Hemispherical single-crystalline Si dots (4–5 nm in height) were first grown on thermally grown SiO_2 on Si(1 0 0) at 560 °C from the thermal decomposition of pure SiH_4 by maintaining the gas pressure at 66.66 Pa. Ge deposition was performed selectively on pregrown Si dots at 400 °C for 3 min using 5% GeH_4 diluted with He and subsequently followed by the Si selectively deposition on the dots at 540 °C under a SiH_4 pressure of 2.66 Pa. The sizes of the Ge core and the Si cap were 3–4 nm and 5–6 nm in height, respectively. To minimize the compositional mixing during this preparation process, after each deposition step, the CVD chamber was completely purged with dry N_2 and evacuated down to $\sim 1.33 \times 10^{-5}$ Pa. For preparing multiply stacked dots structures, Si dot formation with areal density as high as $\sim 2 \times 10^{11}$ cm^{-2} was carried out on as-grown SiO_2 without the dilute HF treatment, using a condition that pure SiH_4 under 7.99×10^{-2} Pa was decomposed at 590 °C for 35 s, Ge core and subsequent Si cap formation were done with the same condition mentioned above, followed by the surface oxidation. The surface oxidation of the Si cap was performed at 600 °C to form ~2 nm-thick SiO_2 and the process sequence mentioned above was repeated five times. Some of the samples were annealed isochronally for 5 min each in temperature range of 550–800 °C for a single layer and 800–1000 °C for a five-stacked dots structure in N_2 ambient. Structural changes with annealing were characterized by high-resolution X-ray photoelectron spectroscopy (XPS) for a single layer structure and Raman scattering measurements for a five-stacked structure after each annealing step. For high-resolution XPS and Raman scattering measurements, monochromatized Al Kα (1486.6 eV) and a p-polarized 441.6 nm line from a He-CD laser were used, respectively. For further structural characterizations, the high-resolution transmission electron microscope (HR-TEM) images were also taken using a system operating at 200 kV.

3. Results and discussion

Cross-sectional TEM images show spherical nanometer dots made of a Si clad and an ellipsoidal Ge core (Fig. 1), in contrast to hemispherical pure-Si dots pregrown on SiO_2. This implies that the strained energy is larger than the bonding energy at Si/SiO_2 interface generated at the Si/Ge interface. Notice that the crystallographic orientation of the Si cap is different from that of the pregrown Si dot presumably due to the structural strain at the Si/Ge interface. The orientation of Ge core is not clear because of its poor contrast.

Raman scattering spectra for as-prepared samples as shown in Fig. 2 implies that the compositional mixing partly occurs at Si/Ge interfaces during the sample preparation as verified from relative intensity of Si–Ge bonds with respect to Si–Si and Ge–Ge photon intensity. Fig. 3 shows Raman scattering spectra for the samples annealed at various temperatures. To reveal the spectral change in the Si–Si TO phonon mode for the Si clad around 500 cm^{-1}, the TO phonon signals originating from the Si(1 0 0) substrate were subtracted from the measured spectra for the annealed sample. The evolution of the signal due to Si–Ge phonon mode at ~400 cm^{-1} indicates that the further

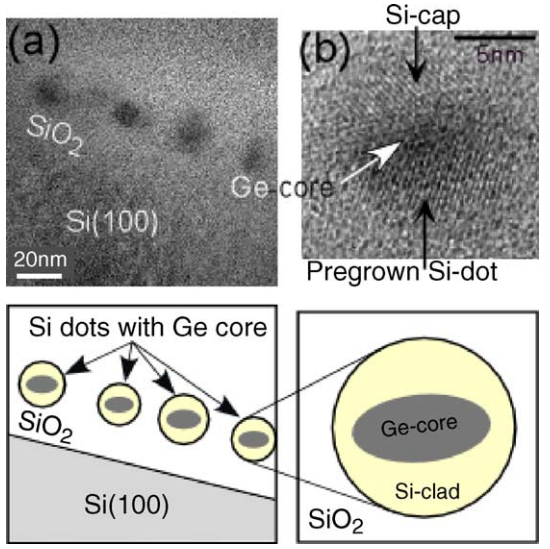

Fig. 1. The cross-section of HR-TEM images of Si dots with Ge core (a) an as-prepared sample after Si-cap formation; (b) a magnified image of single dot, corresponding to their schematic images.

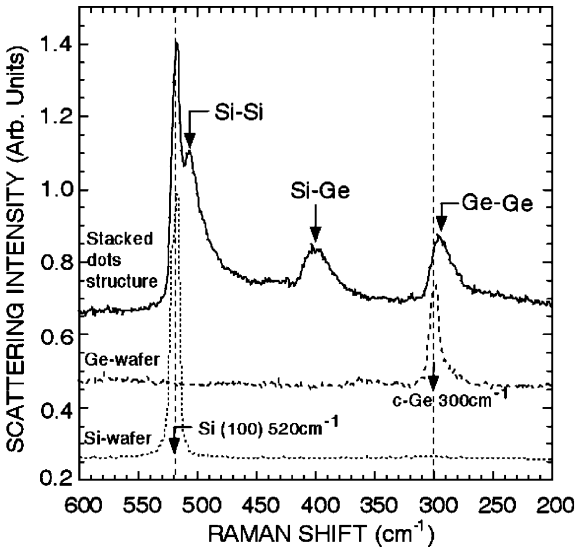

Fig. 2. Raman scattering spectra for an as-prepared five-stacked structure. The Raman spectra of Si(1 0 0) and Ge wafer are also shown as references.

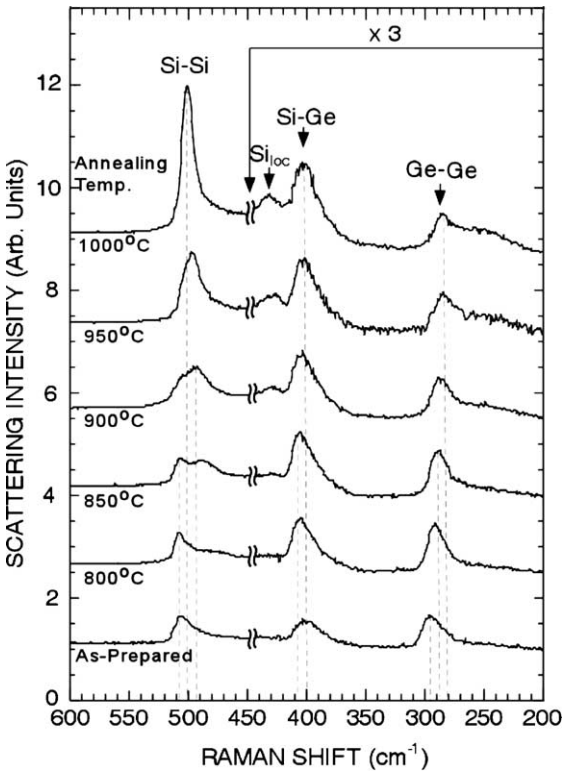

Fig. 3. Raman scattering spectra of a five-stacked structure of the Si dots with Ge core after annealing at various temperatures. The signals originating from Si(1 0 0) were subtracted from the as-measured spectrum. For each spectrum, the scattering intensity in the range of 200–450 cm^{-1} was magnified by a factor of 3.

compositional mixing is promoted with annealing at temperature as high as 800 °C. The ~490 cm^{-1} peak seen in the Raman spectrum of the sample annealed at 850 °C indicates the intermixing between the Si clad and the Ge core and the deterioration of the crystallinity of the Si clad. With 950 °C annealing, the compositional intermixing seems to spread all over the Si clad. A significant increase in the Si–Si TO phonon intensity with 1000 °C annealing suggests that the Ge atoms reaching the Si clad/SiO_2 interface reduce SiO_2 with the formation of volatile GeO units and thus the Si–Si bonds are generated. A broad Raman feature around 250 cm^{-1} is attributable to the trace of GeO_x. Notice that, the local Si TO phonon mode, in which Si atoms are bonded to one or more Ge atoms [7], emerges at ~430 cm^{-1} with annealing higher than at 900 °C. This result implies that the ordering in the atomic arrangement is improved at such a high annealing temperature accompanied with progressive alloying. The origin of the observed peak shift in the Si–Ge phonon mode towards the lower wavenumber side is not clear yet, but might be related to a structural relaxation accompanied with a size-reduction or annihilation of Ge core.

In fact, TEM images for the sample annealed at 1000 °C show the shrinkage of the stacking dot structure due to reduction of SiO_2 in among dots. Also, the in-plane current characteristic measured with co-planar electrodes implies an increase in the current density under 15 V cm^{-1} up to 18.5 nA cm^{-2} for the sample annealed at 1000 °C, while for the 800 °C annealed sample the current density is 2.9 nA cm^{-2}.

The intermixing between the Si clad and the Ge core was also characterized from the XPS analysis of a single layer of dots formed on 10 nm-thick SiO_2. Fig. 4 represents the peak intensities of Si 2p and Ge 3d spectra for annealed samples as a function of annealing temperature, in which the metallic (0+) and oxidized (4+) components [8] are separately plotted. With increasing annealing temperature, Si^{0+} signals originating from the Si clad decrease gradually, and the Si^{4+} signals from the underlying SiO_2 and surface

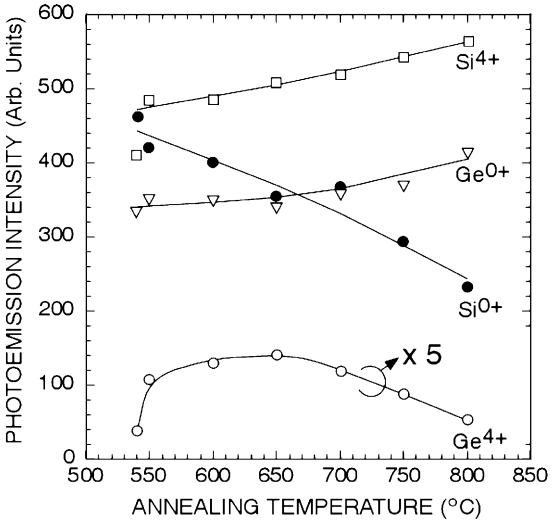

Fig. 4. Si2p and Ge3d intensities for as-prepared and annealed samples at different temperatures, which were taken at photoemission take-off angle of 90°. The signals peaked at 99.5, ~103.7, 29.5 and ~33.7 eV are assigned as $Si2p^{0+}$, $Si2p^{4+}$, $Ge3d^{0+}$ and $Ge3d^{4+}$, respectively. For this experiment, a single layer of Si dots with Ge core was prepared on 10 nm-thick SiO_2/Si(1 0 0). Ge^{4+} signals intensity was magnified by a factor of 5.

oxide on the dot surface and Ge^{0+} signals increase slightly. Considering no detectable chemical shift for Si–Ge bonds without any oxygen atoms, the result indicates that, although the Si clad surface was oxidized during annealing after air exposure, Ge atoms diffuse toward the dot surface, that is, compositional mixing at Si/Ge interface. Notice that chemically shifted Ge 3d signals assigned to Ge^{4+} in oxide increase until it becomes its maximum at an annealing temperature around 650 °C. This indicates that thermal desorption of GeO_x becomes significant at temperatures higher that 650 °C.

4. Conclusions

The thermal stability of dot structures, which consist of Si clad (4–5 nm in height) and Ge core (3–4 nm in height), on thermally grown SiO_2 has been studied systematically as a function of annealing temperature. For multiply stacked structures with 2 nm-thick SiO_2 interlayers, progressive intermixing and deterioration of the crystallinity of Si clad in annealing at 800–900 °C are demonstrated from a distinct increase in the Raman scattering intensity due to Si–Ge TO phonons and broadening of the Si TO phonon mode. In annealing higher than 900 °C, a reduction of SiO_2 with Ge atoms diffusing at and near the Si clad surface to form volatile Ge oxide becomes significant, resulting in an increase in the Si composition accompanied with an improvement in the crystallinity. For a single layer of dots, a gradual increase in Ge signals from metallic states with annealing higher than 650 °C confirms the diffusion of Ge atoms into the Si clad and a decrease in the chemically shifted Ge signals originated from oxide is indicative of thermal desorption of volatile Ge oxide units.

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