Towards World Top-Level Hiroshima University with Outstanding Characteristics

Fundamental Philosophy and Target

- Five Guiding Principles of Hiroshima University (Established in 1995)
  1) Pursuit of Peace, 2) Creation of New Forms of Knowledge, 3) Nurturing of Well-Rounded Human Beings, 4) Collaboration with Local, Regional and International Community, 5) Continuous Self-Development
- Master Plan: Direction of Hiroshima University towards 21st Century (Established in June 2000)
  A Position as an Excellent University for Research as well as Teaching
- Essence of Medium Term Targets (Determined by the Senate in June 2002)
  Reform Hiroshima University towards World Top-Level Research University through the Leadership of the President.

Strategy

- Emphasis on Graduate School, Reorganization, Reform, Improvement
- Improvement of Education Quality at Undergraduate Courses. Clear Statement of the Achievement Targets in the Curriculum
- Promotion of World Top-Level Research by Special Financial and Manpower
- 21st Century COE Program is Really Timely for Hiroshima University.

Position and Necessity of Center of Excellence Formation Plan for Hiroshima University

Essence of Medium Term Target

1. Outstanding Highest Level Research and Educational Institution
2. Stimulating Environment for World Top-Level Research and Cultivation of New Research Seeds
3. Output of High Quality PhDs, Globally Oriented Researchers and Advanced Professionals
4. At Undergraduate Courses, Development of Cultural Education. By Introducing Program Education and Clear Statement of the Achievement Targets in the Curriculum, Flexible Talent with both Fundamental and Application Ability will be Graduated.

Challenge to the Formation of Core of Excellence

1) Special Improvement and Strengthening of the Research Fields in which the Original Features and Characters of Hiroshima University are Demonstrated.
2) Concerning the Basic Research of Culture Creation, Cultivation of the Research Seeds which are Expected to Develop in Medium and Long-Term Range.
3) Academic Research which is already World-Class is Selected, and It is Strategically Promoted. Research Fields which should be a Distinguished Feature of Hiroshima University are Improved and Centers of Excellence are Formed.
4) Close Cooperation and Dynamic Fusion of Basic and Application Research. Systematic Inclusion of New Research Fields.

Nanoelectronics for Terra-Bit Information Processing

Position and needs of this COE program

1) The Research Center for Nanodevices and Systems (RCNS), as a Core of this COE Program, has already made Considerable Contributions to the Society through Advanced Research Results, and is Distinguished Research Center of Hiroshima University (Corresponding to Previous 1st and 3rd Issues).

2) RCNS and Laboratory for Electronic Intelligent Systems of Tohoku University are the Two World-Leading Academic Centers for the Research Field "Si Integrated Circuits" in Japan. RCNS is already Positioned as a Distinguished Center of Excellence at Hiroshima University and is further Supported to Extend Its Capabilities by the Strategic Industry/University/Government Cooperations. In This Way, RCNS will Become an Important Pillar for Development of the Semiconductor Industry in Japan.

Support by Hiroshima University

1) Supply Research-Assistant Positions: Many High-Technology Equipment is Operated at RCNS.
2) The Graduate School Responsibility is Expanded: The Staff of RCNS will Enlarge Its Teaching Responsibility at the Graduate School of Advanced Sciences of Matter.
3) Invitation of Oversea Researchers: Support Research Stay of Excellent Researchers from Foreign Countries.

Expectation for the Bright Future of COE Group

Targets and Research Plan of 21st Century Center of Excellence (COE) on Nanoelectronics for Tera-bit Information Processing

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1. Abstract

We are aiming at fusion of silicon-based nanodevice, circuit and chip-architecture research for the basic construction of integrated systems with high-level recognition and learning functionality. For this purpose interactive concurrent research is being undertaken. This cooperative research brings up independent researchers who are capable of advanced, visionary and well reflecting research in a broad range of fields.

2. Introduction

In the next decade, silicon integration technology will remain the main stream of the industries micro-fabrication technology. For taking the leadership in this field, research for an evolutionary technology development is essential. Furthermore, development of a large-scale and flexible integrated information processing system is required through a joint research in the engineering fields of data and picture processing. Thus independent specialists and leaders in three different fields (process and device development, modeling combining circuits and technologies, and circuits development) are working together to fulfill the requirements.

3. Basic Idea and Objectives

Cooperative research between all elementary technologies of silicon integrated circuits at the world's top level will be undertaken as shown in Fig. 1. Through the cooperation, evolutionary development of new future main-stream technology will be realized. Thus the main goal is the development of basic technologies for: the fusion of system, circuit, device-modeling and device-fabrication research; wireless and light interconnections; vertical transistors as well as systems with high-level recognition and learning capabilities. Not only technology advancements, but through industrial promotion, a contribution to the information society will be made by this process of center-of-excellence formation. Furthermore, highly-capable human resources will be brought up by the practical education in research and development. Thus training of new specialists and leaders who are geared towards broad interacting fields is also our objectives.

Following are Objectives as Summarized in Fig. 1:

1. Merging and Unification of R&D on silicon-based system, circuit, device-modeling and device-fabrication (Figs. 2 and 3)
2. Solution of the 3-dimensional-integration problems by wireless integration technology (Figs. 4 and 5)
3. Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures (Figs. 6 and 7)

4. Plans for Formation of Research

The objectives are investigated in parallel in three independent fields at the beginning, and merged a year after a year (see Fig. 2). Following are overview of our development plan:

2002- Extension of the worldwide top-level basic-technology position. Accelerated fusion of the research activities of the program's three research pillars. Young program-member research proposals: Start of 2 cooperative projects on devices and modeling.

2003- Expansion of the cooperative research between the research fields. Promotion of research on wireless interconnects between chips. Young program-member research proposals: 2 additional cooperative projects between the device and circuit/system fields.

2004- Upgrading of the technology level in the light-interconnect and functional-memory fields to introduce them as new elementary technologies for integrated circuits.

2005- Highly efficient method for integrated device and circuit design. Basic 3-dimensional design technology for integrated circuit (vertical device) and electrical/optical integration.

2006- Establishment of the research-field organization and future-plan decision. Organizational fusion of the hard/software fields for nanodevice integration and high-level recognition.

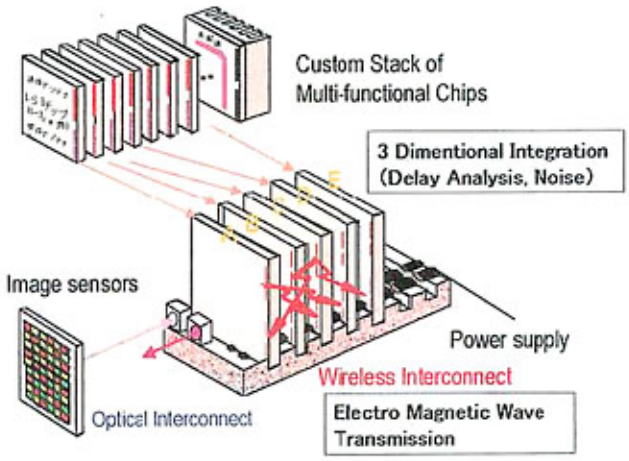


Fig. 1 Overviews of objectives.

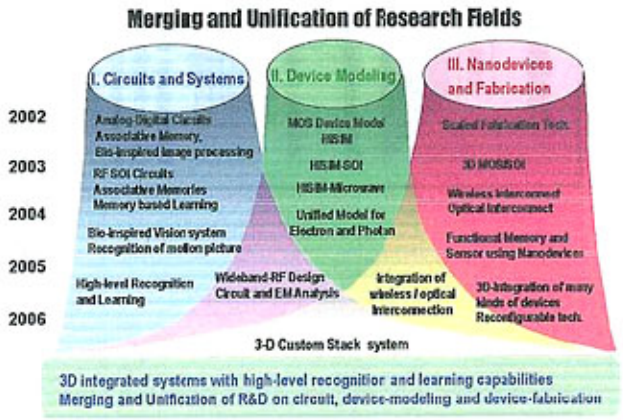


Fig. 2 Research fields cooperatively investigated.

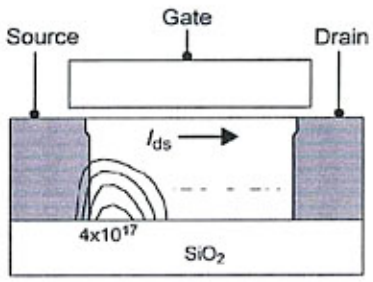


Fig. 3 Research objective for SOI-MOSFET modeling.

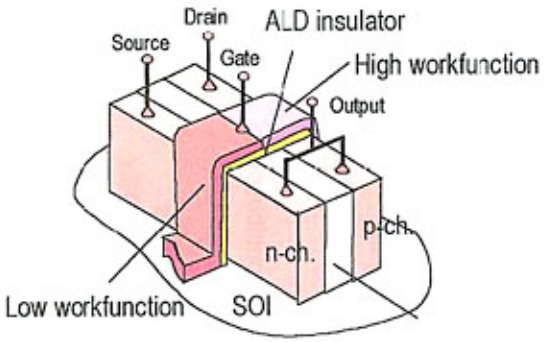


Fig. 4 Proposal for 3D integrable device.

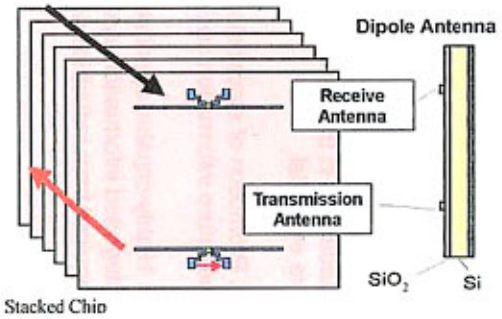


Fig. 5 Concept for communication with wireless system.

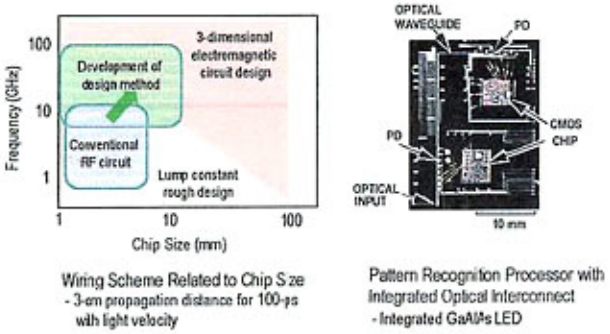


Fig. 6 Inter- and Intra-Chip Optical and RF Wirings.

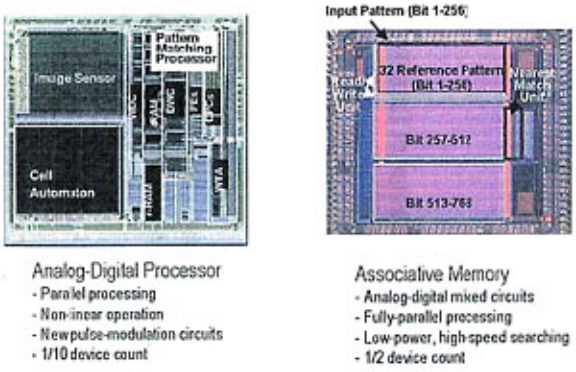


Fig. 7 System Architecture and Integrated Circuits.

21st Century Center of Excellence (COE) on

Nanoelectronics for Tera-bit Information Processing

- Targets and Research Plan -

Research Center for Nanodevices and Systems (RCNS)
Graduate School of Advanced Sciences of Matter
Hiroshima University

Needs and Requirements

1. Silicon technologies will remain the main stream of the industries for more than 10 years. For taking the leadership in this field, R&Ds for evolutionary technologies are essential.

2. Promotion of electronics industries and contribution to the future information society are required.

3. Highly-capable specialists and leaders in future integrated information system technology are strongly required from industries and academia.

Basic Idea and Objectives

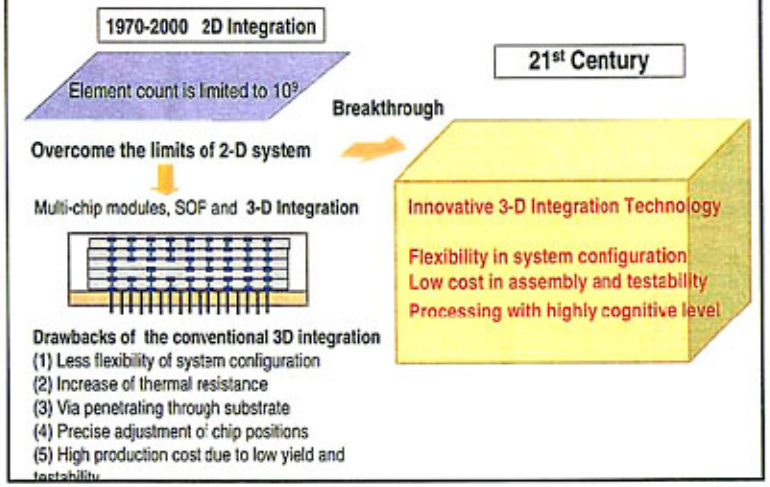
Research:

1. Merging and Unification of R&Ds on silicon-based system, circuit,device-modeling and device-fabrication
2. Solution of the 3-dimensional-integration problems by wireless integration technology
3. Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures

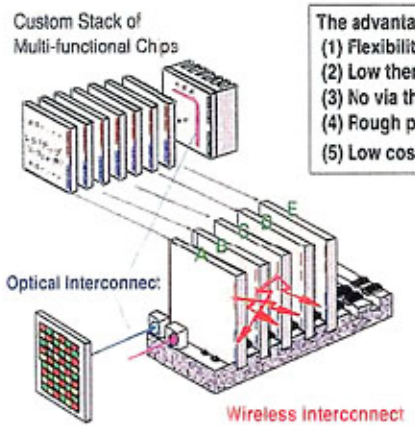
Education:

We are intending to bring up highly-capable human resources: PhD researchers who are capable of advanced, visionary and well reflecting research, in a broad range of fields, by the cooperative research.

Technology Breakthrough for Tera-scale Integration



New Three Dimensional Integration System
(3D Custom Stack Sytem)



The advantages
(1) Flexibility due to no physical connections
(2) Low thermal resistance
(3) No via through substrate
(4) Rough positioning
(5) Low cost for mounting

Hierarchical Image Recognition System (example)

A: Spatial Filters
B: Feature Extraction
C: Pattern Matching
D: Reference Pattern
E: Recognition

Three Core Research Fields

I. Circuit and System Architecture

1. RF analog circuits (Prof. Iwata and Prof. Sasaki)
2. Associative-memory based systems with recognition and learning capability (Prof. Mattausch and Prof. Koide)
3. Processing system with highly cognitive level (Prof. Iwata)

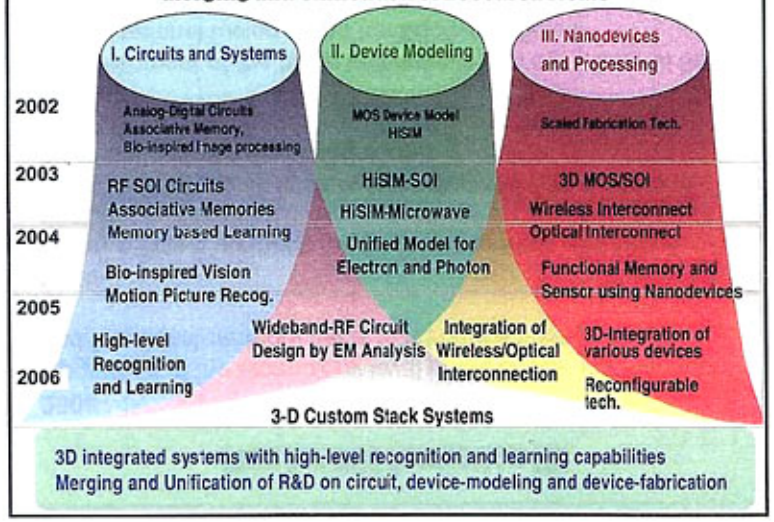
II. Device Modeling

1. Integration of electron and optical devices
2. Three Dimensional SOI-MOS device (Prof. Miura and Dr. Ueno)

III. Nanodevice and Process

1. Fundamental device scaling techniques (Prof. Shibahara and Prof. Miyazaki)
2. Ultra-small SOI-MOS devices (Prof. Sunami and Prof. Miura)
3. Functional nano-devices (Prof. Miyazaki and Mr. Murakami)
4. Wireless interconnection (Prof. Kikkawa and Prof. Sasaki)
5. Optical interconnection (Prof. Yokoyama and Prof. Nakajima)

Merging and Unification of Research Fields



3D integrated systems with high-level recognition and learning capabilities
Merging and Unification of R&D on circuit, device-modeling and device-fabrication

Plan for COE Formation (1)

2002-
Extension of the worldwide top-level basic-technologies.
Accelerate fusion of the research activities of the three fields.
Call for Young researchers and research proposals.

2003-
Expansion the cooperative research between the fields.
Promotion of the research on wireless interconnects.
Based of Young researcher's proposals, start cooperative research projects for merging the 3 fields: circuit/system, modeling and device/process.

Plan for COE Formation (2)

2004-
Upgrading of the technology level in the optical-interconnect and functional-memory fields to introduce them.

2005-
Highly efficient methods for device integration and circuit design.
Basic 3-dimensional system technology for tera-scale and electrical/optical fused integration.

2006-
Establishment of the basic technologies on the research fields.
Organizational fusion of the hard/software fields
for nano-device integration and high-level recognition system.

ducation Implementation Plan

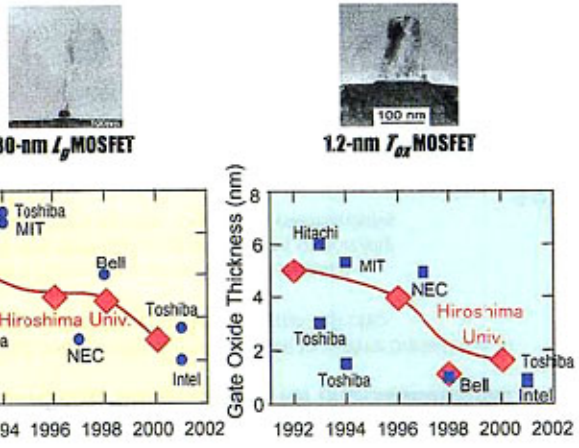
Goal:
Output of PhD students with high scientific judgment and management capability toward the future **leader** in industries and academia.

Plan:
1. Education program directly associated with the advanced research.
2. New Major for Semiconductor Integration Sciences in the graduate school
3. Improve quality of the doctor-course program
   a) Double-major & several supervisors
   b) Practical and management capabilities
   c) Severe Conditions for the PhD acquirement:
   d) International sense and communication

Nanodevices and Fabrication

- Fundamental technology development for ultimately miniaturized planar MOSFET's
- Implementation of future 3-D MOS FET's
- Proposal of non-volatile dot memory
- Proposal of on-chip, ultra-high speed signal transfer systems such as optical interconnect and wireless communication
- Basic material development for future LSI system such as low-k dielectrics and resistless patterning

Scaled MOSFET's Realized at Hiroshima University



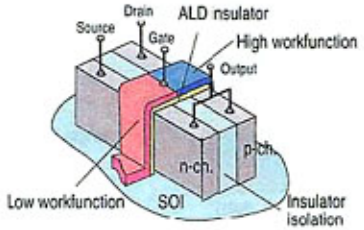
Fundamental Technologies for Ultra-Scaled Devices

Purpose :

- Elementary technology development for ultimate miniaturization of planar MOSFET
- Pioneering technology development for 3-D devices

Emerging Technologies :

- High-k ALD gate insulator with dual metal gate
  - * Conformable and controllable atomic layer deposition
  - * Optimized V_T setting with dual metal gate



An example of emerging technology application

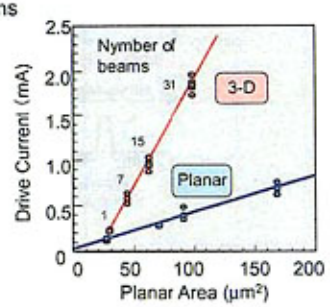
3-D (Three-Dimensional) MOS FET Structure

Target : High drive current MOS FET in relatively small planar area

- Steep and tall beam formation
- 3-D doping into steep and tall beams

A 3-D MOS FET having equivalent gate width of that of planar

An MOS FET with 31-beams of 1-μm height and 50-nm width



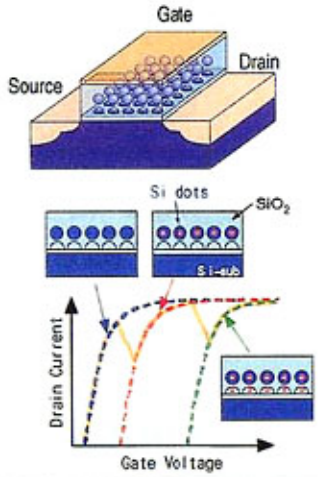
Drive current increase for multi-beam 3-D MOS

Silicon Functional Memory

Target :

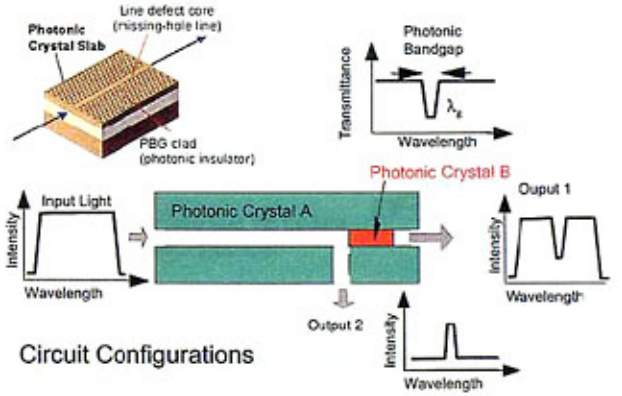
Implementation of a new non-volatile memory having potential performance of multi-bit value, defect insensitivity, long term reliability.

- Electron charging and discharging mechanism
- Self-aligned dot arrangement
- Separation performance for multi-bit memory



Compact Optical WDM Circuits using Photonic Crystals

Target : Realization of long distance, high speed wiring, and massively parallel processing by means of optical interconnection

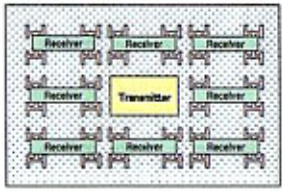


Circuit Configurations

Some Experimental Results of On-Chip Antenna

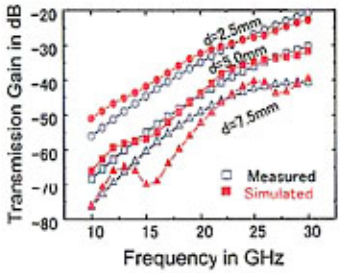
Target : Ultra-high speed data transfer with on-chip wireless communication

- Connection loss management



Antenna arrangement

Integrated dipole antenna

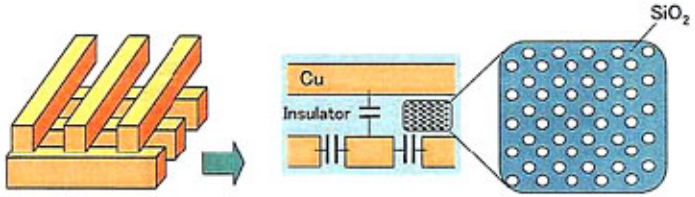


Some experimental results

Basic Technology Development for Miniatualization

Target : Evolutionary material development to realize breakthrough to signal transfer saturation on large LSI chip

- Cu wiring + Nano-porous low-k interdielectrics
- Electrical and chemical characterization of porosity
- Metal-ion drift and electric conduction mechanisms



Cu multi-layer wiring | Equivalent circuit | Nano-porous insulator

Circuits and System Architectures

I. Circuits and System Architectures

1. RF analog circuits (Prof. Iwata and Prof. Sasaki)
2. Associative-memory-based systems with recognition and learning capability (Prof. Matsuzaki and Prof. Kotde)
3. Processing system with highly cognitive level (Prof. Iwata)

II. Device Modeling

1. Integration of electronic and optical devices
2. Three Dimensional SOI-MOS devices (Prof. Miura and Dr. Ueno)

III. Nanodevices and Processes

1. Fundamental device scaling techniques (Prof. Shibahara and Prof. Miyazaki)
2. Ultra-small SOI-MOS transistors (Prof. Sunami and Prof. Miura)
3. Functional nano-devices (Prof. Miyazaki and Mr. Murakami)
4. Wireless interconnection (Prof. Kikkawa and Prof. Sasaki)
5. Optical interconnection (Prof. Yokoyama and Prof. Nakajima)

I. Circuits and System Architectures

1. RF analog circuits
   - Design technology
   - Research contents
2. Associative-memory-based systems with recognition and learning capability
3. Processing system with highly cognitive level

RF and Analog Circuit Design Technologies

Purpose

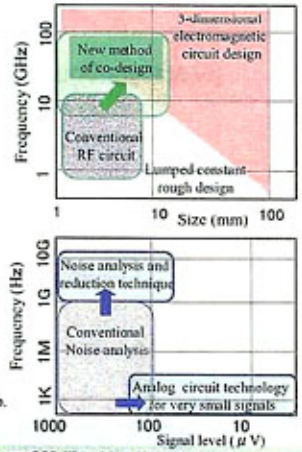
Establishment of high frequency and analog circuit technologies for the advancement of information, communication and control applications.

Scientific approach

① Co-design method for MOS devices, line connections and antenna, by unifying electromagnetic-field analysis and device modeling.
② Noise analysis and reduction technique for mixed analog/digital circuits in the domain of several deca GHz.
③ Circuit technology for analog information processing handling very small signals (device noise suppression, low voltage operation)

Originality

Programmable interface circuits for wireless and optical communication between chips mounted in 3-dimensional structures as well as between subsystems on the same chip.



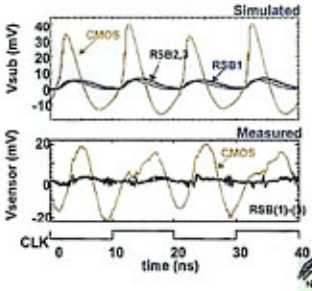
Contents of RF and Analog Circuit Research

1. RF and mixed analog/digital LSI design technology

Cross talk noise analysis and reduction techniques

Current technology analysis resolution 100ps, 1GHz, 100 μV → Target resolution 10ps, 10GHz, 10 μV

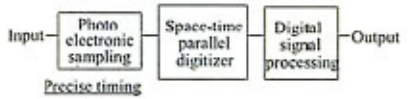
Low noise logic circuit



2. SOI-RF circuit

- Small chip area RF power amplifier
- Active broadband matching circuit
- Application of 3D MOSFETs

3.1 A-D converter for software radio



Precise timing compensation

3.2 A-D converter for living body information sensing

Voltage sensitivity: 10 μV, 100KHz, 8bit

- Low-voltage chopper stabilization technique
- Optical isolation technique

I. Circuits and System Architectures

1. RF analog circuits
2. Associative-memory-based systems with recognition and learning capability
   - Envisaged system structure
   - Image-preprocessing front end
   - Associative-memory core
   - Implementation of the learning function
3. Processing system with highly cognitive level

Structure of Envisaged Associative Memory-Based Systems with Recognition and Learning Capability

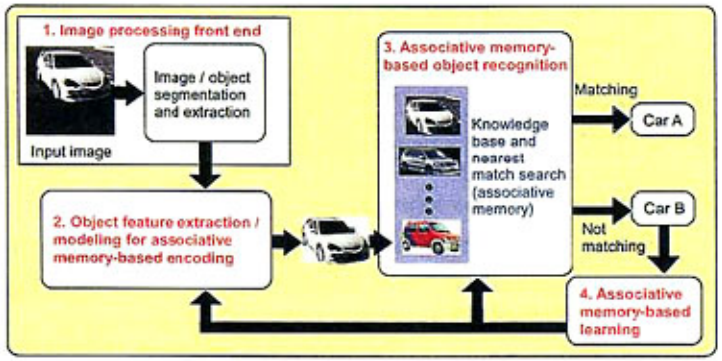
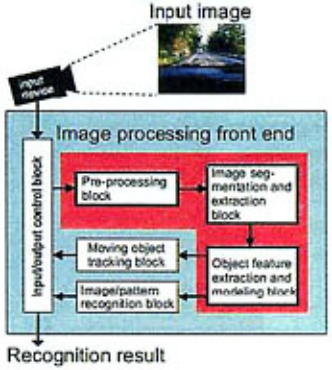


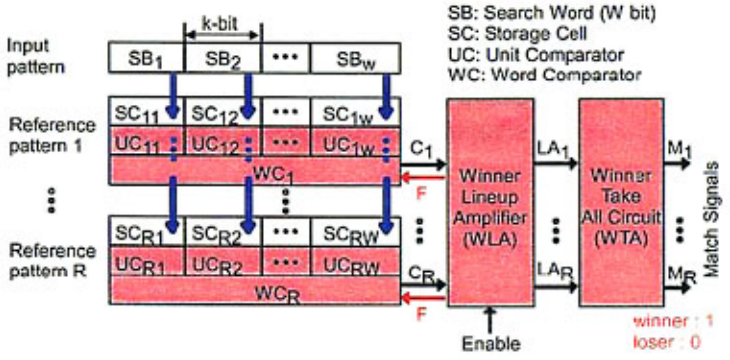
Image Segmentation and Feature Extraction for Real Time Applications



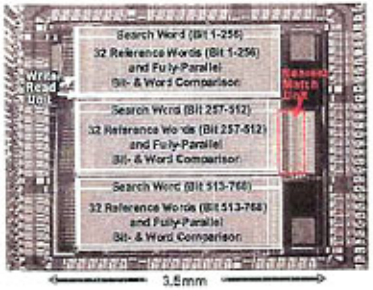
Core of the image-processing front end is the image segmentation and extraction block

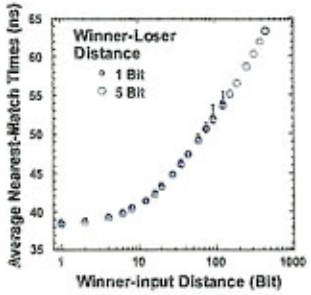
Developed test-chip of a digital CMOS-based architecture for real-time color-motion-picture segmentation

Associative Memory Architecture with Fast Fully-Parallel Match Capability



32-pattern, 24K-bit Hamming-Distance Search Memory Chip

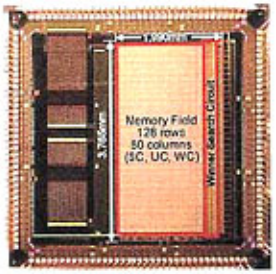


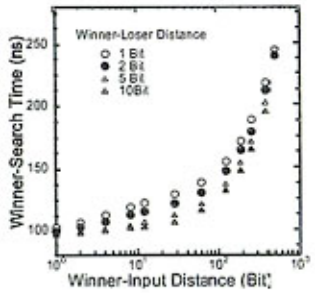


Test-chip fabricated in 0.6μm CMOS

- Nearest-match search times: < 70ns
- Power dissipation: <43mW at 10MHz (4.4mW/mm²)

128-Pattern, 10K-Bit Manhattan-Distance Search Memory Chip

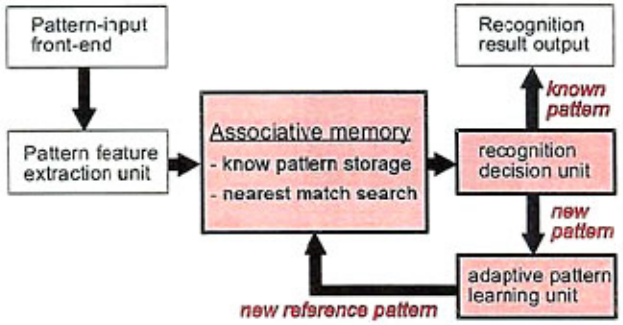




Test-chip fabricated in 0.35μm CMOS

- Nearest-match search times: < 240ns
- Power dissipation: <260mW at 10MHz (34.7mW/mm²)
- Equivalent performance: 170GOPS (20GOPS/mm²)

Associative Memory-Based Adaptive Learning



The adaptive pattern-learning unit uses the distance information, knowledge-based similarity-reasoning algorithms and information about previous unknown patterns for the decision of adding an unknown pattern to the knowledge base.

I. Circuits and System Architectures

1. RF analog circuits
2. Associative-memory-based systems with recognition and learning capability
3. Processing system with highly cognitive level
   - Base technologies
   - Concepts for a prediction and strategy based robot brain

Base Technologies of Highly Cognitive Processing System

Purpose

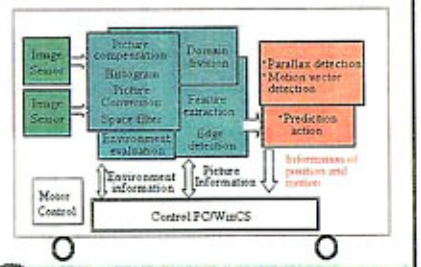
Development of the base technologies for brain-type processors with high cognitive capability.

Vision technology for self-running robot control

- Acquisition of vision information for movement control
- Evaluation and compensation of scene fluctuation caused by movement

Scientific approach

- Vision processing techniques with high flexibility and high reliability.
- Learning scheme for acquisition of strategy models.
- Base technologies for a robot with predicting and planning capability.



Originality

- 3-dimensional integrated vision system with reliable compensation and multi-algorithm parallel processing (3DCSS)
- Robot brain recognizing surrounding motion and environmental change, and elaborating an action strategy from visual information.

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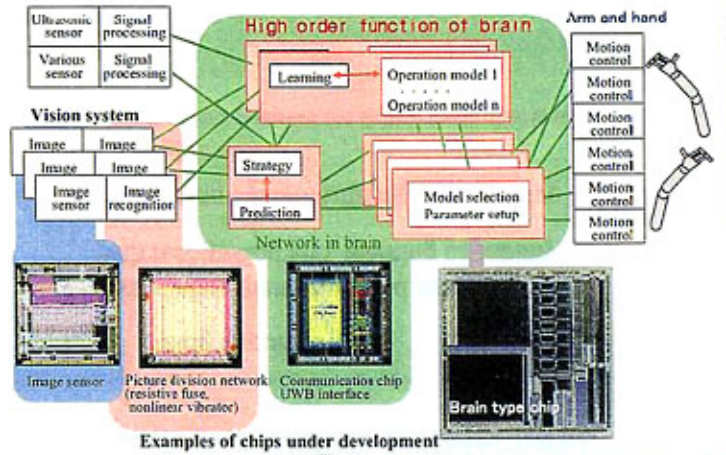
Prediction and Strategy Based Robot Brain



Examples of chips under development

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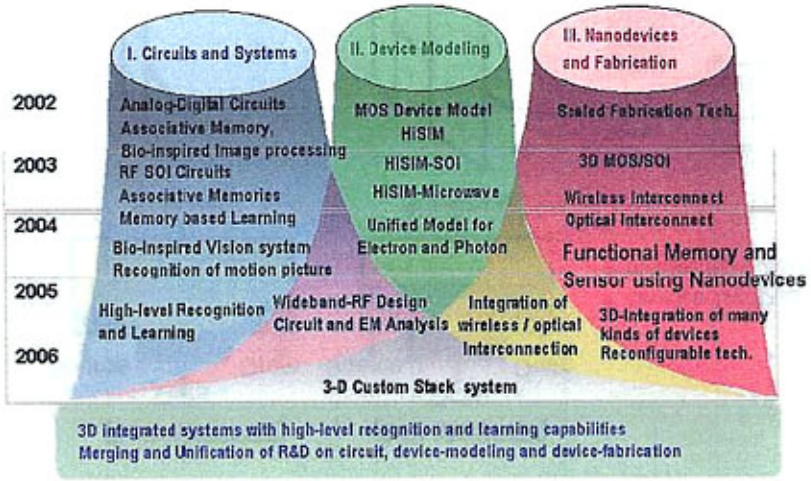
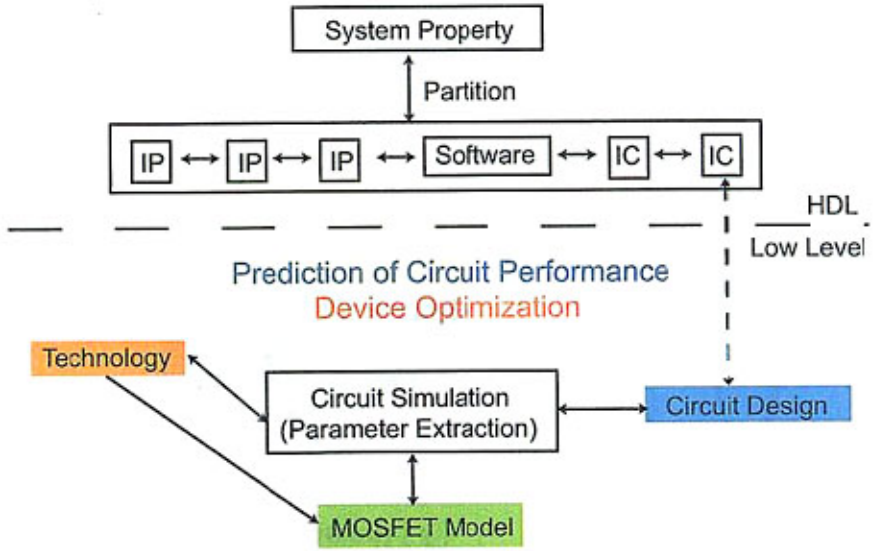
Nanoelectronics for Tera-bit Information Processing

II. Device Modeling



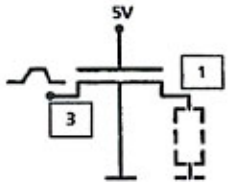


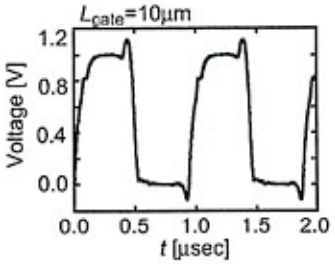
Prediction of Circuit Performance
Device Optimization

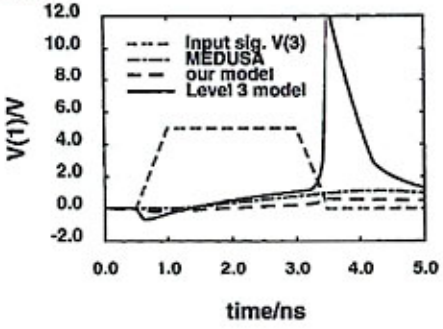
Accurate Model

HiSIM

(Hiroshima-university STARC IGFET Model)



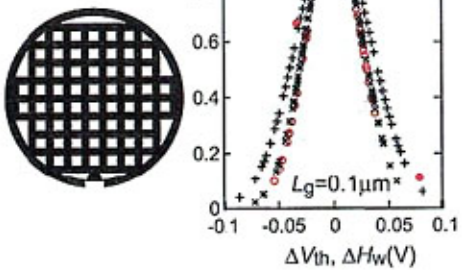


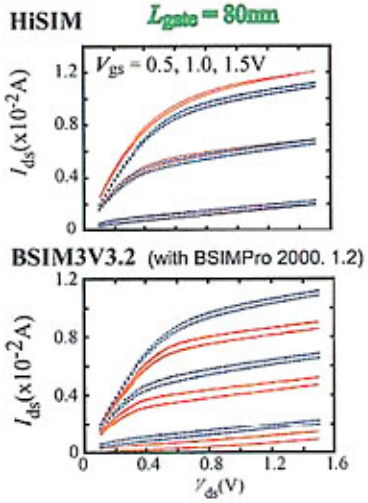


HiSIM : Predictability

Nr. Model Param.

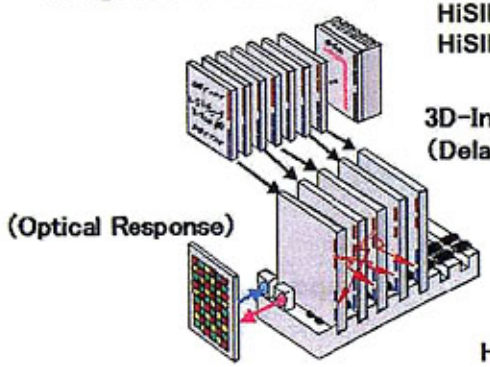
HiSIM	72
BSIM	400





3D Custom Stacked System: Requirements

Integration of Different Chips : HiSIM
HiSIM-RF
HiSIM-SOI



3D-Integration
(Delay Analysis, Noise Analysis)

(Optical Response)

HiSIM-Microwave

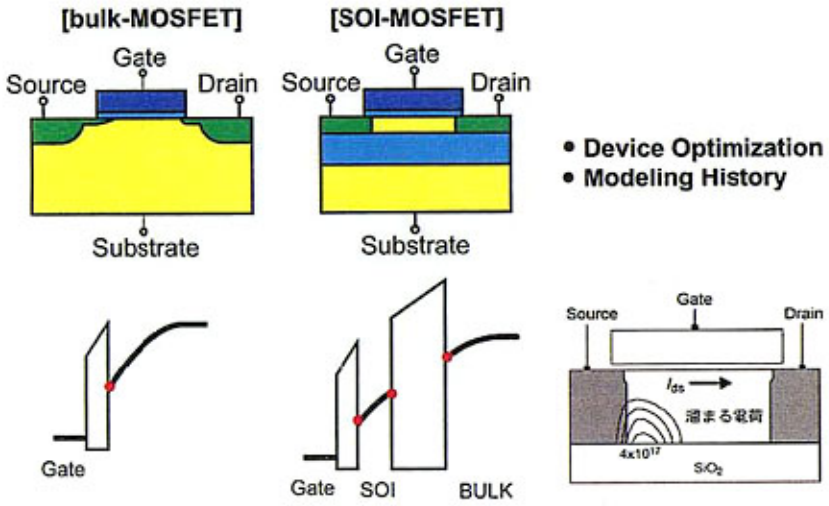
Concept of Model Development

- Refelecting Technology Features
- Capability for RF + Microwave Applications
- Capability for Optical Applications

HiSIM Generations

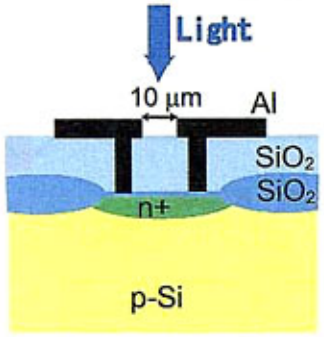
- HiSIM
- HiSIM-RF
- HiSIM-SOI
- HiSIM-Microwave

HiSIM-SOI: Device for Next Generation



- Device Optimization
- Modeling History

Photo Current (*I*)



p/n junction diode

Delay in Reponse