Industry-Academia Cooperation for Advanced Semiconductor Technology

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Horizontal deployment of IT companies accompanied with globalization of economy that happened in mid-eighties induced dramatic changes in the R&D environment in industry. Increasing competition in world-wide semiconductor market forced the industries to enhance the R&D speed and efficiency. This caused a shift of R&D activities from corporate research laboratories to business divisions and shrinkage of corporate labs. Simultaneously, companies enhanced strategic cooperation with universities and collaborated with business competitors through consortium.

SRC (1982) and SEMATECH (1987) are typical examples in U.S.A., while IMEC (1984) and JESSI/MEDEA (1988) in Europe. In addition, industry-academia-government cooperation was strongly motivated by Bayh-Dole Act in 1980 which allows industry and university to hold the IP rights even if the invention was done by government budget. This concept and the similar act were authorized also in Japan in 1999. In Japan STARC has promoted the industry-university collaboration program since 1995, and recently extended the activity to design technology development. Also, Selete was established in 1996. The Project ASUKA which is composed of Selete and STARC started from 2001. Also, MIRAI Project, industry-academia-government cooperation program, started in the same year. ASPLA was established in 2002. The consortia activities and industry-academia collaboration in Japan have been activated very recently, far behind U.S.A. and EU. Nevertheless, such activities will offer excellent opportunities for Japan to revitalize the semiconductor industries and strengthen the university research. This is because (1) the second wave in IT revolution, namely, the ubiquitous computing which needs new technologies and service infrastructures, is coming. Accumulated knowledge and technology in digital consumer, mobile systems etc. will help the competitiveness of Japanese industries in the future ubiquitous systems, devices and contents. And also (2) emerging walls to semiconductor technology prohibit simple extrapolation of existing knowledge for device scaling. New materials, new device structures and even new algorithm for circuit design are needed for breakthrough of the technology roadblocks, through extensive R&D efforts in respective industries and through cooperative R&D in the National Project (MIRAI) and the Consortia (ASUKA, HALCA, and ASPLA).

In order to guarantee the signal integrity of SOC (System on Chip), chip design, device manufacturing, packaging and inspection technologies must be totally optimized. This trend contradicts current fabless-foundry model particularly in 90nm node and beyond. The consortia activities and projects can offer the enabling technology to company, while each company can fuse it with its own core technology to develop highly market-competitive products, creating company differentiation in business. Thus strong management for external research including consortia projects and university activities is key for the success of the efficient R&D of each company. This will enhance industry-academia tie-up and corporate competitiveness.

In this presentation, a new model of industry-academia-government cooperation will be discussed by taking the example of MIRAI Project. Also, recent progress in key areas of semiconductor technology such as interconnect, circuit design, and new transistor structures will be reviewed based on challenges in MIRAI Project. Finally, an idea for the success of the COE Program at Hiroshima University will be proposed.

MIRAI

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Information Processing
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MIRAI

Outline

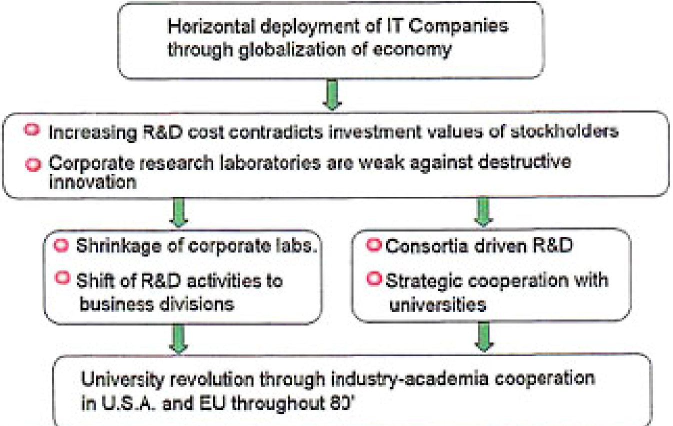
1. Why industry-academia cooperation?
2. Paradigm changes in semiconductor business
3. Challenges to new technology
   - MIRAI Project R&D
4. Summary
   - Issues expected to COE

MIRAI

1. Why industry-academia cooperation?

MIRAI

Dramatic Changes in R&D Environment in Industry and Academia



MIRAI Industry-Academia Partnership - U.S.A

1. **Semiconductor Research Corporation (SRC, 1982)**
   - Semiconductor technology research necessary in coming 3-5 years (from design to manufacture)
   - 40 universities participating (4.4 billion yen in fiscal 2001 from SIA)
2. **Focus Center Research Program (FCRP)**
   - Research and development of leading-edge semiconductor technology necessary in coming 5-10 years (period of 10 years)
   - Circuit design and testing (UCB), materials and devices (MIT), interconnect technology (GIT) and system / software (CMU)
   - An alliance of 4 main universities and more than 50 cooperating universities with researchers also dispatched from private companies to universities
   - Government 25%, industrial world 75%, 1 billion yen annually on one theme, 2005: 7.5 billion yen
3. **SEMATECH/ISMT (1987)**
   - Front-end and back-end technology development
   - 10 Member companies (AMD, Agere Systems, HP, Infineon, IBM, IntelMotorola, Philips, TSMC, TI)
   - Budget (FY2003/US$135M)

5

MIRAI Industry-Academia Partnership - Europe

1. IMEC (1984, R&D company invested in by the Belgian government)
   * Core staff are professors and graduate students of Leuven University
   * Infineon Technologies (Germany), Philips and ASML (Holland) have integrated their R&D functions with IMEC to develop next generation semiconductor technologies
   * Wide range of joint research with semiconductor equipment and chip manufacturers
2. LETI (French national research institute)
   * Combined with ST Microelectronics (France) to develop next generation semiconductor technologies
   * LETI staff and ST Microelectronics engineers share development functions with funding by the government
3. JESSI/MEDEA (1988)
   * 12 countries and 55 projects

6

MIRAI Impact of Bayh-Dole Act

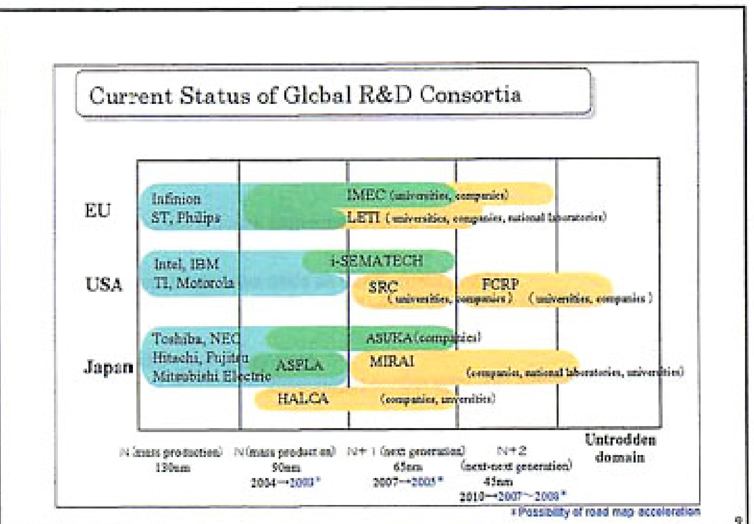
- Industry-academia-government cooperation was significantly motivated by Bayh-Dole Act in 1980
- The Act allows industry and university to hold the IP rights even if the invention was done by government budget.
- The similar act was authorized also in Japan in 1999

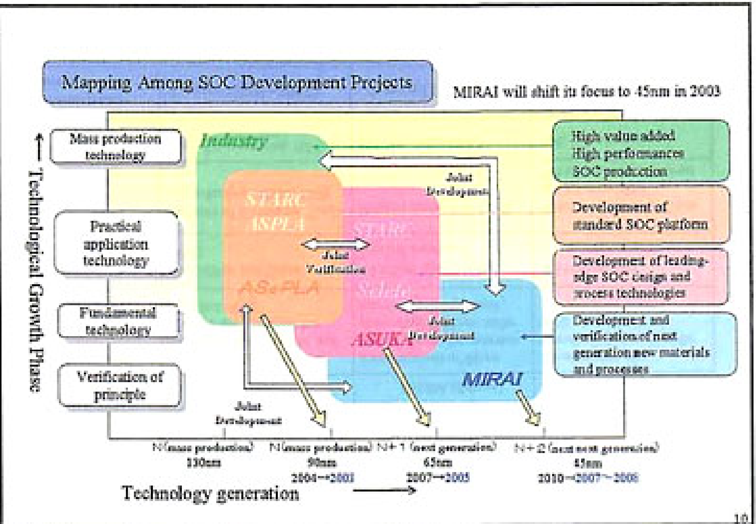
7

MIRAI Comparison of MIRAI, ASUKA(Selete) and HALCA Projects

	MIRAI	ASUKA(Selete)	HALCA
R&D themes	Development of advanced semiconductor material and process technologies for 65-45nm node	Establishment of 65nm generation device process technology (300mm wafer compatible integration)	Development of a manufacturing system for SOC
Budget	4.56 billion yen (fiscal 2002)	14 billion yen/year (period average)	3.11 billion yen
Supporting institution	Ministry of Economy, Trade and Industry/NEDO 100%	Private company 100%	Ministry of Economy, Trade and Industry/NEDO 50% or less is supplemental
Personnel	150 (25 companies, AIST, 20 univ labs)	250 (14 companies)	35 (14 companies)
Development period	7 years (2001–2007)	5 years (2001–2005)	3 years (2001–2003)

8





Industry, Academia and Government Tie-ups and Corporate Competition

1. Project results are shared by the participating companies (IP rights of the inventor are protected).
2. Cooperative R&D of difficult and risky technology which is important for the future.
3. Each company obtains enabling technology as a result.
4. This technology is fused with the company's own technology. The capability of developing highly market-competitive products in a short time creates company differentiation and competitiveness.
5. Functioning of this differentiation requires the clear core-competence management in company.

11

2. Paradigm changes in semiconductor business

12

World Wide Semiconductor Market in 2010

- System LSI 720 B US$
- Equipment 100 B US$

- Impact to Nation's Economy
- Consortia-driven R&D and Government Commitment
- Global Competition and Collaboration

  (Any company can not cover the whole range of technology development)

13

Limit of the Fabless-Foundry Model

- In the 130nm node, chip design and fabrication technology became more complex because of the introduction of new materials (low-k/Cu interconnect) and sophistication of lithography (OPC).
- In order to guarantee the signal integrity and minimizing defect generation in fabricated chips, total solutions of problems encompassing design, manufacturing, packaging, and inspection hierarchies are needed. Thus the horizontal specialization model lost its potential to handle these issues.
- In the future 65nm and 45nm nodes, the introduction of new materials and processes will proceed even further. Thus design and manufacturing without technology know-how accumulated by integrated device manufacturers (IDM) and R&D results by consortia activities will become even more difficult.
- Foundry service can work only when the full set of technology files is provided to users (fabless). Otherwise, fabricated chip yield will be poor.

14

Can Integrated Device Manufacturers Effectively Grab This Opportunity ?

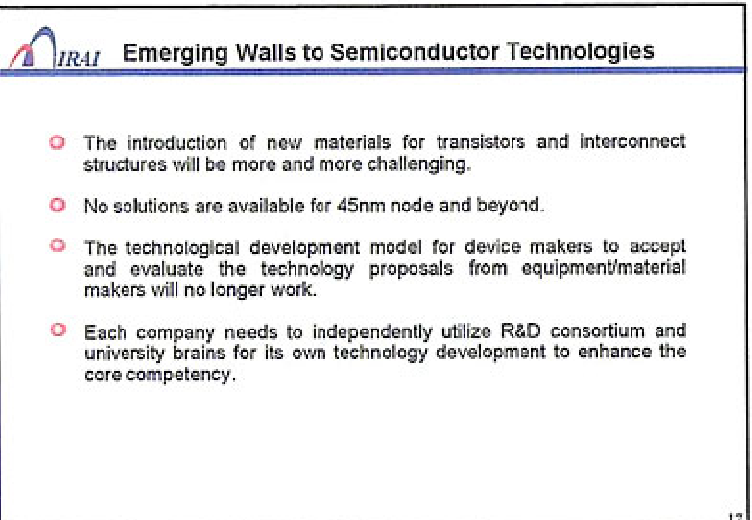
- Countermeasures
  1. ASPLA provides a standard 90nm process. Library and CAD tools are offered to users in cooperation with STARC. The users can access to an SOC platform that can provide verified IPs (ASPLA scheme).
  2. ASPLA attracts a leading-edge fabless from overseas by offering the advanced technical support and leading-edge technology
- Challenges
  1. Manufacturing by a leading-edge fab that incorporates results of R&D from consortia and IDM.
  2. Realization of ultra QTAT and an advanced production technology with a suitable cost
  3. High quality services matching market needs

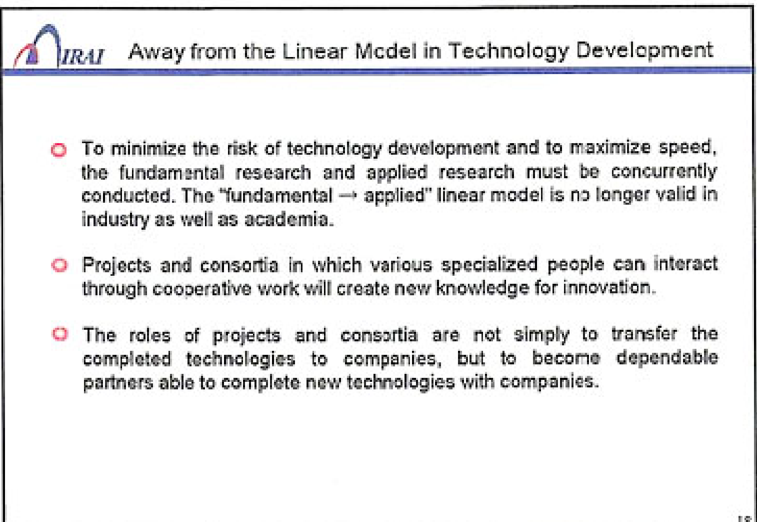
15

Shift from the PC Era to the Ubiquitous Computing Era

- More than 50% of Internet access in 2005 will be by non-PCs
- Ultra compact, ultra low power and low cost computers connected via networks will be embedded in various items surrounding us.
- Clothing, accessories, homes, offices and other overall environments will possess advanced information processing capabilities.
- Companies which have created ubiquitous computing technology and service infrastructures will obtain great profit.
- Realization of Japan-originating standards, competitive systems and services, and business models in ubiquitous society can be expected.

16





MIRAI Project (FY2001-2007)

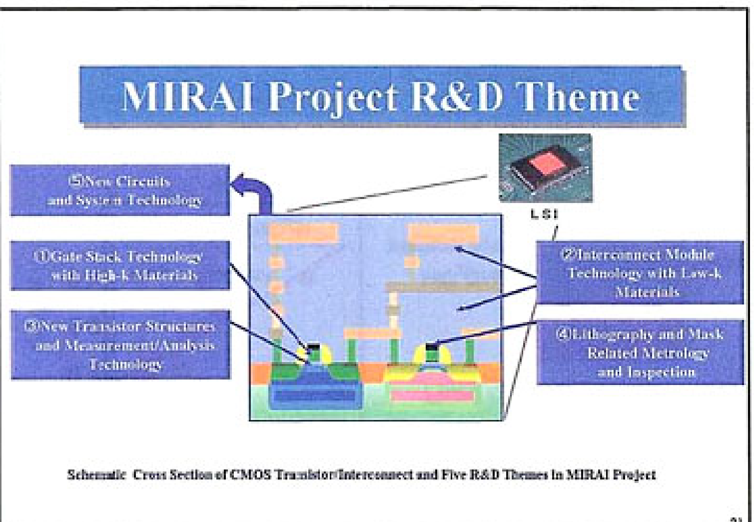
Purpose:Development of advanced semiconductor technology for 65 to 45nm node for establishing a solid basis of the industry competitiveness.

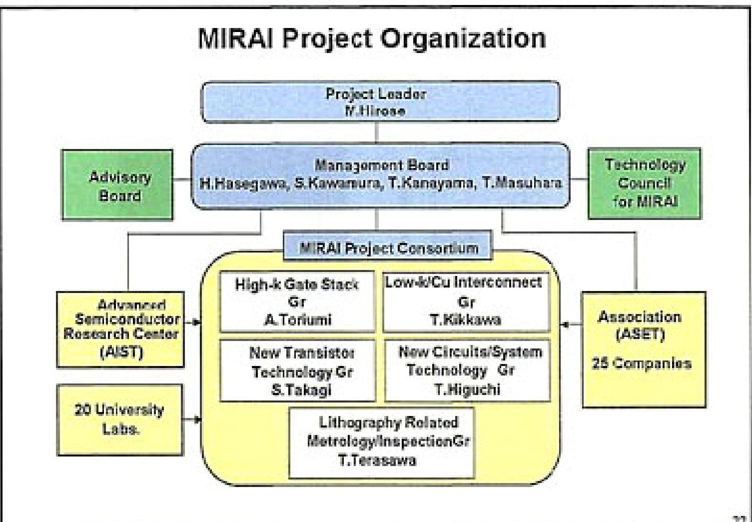
Mission:To achieve the world-top R&D capabilities by FY 2003 through timely achieving major technological breakthroughs,thereby contributing to the ongoing growth of the semiconductor industry.

Philosophy:Fusion of various expertise and scientific approach are emphasized in order to take high risk in technology development. Moreover, MIRAI offers a place for developing superior researchers able to achieve world-class R&D.

Organization:The MIRAI project is conducted by a virtual organization of 74 researchers from 25 companies and 62 researchers from AIST/ASRC in cooperation with 20 university laboratories. The main site for research is Tsukuba AIST Super-Clean Room.

20



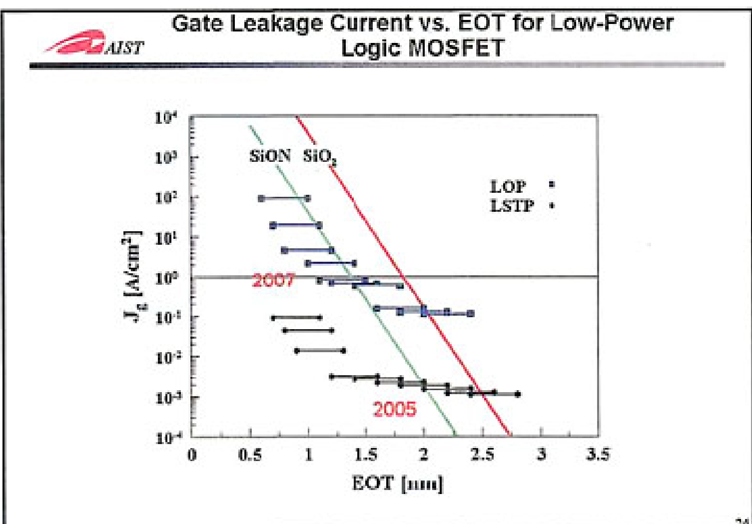


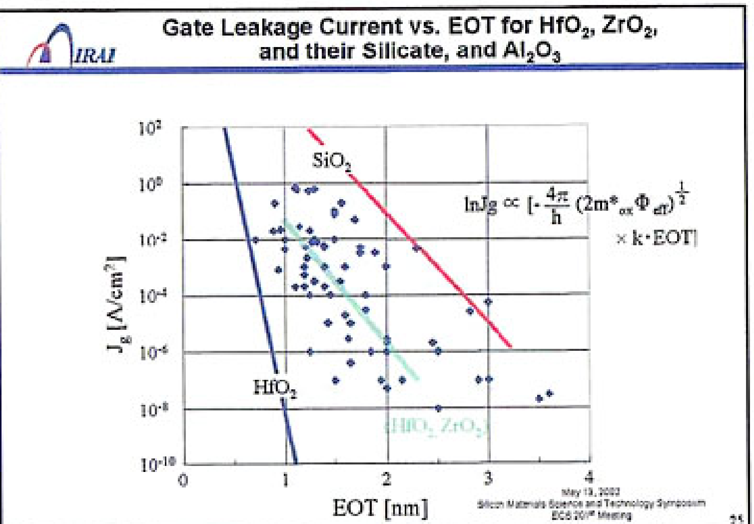
High-k Gate Stack Gr

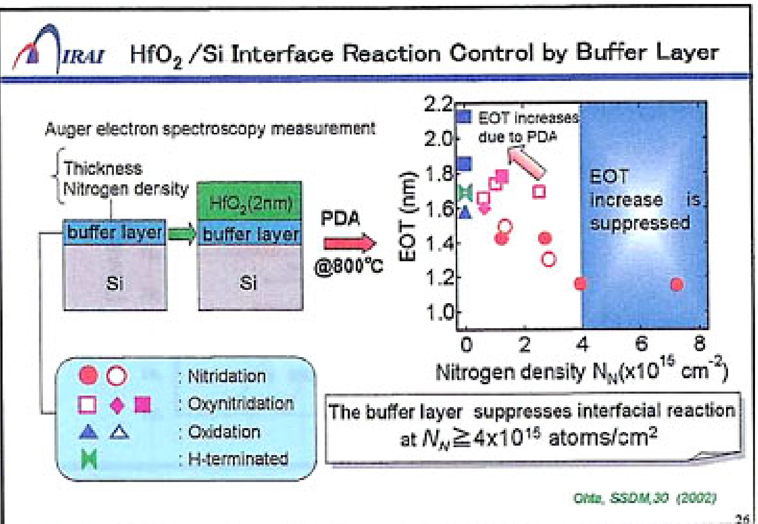
Key Challenges

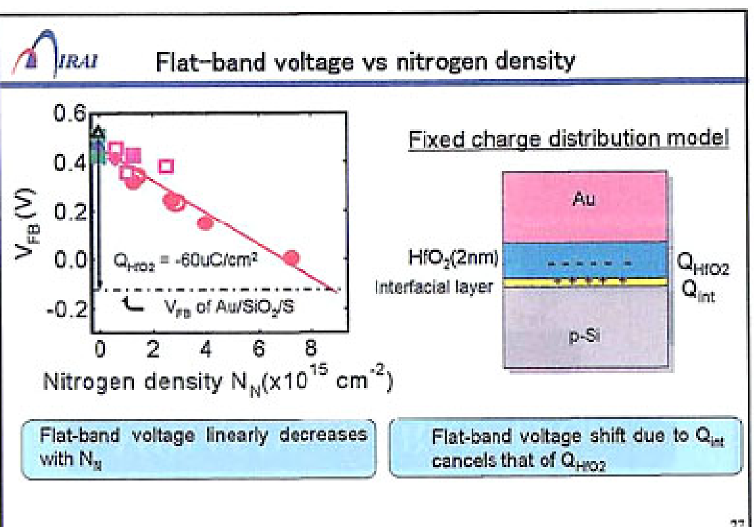
1. Materials selections (high-k, gate metal) with atomic scale control of the interfaces
2. Precursors and tool development for high-k CVD
3. Systematic understanding of candidate materials, interface reactions, and deposition chemistry
4. Metrology to quantify energy band diagram, electronic density of defect states (bulk and interface), localized strain, and EOT
5. Process integration with keeping mobility high
6. Modeling of tunnel leakage current and charge trapping
7. Dielectric reliability model

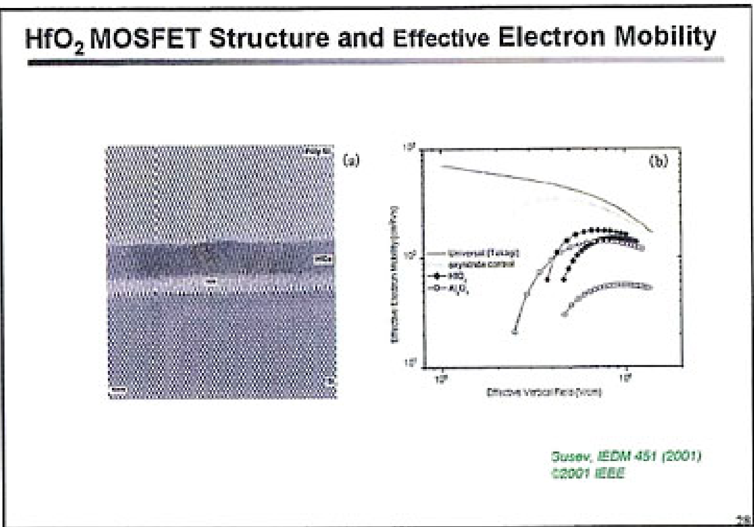
23




MIRAI
Gate Leakage Current vs. EOT for HfO2, ZrO2, and their Silicate, and Al2O3
SiO2
HfO2
(HfO2, ZrO2)
lnJg ∝ [- 4π/h (2m*ox Φeff)^1/2 × k·EOT]
Jg [A/cm2]
EOT [nm]
May 13, 2002
Silicon Materials Science and Technology Symposium
25


MIRAI
HfO2 /Si Interface Reaction Control by Buffer Layer
Auger electron spectroscopy measurement
Thickness
Nitrogen density
buffer layer
Si
HfO2(2nm)
buffer layer
Si
PDA
@800℃
: Nitridation
: Oxynitridation
: Oxidation
: H-terminated
EOT increases due to PDA
EOT increase is suppressed
EOT (nm)
Nitrogen density NN(x10^15 cm^-2)
The buffer layer suppresses interfacial reaction at NN≧4x10^15 atoms/cm2
Ohta, SSDM,30 (2002)
26


MIRAI
Flat-band voltage vs nitrogen density
VFB (V)
QHfO2 = -60uC/cm2
VFB of Au/SiO2/S
Nitrogen density NN(x10^15 cm^-2)
Fixed charge distribution model
Au
HfO2(2nm)
Interfacial layer
p-Si
QHfO2
Qint
Flat-band voltage linearly decreases with NN
Flat-band voltage shift due to Qint cancels that of QHfO2
27


HfO2 MOSFET Structure and Effective Electron Mobility
(a)
(b)
Gusev, IEDM 451 (2001)
©2001 IEEE
28

Layer-by-Layer Deposition & Annealing

Depo. 1st layer → Annealing Out gas → Depo. 2nd layer → Annealing Out gas → Multilayers

Purpose

Impurity removal

Interface control

Features

- In-situ D&A process
  Gate/I.L./High-k/I.L./Si
- Interface control technique
  Oxidation/nitridation
- Impurity removal technique

Schematic diagram of LL-D&A process

Interface control chamber

Si wafer

RTA chamber

ALD chamber

29

Goal in the First Phase (2001-2003)

1. POC machine for depositing high-k gate dielectrics will be developed.
2. Evaluation of 100nm CMOS with EOT=1.0nm will be completed.
3. Transistor model including mobility and reliability issues will be developed.

30

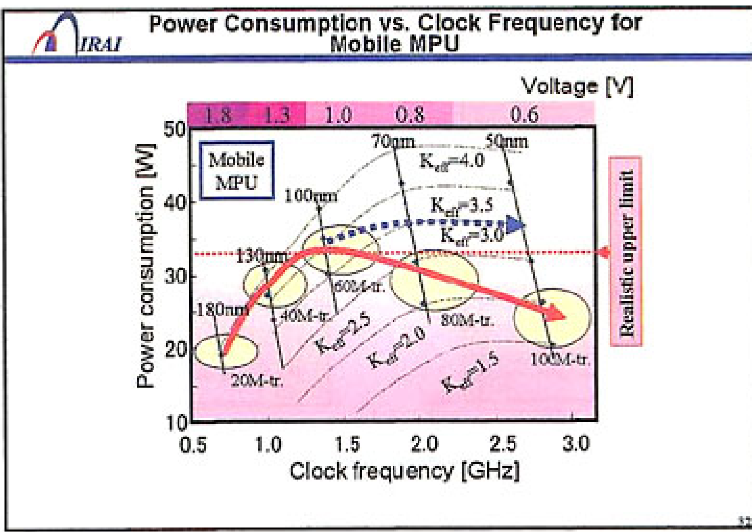
Low-k/Cu Interconnect Gr

Key Challenges

1. Inorganic and organic porous materials development by controlling pore size distribution, pore structure and hydrophobicity
2. Precursors and tool development
3. Metrology standards for determining porous structure, chemical bonding states, local dielectric constant, thermal conductivity, Cu^{+} drift rate, and nanoscale mechanical properties
4. Process integration with minimum steps
5. Ultra-high speed signal transmission integrity
6. Interconnect reliability model

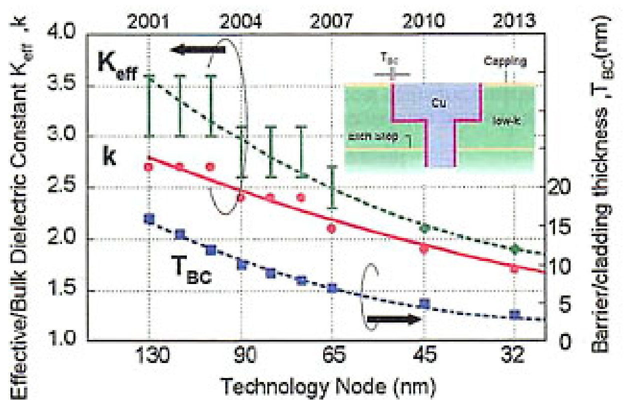
31

Power Consumption vs. Clock Frequency for Mobile MPU



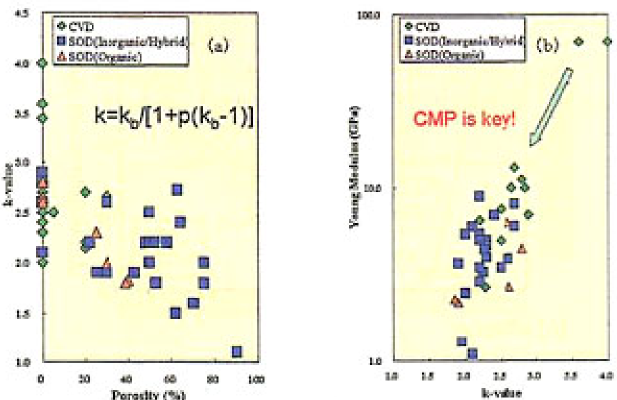
32

Materials Requirements for Interconnects



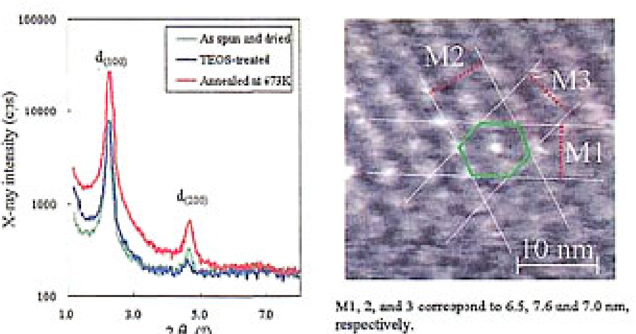
33

Dielectric Properties of Porous Low-k Materials



34

IRAI Thermally-stable Periodic Nanoporous Silica

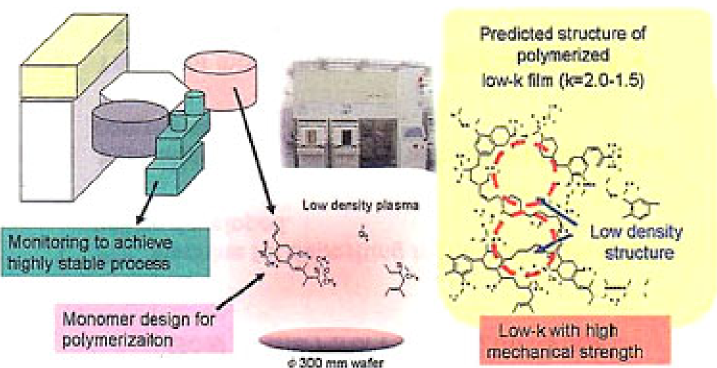


M1, 2, and 3 correspond to 6.5, 7.6 and 7.0 nm, respectively.

Oku, MRS Proc. 716 B12.6 (2002)

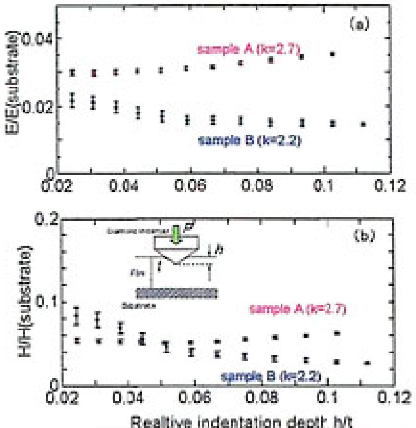
35

IRAI Low−k deposition by plasma polymerization

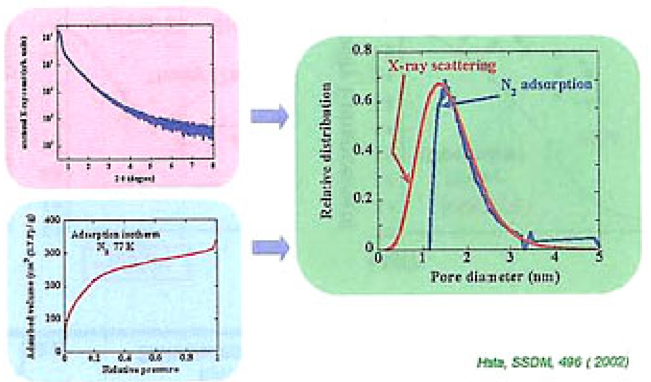


36

Young Modulus and Hardness Measured by Nanoindentation



Pore-size distributions from X-ray scattering and gas adsorption



Hata, SSDM, 496 (2002)

Voiding in Ultra Porous Low-k Materials Proposed Mechanism, Detection and Possible Solutions

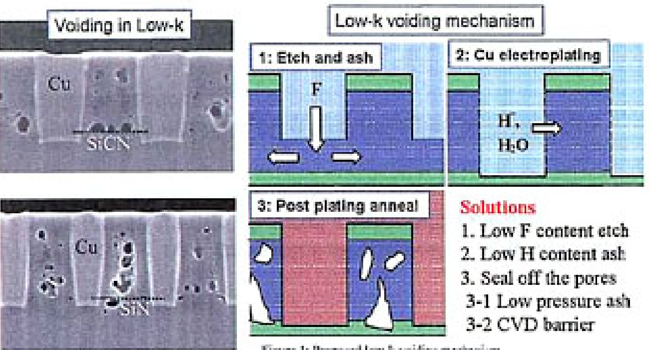


Figure 2: Voiding in MSQ film

Figure 4: Proposed low-k voiding mechanism

Jacobs, Proc. IITC, 236 (2002)

Goal in the First Phase (2001-2003)

1. Deposition tools for ultra low-k dielectrics will be developed.
2. Ultra low-k materials with sufficient mechanical strength will be developed.
3. Integration issues (CMP for porous materials, wet chemicals damage, etch/ash damage, etc.) will be systematically understood.
4. Dual damascine Cu/low-k interconnect module technology will be demonstrated by using 300mm wafer process tools.

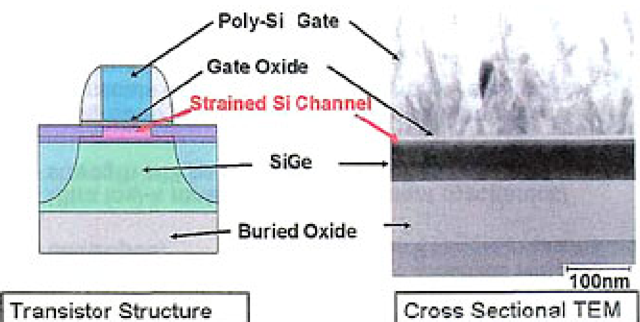
New Transistor Technology Gr

Key Challenges

1. Developing new transistor structures by implementing new materials and channel engineering methodology such as strained-SOI
2. Developing novel doping technologies to form ultra shallow junctions
3. Designing new metrology tools such as impurity profiles and local stress in transistor channels with a high spatial resolution better than 10nm

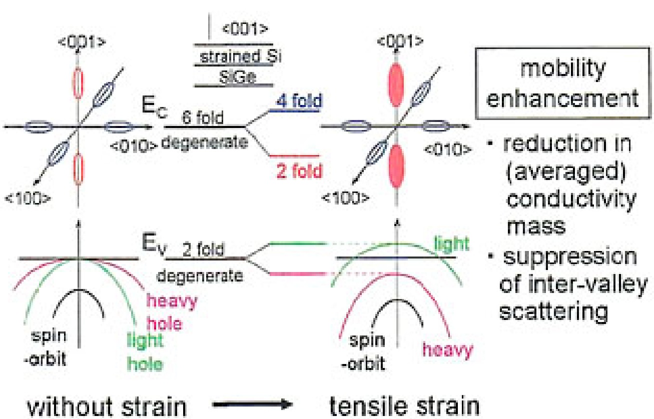
41

Strained SOI MOSFET



42

Modulation of Band Structure due to Strain

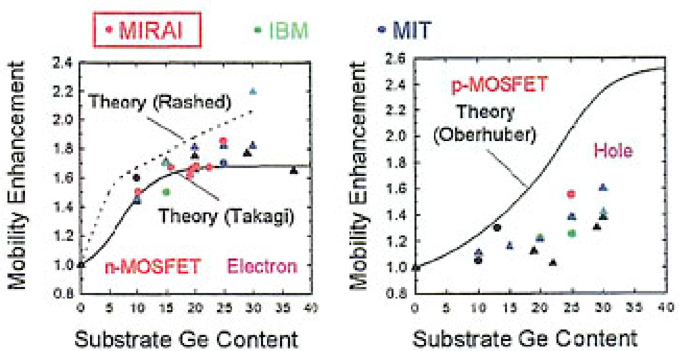


mobility enhancement

- reduction in (averaged) conductivity mass
- suppression of inter-valley scattering

43

Electron and Hole Mobility Enhancement in Strained-Si MOSFET



44

MIRAI Mobility Enhancement in Strained-Si MOSFET

Thickness: total/strained Si = 375nm/25nm(PD), 60nm/7nm(FD)

- Maximum Mobility Enhancement against Universal Mobility

  Electron: 85%, Hole: 53%

Mizuno, VLSI Symp, 106 (2002)

45

MIRAI First Operation of Strained-Si CMOS Ring Oscillator

- First Demonstration of CMOS Ring Oscillator
- Speed Improvement against Conventional SOI CMOS

  70% higher @ V_{dd} = 1.5V, 30% higher @ V_{dd} = 2.5V

Mizuno, VLSI Symp, 106 (2002)

46

Double-gate MOSFET (ITRS 2001)

(a) Planar — Wong et al, IEDM 1997; Lee et al, IEDM 1999

(b) Vertical pillar — Hergenrother et al, IEDM 1999

(c) Vertical — Hisamoto et al, IEDM 1998, Huang et al, IEDM 1999

47

AIST Strained-Si-on-Insulator

- Low defect Strained SOI wafers
  - ⇒ not ready to supply but possible
- Mobility enhancement of holes insufficient
  - ⇒ Ge profile control in channel
- Target system using Strained SOI CMOS
  - ⇒ emerging

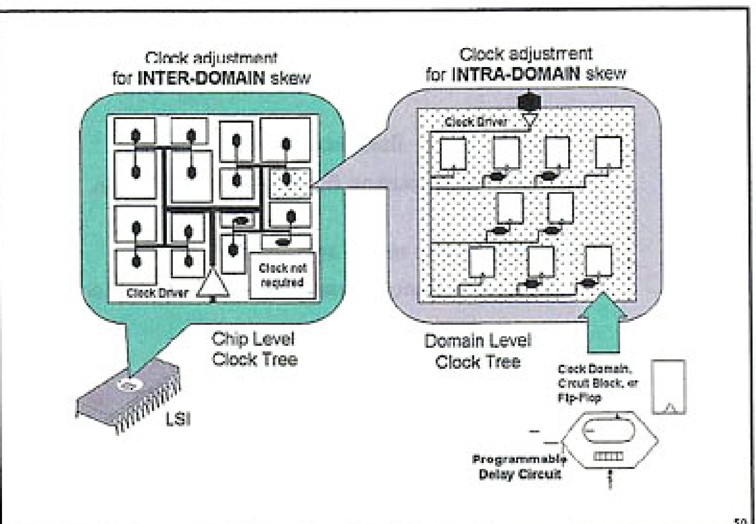
48

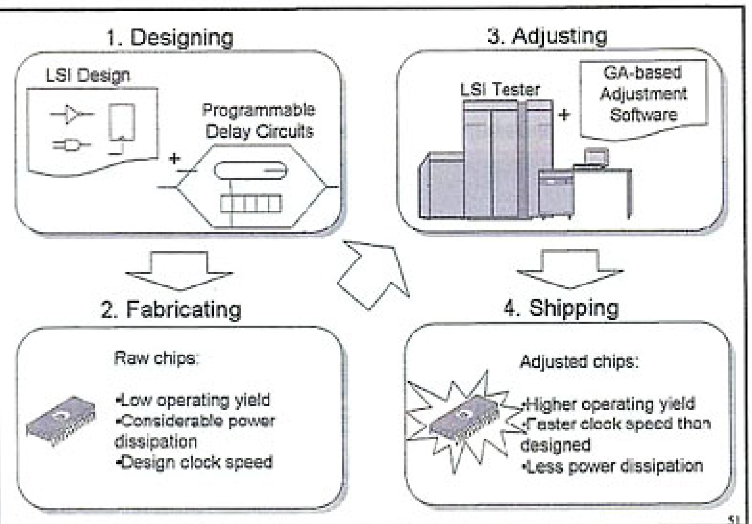
New Circuits/System Technology Gr

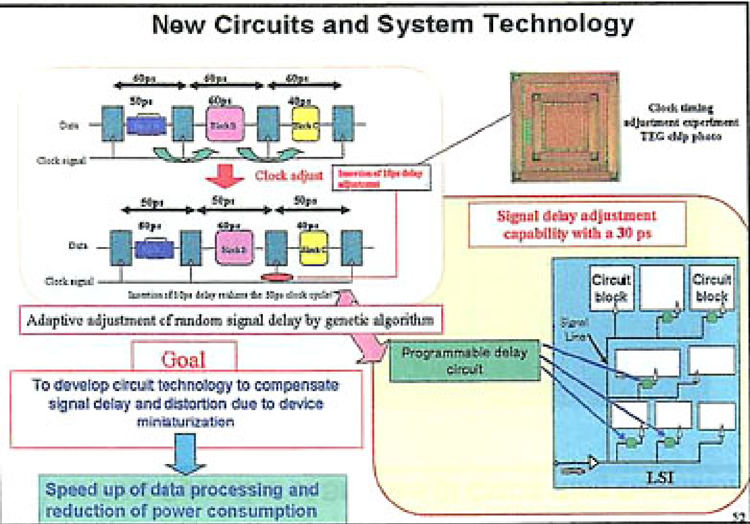
Key Challenges

1. Developing a new circuit technology to solve the problem of signal clock skew
2. Improving integrity in high-speed data transfer
3. Artificial Intelligence(AI)-calibrated analog LSI design

49



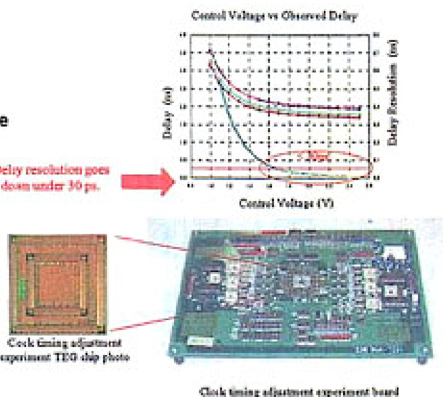




Clock timing adjustment: results

- Small sizing of delay unit
  - Minimum delay: 30ps
  - 10 gate size
  - 90% reduction of the space
- Verified by TEG development
  - April 2002 completed
  - patent

Delay resolution goes down under 30 ps.

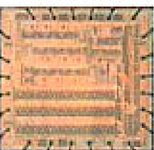


Clock timing adjustment experiment TEG chip photo

Clock timing adjustment experiment board

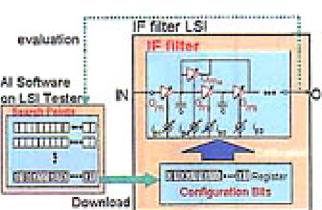
53

Adaptive Analog Circuit: IF Filter LSI for Mobile Phones

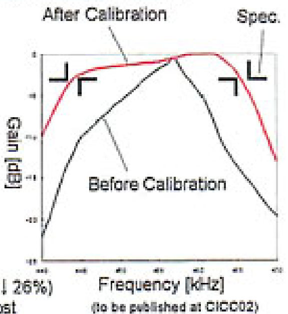


The LSI has been mass-produced for mobile phones since autumn 2001.

Calibration of 39 parameters in IF filter LSI using an **Artificial Intelligence (AI) technique**



Results
- High Yield (97%)
- Compact (↓51%)
- Low power dissipation(↓26%)
- Reduction of Design Cost



(to be published at CICC02)

54

Issues Expected to COE

1. Global competitiveness in the focused area of research and potential for systematic education.
2. Strong management for cooperative research among specialists from different fields.
3. Bilateral devloyment of fundamental research and applied research in the COE (no longer "linear model").
4. Enhancement of communication channels to industrial partners for better agreement on bylaws to handle and manage IPs, concurrent technology transfer and exchange of knowledge and human resources.

55

Issues Expected to COE

1. University was the place where researchers were personally driven by curiosity, while now university becomes the place where researchers are encouraged to interact more with the other faculties and external partners.
   COE is a leader of this movement to change the function of university.
2. COE offers the platform where specialists from different fields cooperate for the common mission.
3. COE needs to solve the paradox that academic freedom and capiital efficiency as defined by the productivity of researchers measured by external evaluation scale must be simultaneously realized.

56