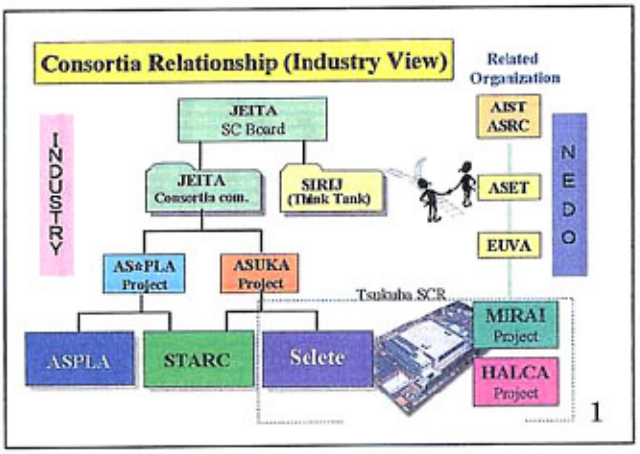
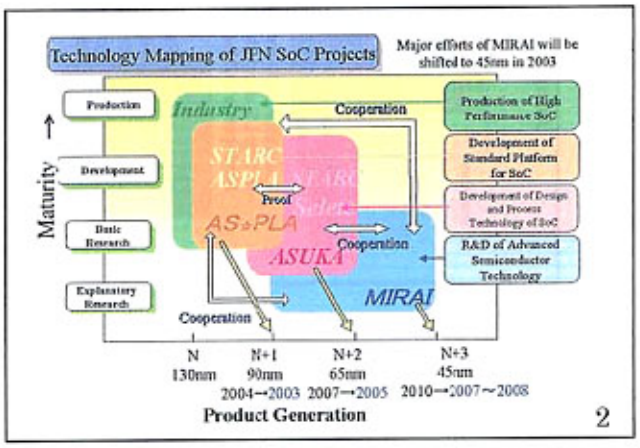
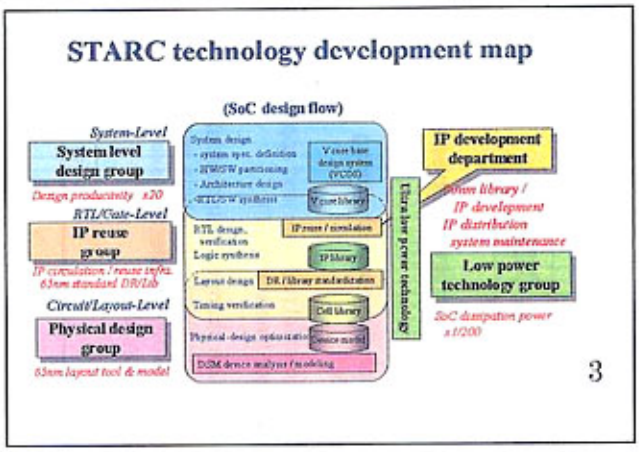
Strategic Directions of Semiconductor Consortia and Expectation to COE Program

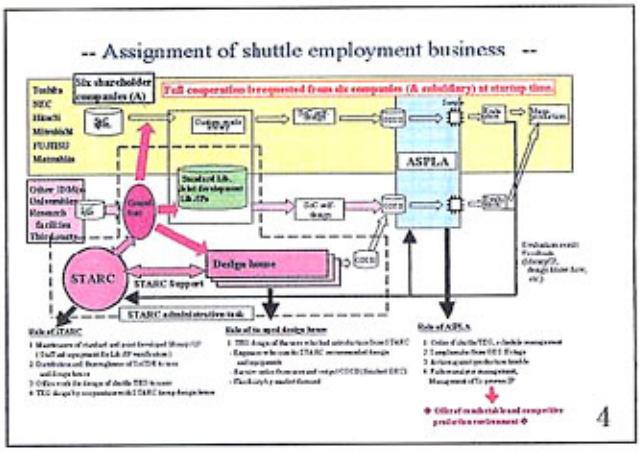
Semiconductor Technology Academic Research Center (STARC)
President & CEO Toyoki Takemoto

Semiconductor products have become a staple of industry, having incorporated into not only information and communication devices but a wide range of other industrial devices as well.
On the other hands, competition becomes more and more severe, so semiconductor companies have to increase the speed of selection and focus, and promote rapid standardization as an industry. Therefore, a lot of Japanese consortia are founded to contribute to help making standardization and decrease the duplicated investment.
First of all, I explain the activities of Japanese consortia including STARC and next, I discuss examples of the cooperation of industry and academia. Lastly, I touch upon the expectation to the 21st century COE.







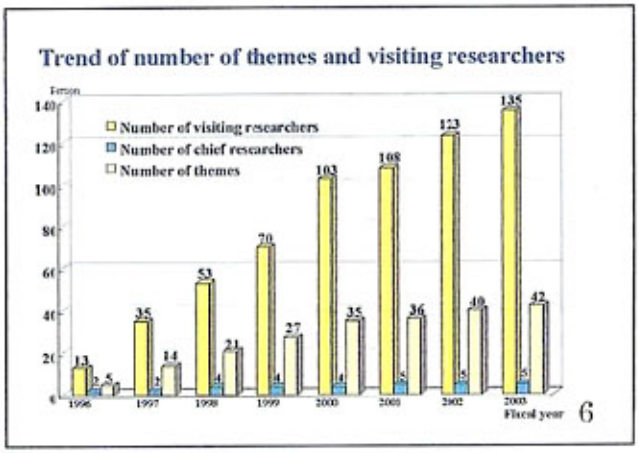


Feature of STARC Design Course

- Reform lecture text
  - Establish embedded SW design course, create three courses text in 2002.
- Develop three training course
  - Training of simple AV playback system in DVD system.
  - LSI design course .. Done
    Embedded SW design / System design course .. Done
- Start advanced lecture course
  - IP reuse design (volume on SoLID) .. done

Training equipments of DVD system and training scenery in LSI design course

5



STARC Semiconductor Technology Academic Research Center

Strategic Directions of Semiconductor Consortia and Expectation to COE Program

Toyoki Takemoto
President & CEO
STARC
March 17, 2003

STARC Semiconductor Technology Academic Research Center

Outline

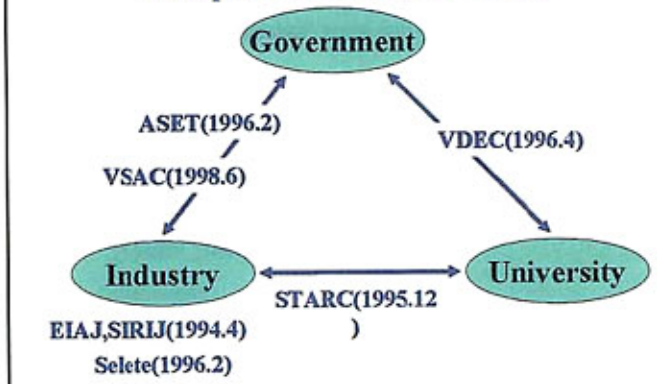
1. Semiconductor Consortia
2. Technology Trend
3. STARC Activities
4. Actibity-1
   Strengthening of SoC Design Power
5. Activity-2
   Research Support and Activation in Universities
6. Expectation to the "COE"

STARC Semiconductor Technology Academic Research Center

1. Semiconductor Consortia
2. Technology Trend
3. STARC Activities
4. Actibity-1
   Strengthening of SoC Design Power
5. Activity-2
   Research Support and Activation in Universities
6. Expectation to the "COE"

STARC Semiconductor Technology Academic Research Center

Industry, university and government in Japan semiconductor world



STARC Semiconductor Technology Academic Research Center

Semiconductor Industry Players

Industry

Chip Makers

NEC, Toshiba, Hitachi, Fujitsu, Mitsubishi, Matsushita, Sony, Sharp, Sanyo, Rohm, Oki, (Elpida, Trecenti, RENESAS)...

Equipment Suppliers

TEL, Nikon, Canon, Accretech, DNS, Advantest, ULVAC,...

Material/Mask Suppliers

TOK, JSR, Shinetsu, MS Silicon, Hoya, DNP,Toppan....

Trade Associations

JEITA: Chip Makers, Electronics Equipment and Component Manufacturers

SEAJ: Equipment and Material Suppliers

STARC Semiconductor Technology Academic Research Center

Academia / National Labs

Universities

Tohoku, Tokyo, Osaka, Hiroshima, ...

National Labs (AIST)

Advanced Semiconductor Research Center (ASRC)

Nanoelectronics Research Institute (NeRI) ....

Government

Ministry of Economics, Trade and Industry (METI)

New Energy and Industrial Technology Development Organization (NEDO)

STARC Semiconductor Technology Academic Research Center

Semiconductor R&D Consortia in Japan

STARC: Semiconductor Technology Academic Research Center

Selete: Semiconductor Leading Edge Technology Inc.

ASET: Association of Super-Advanced Electronic Technologies

MIRAI: Millennium Research for Advanced Information Technology (ASRC + ASET)

ASPLA: Advanced SOC Platform Corporation

EUVA: Extreme Ultraviolet Lithography System Development Association

STARC Semiconductor Technology Academic Research Center

Major R&D Programs

ASUKA	2001-2005	Selete STARC
MIRAI	2001-2007	MIRAI
HALCA	2001-2003	ASET
Electronic SI	1999-2003	
PFC Alternative	1999-2003	
EUV	1998-2006	EUVA ASET
SOC Platform	2002-2004	ASPLA STARC

STARC Semiconductor Technology Academic Research Center

Selete

- Semiconductor Leading Edge Technology Inc.
- Founded Feb. 1996
- Programs
  - Advanced Lithography (VUV, Mask, EPL)
  - Advanced Process (FEP,BEP)
  - TCAD
  - ASUKA Research Line
- Members
  - Shareholders: Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC,Oki, Rohm, Sanyo, Sharp, Sony, Toshiba
  - Contractors: Shareholders, Seiko Epson, Samsung

STARC Semiconductor Technology Academic Research Center

ASET

- Association of Super-Advanced Electronics Technologies
- Founded Feb. 1996
- Programs
  - PFC Substitution Process
  - Electronic System Integration
  - MIRAI (Joint project with ASRC)
  - HALCA (Highly Agile Line Concept Advancement)
- Members
  - Chip makers, Suppliers, Materials, Users…47
  - Foreign Members: Intel, Samsung, (ASM Japan)

STARC Semiconductor Technology Academic Research Center

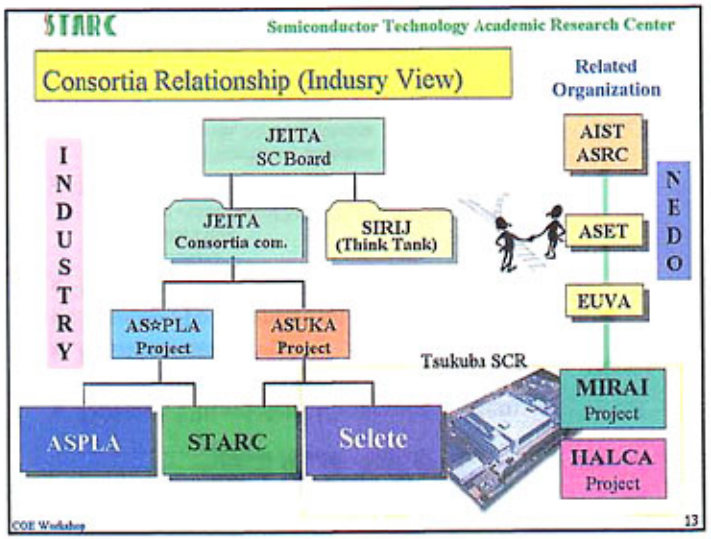
EUVA

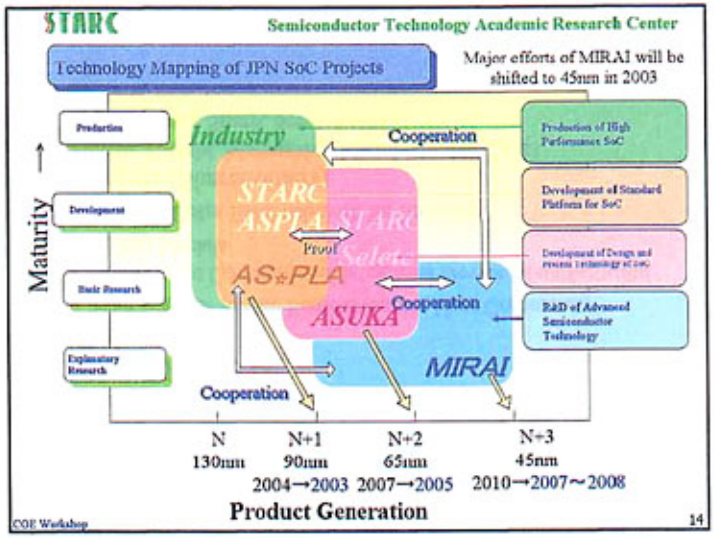
- Extreme Ultraviolet Lithography System Development Association
- Founded June, 2002
- Mission :To complete an EUV prototype machine
- Programs
  - EUV light source
  - EUV exposure tool
  - Design and evaluation of EUV lithography system
- Members
  - Canon, Nikon, Gigaphoton, Komatsu, Ushio, Fujitsu, Hitachi, Mitsubishi, NEC Electronics, Toshiba

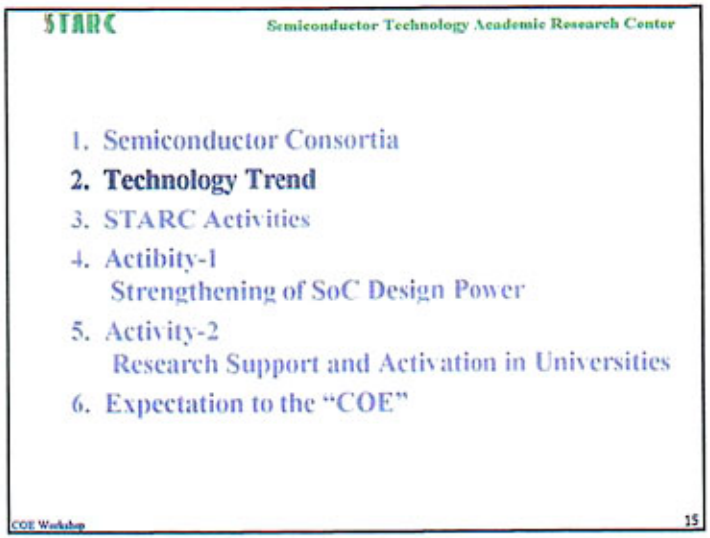
STARC Semiconductor Technology Academic Research Center

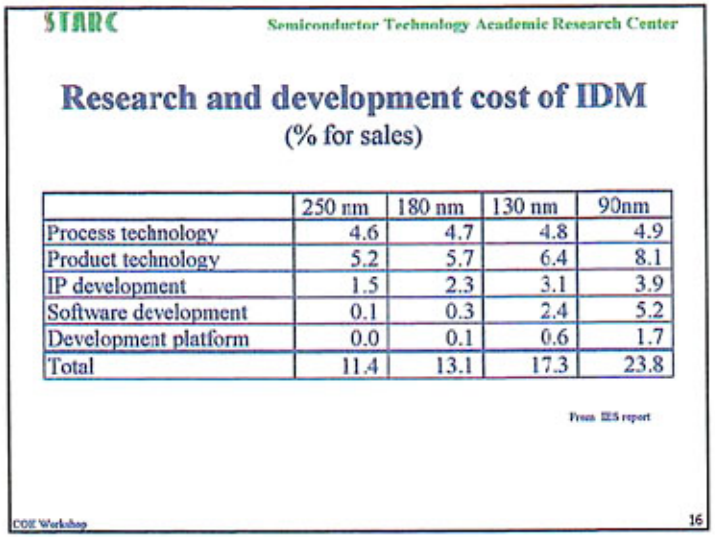
ASPLA

- Advanced SoC Platform Corporation
- Founded July 2002
- Mission
  - Best Practice for the Semiconductor User Community
  - Solution for Conventional Integrated Device Manufacturing (IDM) Models
  - SOC Platform Establishment for Industry
- Members (Shareholders)
  - Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC,Oki, Rohm, Sanyo, Sharp, Sony, Toshiba









	250 nm	180 nm	130 nm	90nm
Process technology	4.6	4.7	4.8	4.9
Product technology	5.2	5.7	6.4	8.1
IP development	1.5	2.3	3.1	3.9
Software development	0.1	0.3	2.4	5.2
Development platform	0.0	0.1	0.6	1.7
Total	11.4	13.1	17.3	23.8

STARC Semiconductor Technology Academic Research Center

Market trend of ICT era

Variation in semiconductor industry

System becomes still more complicated and is determined by the following requests.

* Portability and downsizing
  - Low power (battery drive)
  - Wireless communication
  - Wideband
* Connectability with Internet (WAP/i-MODE)
* Multi-function and high reliability
* Price fixing of wide range based on various requests

STARC Semiconductor Technology Academic Research Center

Semiconductor technology load map

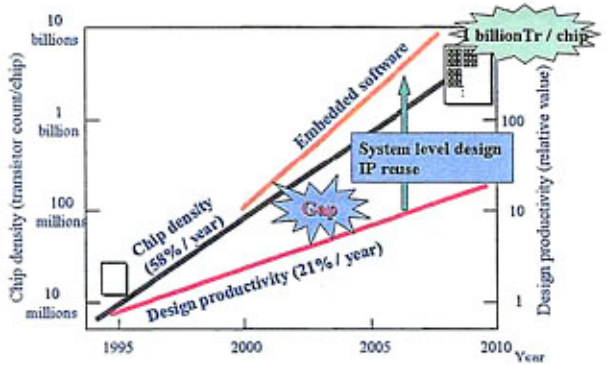
(2001 ITRS-Int'l Technology Roadmap for Semiconductors)

Item	Unit	2001	2004	2007	2010	2013	2016
DRAM half pitch	nm	130	90	65	[illegible]	[illegible]	[illegible]
MPU half pitch	nm	150	90	65	[illegible]	[illegible]	[illegible]
Si wafer diameter	mm	300	300	300	300	450	[illegible]
Gate insulator thickness	nm	1.5-1.6	0.9-1.4	[illegible]	[illegible]	[illegible]	[illegible]
Supply voltage	V	1.2-1.1	1.2-1.0	1.1-0.7	1.0-0.6	0.9-0.5	0.9-0.4
Dielectric constant	k	3.0-3.6	2.6-3.1	[illegible]	[illegible]	[illegible]	[illegible]
Wiring levels		7	8	9	9-10	9-10	10
DRAM development (mass production)	bit	2G(512M)	4G(1G)	16G(4G)	32G(8G)	64G(32G)	64G(64G)
No. of Trs. (SoC)	M Tr.	193	386	773	1546	3092	6184
Tr. Density (SoC)	M Tr./cm2	38.6	77.2	154.3	309	617	1235
Clock frequency	GHz	1.7	4.0	6.7	11.5	19.3	28.8
Power (LP-HP)	W kTr/ mat*mtch	2.4-130	1.2-160	3.5-190	3.0-218	3.0-251	3.0-288
Design labor (SoC)		10	22	[illegible]	[illegible]	[illegible]	[illegible]

Solutions are Known. Solutions are NOT Known.

STARC Semiconductor Technology Academic Research Center

Design crisis



(Source: SEMATECH)

STARC Semiconductor Technology Academic Research Center

1. Semiconductor Consortia
2. Technology Trend
3. **STARC Activities**
4. Actibity-1
   Strengthening of SoC Design Power
5. Activity-2
   Research Support and Activation in Universities
6. Expectation to the "COE"

Business of STARC

1. Strengthening of SoC Design Power!

Purpose: Improvement of SoC design productivity

(1) SoC design environmental development
- system level design automation
- physical design optimization

(2) IP (Intellectual property)
- IP reuse / circulation
- low power IP

(3) Acceleration of 90nm library and IP development
- Cooperation with ASPLA

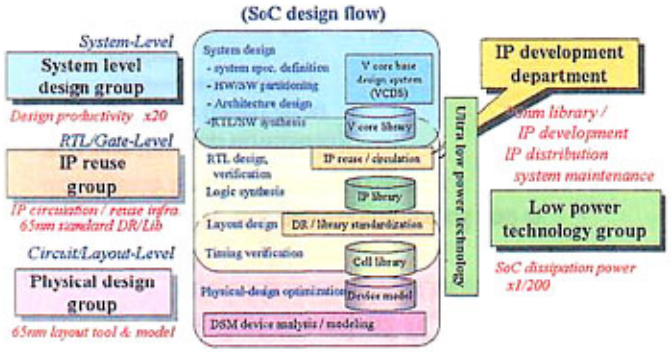
2. Research Support and Activation in Universities

(1) STARC / universities joint research

(2) SoC designer education (students & engineers)

1. Semiconductor Consortia
2. Technology Trend
3. STARC Activities
4. **Actibity-1**
   Strengthening of SoC Design Power
5. Activity-2
   Research Support and Activation in Universities
6. Expectation to the "COE"

STARC technology development map



Missions of Physical Design Group

- Development of optimization technology of circuit and layout design accompanying scaling
  - Verification of physical and electromagnetic phenomena by using TEG
    - Wiring delay, cross talk, inductance, fluctuation
    - Substrate noise, reliability (electro-migration)
  - High precision simulation model of scaled elements
    - LCR extraction, analysis, HiSIM model
  - Introduction and benchmark to layout EDA tools

STARC Semiconductor Technology Academic Research Center

Physical level optimal design environment

Effect of device scaling

- Increase of wiring delay
- Increase of cross talk noise
- Increase of fluctuation

- Timing Closure is difficult.
- Performance cannot be taken out with conventional margin design.

Physical design becomes a neck of SoC design.

Innovation of physical level optimal design environment
TEG technologies: Fact Finding on Chip & Modeling

Expansion of TEG technology

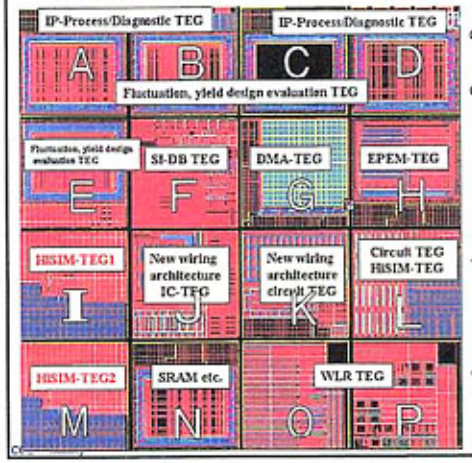
TEG technology [Physical] - delay - noise - PW - fluctuation

[Cell] - Abstraction to cell model - Inter-connect model abstraction (Equivalent Circuit)

[Macro Chip] - Abstraction to macro model - LSI design method to chip mounting

STARC Semiconductor Technology Academic Research Center

Outline of STARC-TEG02



O Chip size
20.5X20.5 mm2 (5X5mm2 x16)

O DRM
90 nm ASPLA-DRM

O Contents
- process, device evaluation TEG
  fluctuation and yield design
- signal integrity design TEG
  HiSIM parameter extraction
  SI model DB
  New wiring architecture / circuit actual proof
  EDA performance benchmark
- Others
  SRAM-TEG
  IP Process Diagnostic TEG
  WLR (Wafer Level Relinbility) -TEG

O Schedule
2002.12 Tape out (N)
2003.04 Wafer up (N)
2003.06 Report

STARC Semiconductor Technology Academic Research Center

Missions of Low Power Technology Group

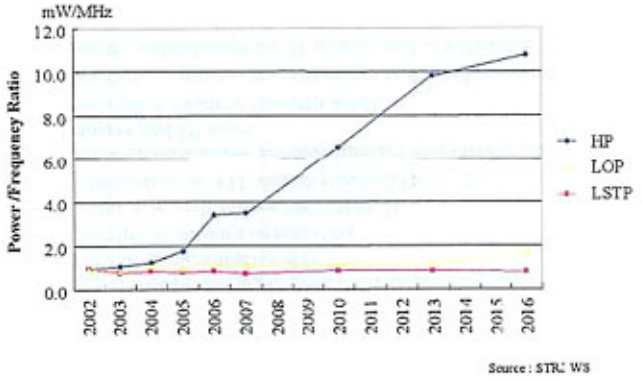
- Development of low power technology of SoC

  Low power technologies in architecture and circuit level aim at the present condition ratios 1/200

  - System (CPU) low power technology
    - **Low voltage circuit technology of 0.5V**
    - **Power control optimization technology**
  - Embedded analog technology
    - **1V operation ADC**
    - **Analog digital mixed noise technology**
  - On-chip RAM technology
    - **0.5V operation on chip RAM**

STARC Semiconductor Technology Academic Research Center

Power dissipation/Operating frequency Ratio



Source : STRC WS

STARC Semiconductor Technology Academic Research Center

Missions of IP Reuse Group

- Development of IP reuse / circulation technology
  - Establishment of criteria, such as IP description and quality
  - Actual proof experiment of IP circulation infrastructure
  - Establishment of recommended DR (design rule) usage technology
  - Development of 65nm common DR / libraries
  - Spread activities of IP related standardization

STARC Semiconductor Technology Academic Research Center

Infrastructure technology of IP reuse and circulation

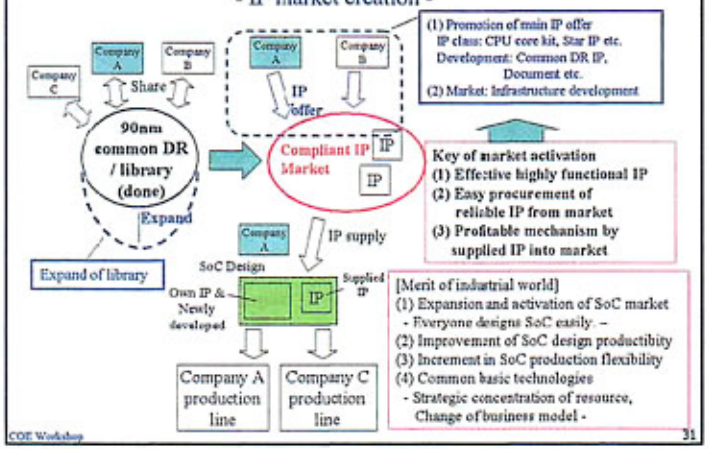
About recommended IP criteria (description, quality)

1. **Technical standards establishment for promoting coordination of system and semiconductor side**
   (IP description standard (syntax side))
   - Design style guide version 2002 (2002. 2)
   - Establishment of RTL sign-off standard (2001. 12)
2. **Standard establishment for coordination and understanding of IP developers and IP users**
   (IP description standard (semantic side))
   - Functional / synthesis description standard (draft) (2002. 3)
3. **Standard establishment for IP quality and certification**
   (IP quality standard (objective criterion of quality measurement))
   - Design property quality certification standard/scoring tool (2001. 12)
4. **IT system standard establishment for IP information distribution**
   (IP information acquirement by easy, safety, cheap way)
   - IP exchange interface standard (2002. 3)

STARC Semiconductor Technology Academic Research Center

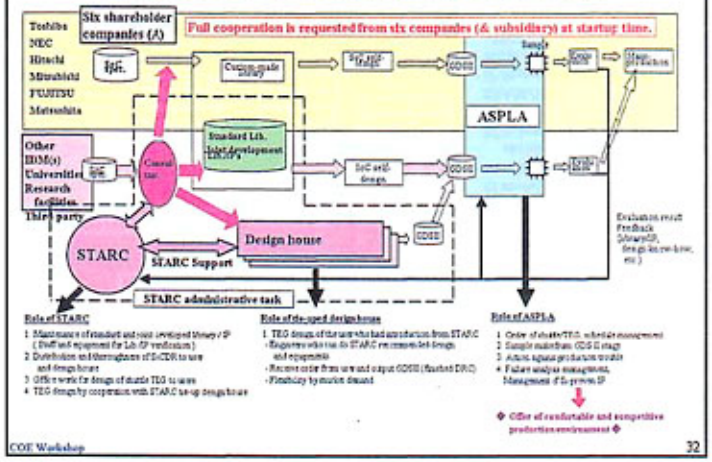
SoC design power strengthening plan

- IP market creation -



STARC Semiconductor Technology Academic Research Center

-- Assignment of shuttle employment business --



STARC Semiconductor Technology Academic Research Center

1. Semiconductor Consortia
2. Technology Trend
3. STARC Activities
4. Actibity-1
   Strengthening of SoC Design Power
5. **Activity-2**
   Research Support and Activation in Universities
6. Expectation to the "COE"

STARC Semiconductor Technology Academic Research Center

SoC Design Engineer Education Scheme

STARC Semiconductor Technology Academic Research Center

SoC Design Course (contribution, support, cooperation)

- Waseda University, Graduate school, Science and Engineering
- Keio University, Graduate school, Science and Technology
- Oita University, Graduate school, Faculty of Engineering
- Osaka University, Graduate School of Engineering Science
- Tokyo Institute of Technology, Graduate School of Engineering
- Ritsumeikan University, Institute of Science and Engineering
- Nagoya University, Graduate School of Engineering
- Kyoto University, Graduate School of Informatics
- Shizuoka University, Graduate school, Faculty of Information

STARC Semiconductor Technology Academic Research Center

Feature of STARC Design Course

- Reform design text
  - Establish embedded SW design course, create three kind of course text in 2002.
- Develop three training course
  - Training of simple AV playback system in DVD system.
  - LSI design course .. Done
    Embedded SW design / System design course .. Done
- Start advanced seminar course.
  - IP reuse design (volume on SoLID) .. done

Training equipments of DVD system and training scenery in LSI design course.

STARC Semiconductor Technology Academic Research Center

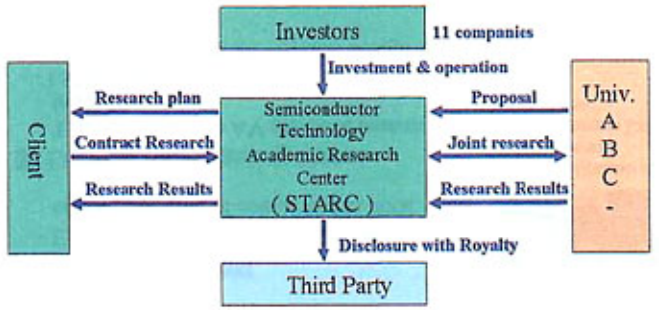
Joint Research with Universities in STARC

Basic approach with regard to joint research themes :

1) Research and development of new technologies that will become industry standards or the mainstream in a particular industry in the future.
2) Pre-competitive R&D relating to technologies that will be transferred to the industrial sector 5-10 years in the future.
3) R&D that will tie into education of young researchers who will contribute to the future of the industrial sector.
4) Target technology roadmap.
   http://www.starc.jp/roadmap/

STARC Semiconductor Technology Academic Research Center

Joint Research Plan



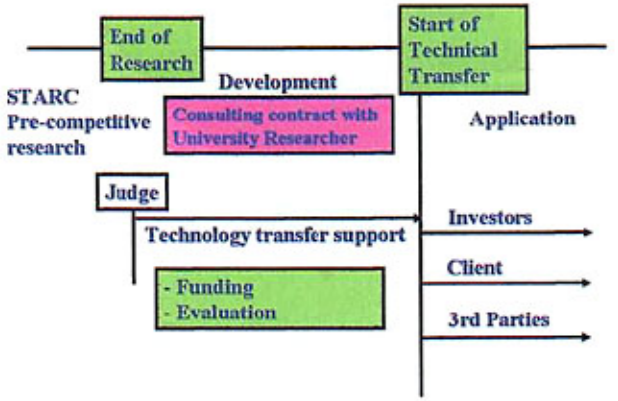
STARC Semiconductor Technology Academic Research Center

STARC supports academic research

1) In the field of Si LSI
2) Valuable and transferable to the industries within 10 years
3) 3 to 5 years project
4) Funding : 15 - 20 million yen / year for PG
   5 - 10 million yen / year for PJ
5) STARC provides industry needs and information through Visiting Researchers from member companies.

STARC Semiconductor Technology Academic Research Center

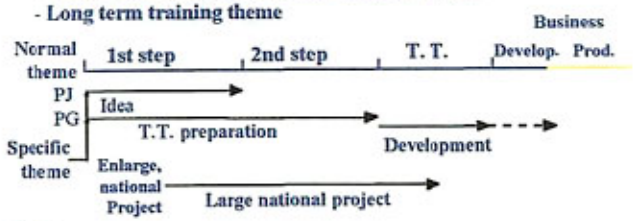
Technical Transfer



STARC Semiconductor Technology Academic Research Center

Specific theme

1. **Purpose**
   Find and support new themes about the field considered that industrial world is important.
2. **Selection points**
   - New theme
   - Enlargement of research, joint research between universities, etc.
   - Theme which may develop into national project
   - Long term training theme



STARC Semiconductor Technology Academic Research Center

Trend of university researchers

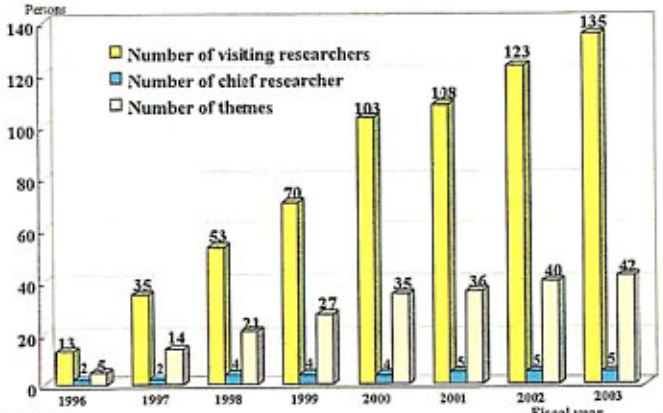
Year	Prof. Assoc. Pr.	Lecturer Assistant	Doctor	Master	Bachelor	Other	Total
1996	8	12	8	12	11	0	51
1997	25	20	28	40	24	0	137
1998	38	20	34	67	35	4	198
1999	50	26	48	95	44	9	272
2000	65	36	57	133	66	16	373
2001	59	30	48	118	44	16	315
2002	81	38	50	147	38	16	370

Position Sequence

Year	IT Comp.	Other Comp.	University	Proceed to	Total
1999	14	14	4	30	62
2000	26	25	6	70	127
2001	34	28	9	45	116
2002	45	31	5	62	143

STARC Semiconductor Technology Academic Research Center

Trend of themes and visiting researchers



STARC Semiconductor Technology Academic Research Center

Research Program and Projects in 2003 (42 themes)

	Area	Research representative
System 28	Architecture 11	Amano (Keio U.) Kasahara (Waseda U.) Maejima (T.I.T.) Mattausch (Hiroshima U.) Miyanaga (Hokkaido U.) Murakami (Osaka U.) Nishikawa (U. of Tsukuba) Sakai (U. of Tokyo) Sueyoshi (Kumamoto U.) Sugino (T.I.T.) Yoshimoto (Kanazawa U.)
	LSI circuit 6	Hyogo (Science U. of Tokyo) Iwata (Hiroshima U.) Kawahito (Shizuoka U.) Kobayashi (Gunma U.) Kuroda (Keio U.) Taniguchi (Osaka U.)
	Design technology 11	Asada (U. of Tokyo) Fujita (U. of Tokyo) Fujiwara (NIST) Hamaguchi (Osaka U.) Higashino (Osaka U.) Iwai (Osaka U.) Iwasaki (TMU) Nakajima (TUT) Sakurai (U. of Tokyo) Takamatsu (Ehime U.) Terai (Ritsumeikan U.)
Process 14	Device 7	Miura (Hiroshima U.) Ogawa (Kobe U.) Okuyama (Osaka U.) Shibahara (Hiroshima U.) Taniguchi (Osaka U.) Toriumi (U. of Tokyo) Kamidono (U. of Tsukuba)
	Process 4	Hamaguchi (Kyoto U.) Keike (Tohoku U.) Masu (T.I.T.) Samukawa (Tohoku U.)
	Common 3	Iwai (T.I.T.) Koyanagi (Tohoku U.) Oshima (U. of Tokyo)

STARC Semiconductor Technology Academic Research Center

Joint Research with Hiroshima University and STARC

1. Prof. Iwata "Analog Digital Mixed Circuit" (1996)
   "Low Voltage Analog Circuit Design for Low Noise Systems" (2003)
2. Prof. Miura "Research on Predictive TCAD for Concurrent Engineering" (1998)
   "HiSIM: A MOSFET Model for Circuit Simulation with Focus on RF Applications" (2002)
3. Prof. Mattausch "Super-Compact Multi-Port Memories with Large Random-Access Bandwidth and their Application for High-Performance Systems on a Chip / Package" (2001)
4. Prof. Shibahara "Research on the Gate Stack Structures with Dual-Metal and ALD Insulator for Advanced CMOS Technologies" (2001)

STARC Semiconductor Technology Academic Research Center

1. Semiconductor Consortia
2. Technology Trend
3. STARC Activities
4. Actibity-1
   Strengthening of SoC Design Power
5. Activity-2
   Research Support and Activation in Universities
6. **Expectation to the "COE"**

STARC Semiconductor Technology Academic Research Center

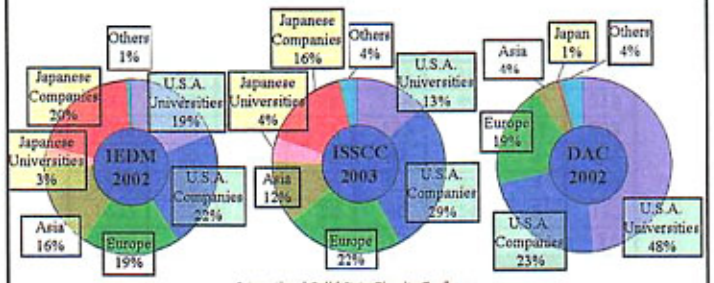
Role of Engineering Sector in University

	U.S.A	Japan
1926s	Europe University Concept Established Bell Laboratories	Europe University Concept
1946s	Success of company research Establishment of research center of companies	
1970s	Retreat from company research Utilization research to a university	Company founds research center. Campus dispute
1980s	SRC starts activity. (1982) Utilization research in universities SEMATECH establishment (1987) MARCO starts activity (1998)	STARC starts activity. (1996)
2000s		Retreat from company research University tackles industry-university cooperation.

Bibliography R. Rosenbloom, W. Spencer work, Yasko Hakimoto translation "The end of the time of a central research institute" 47

STARC Semiconductor Technology Academic Research Center

Comparison of papers in IEDM and ISSCC and DAC



International Solid-State Circuits Conference

International Electron Device Meeting

Design Automation Conference

STARC Semiconductor Technology Academic Research Center

Expectation to the "COE"

1. **The Pioneer Role to Silicon Technology**
   Leading-edge researches and information dispatch in pre-competitive area.

2. **Cultivation of researchers with "Double Major" area of investigation - Fusion and Diversity**
   Talented researchers who could expand his research area to boundary and different domain strategically.

3. **Projects proposed by active young researchers**
   -- STARC anticipates those proposals. --