The Impact of nm CMOS Technology on Wireless Circuit and System

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Due to the continuous progress in semiconductor fabrication technology, many successful integrations of complete radio system including both RF front end and digital base band circuit in a chip have been reported. The driving force for this effort is the cost reduction as well as the improved performance. In this presentation, we show the impact of CMOS technology scaling on the various RF circuit components such as active, passive and digital circuits.

For the active circuits, the impact of scaling on the LNA noise and linearity, one of the most important circuit elements in RF front end, is thoroughly analyzed first. Then two new circuits inventions named CCPP (CMOS Complementary Parallel Push-pull) circuit and the use of parasitic V-NPN (Vertical-NPN) bipolar transistor for DCR (Direct Conversion Receiver) are introduced. In CCPP, the high RF performance of PMOS comparable to NMOS, provides single ended differential RF signal processing capability without the use of bulky balun. The use of parasitic V-NPN (Vertical-NPN) bipolar transistor, available free in triple well CMOS technology, has shown to provide more than an order of magnitude improvement in 1/f noise and DC offset related problems, which have been the bottleneck for CMOS single chip integration.

As for the impact of CMOS technology scaling for various passive devices, performance scaling for the inductor, variable capacitors, MIM capacitor, and switched capacitor, are discussed. Both the forward scaling of the active layer as well as the inverse scaling of interconnection layer, i.e., more interconnection layers with effectively thicker total dielectric and metal layers, provide very favorable scenario for all passive devices.

Because of the accuracy, adaptability, flexibility, and programmability, digital circuitries are employed more and more in RF front end these days. In this last part of our presentation, the impact of CMOS scaling on the various digital circuits are analyzed, taking the digital modem blocks, on the various digital calibration circuits, on the switching RF power amplifier, and finally on the software defined radio, as examples.

MICROS: Low Cost and Low Power CMOS Radio For Ubiquitous Network Application

Mar 17th, 2003

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WPAN Trends

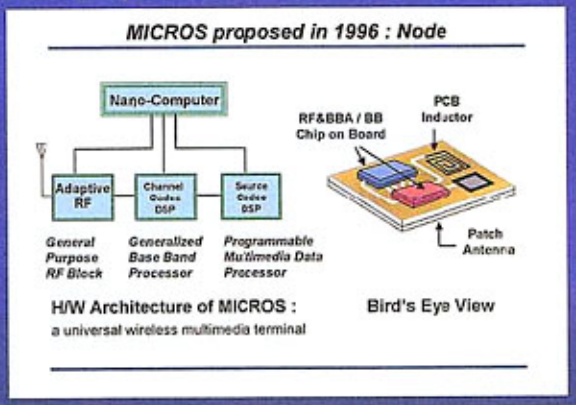
- Bluetooth : *Started feasibility study in 1994 inside Ericsson and SIG formed in 1998*
- PAN : *Proposed in 1995 in MIT*
- **MICROS** : *Proposed in 1996 in KAIST*
- Pico Radio : *Proposed in 1999 in Berkeley*
- IEEE 802.15 Standards : started in 2000
  - *TG1 Bluetooth*
  - *TG2 Compatibility*
  - *TG3 High Rate*
  - *TG4 Low Rate*
- **MICROS** *was introduced at ISSCC '03 (Paper 5.4) as the 1st IEEE 802.15.4 prototype.*

Single Chip Radio Vision: MICROS

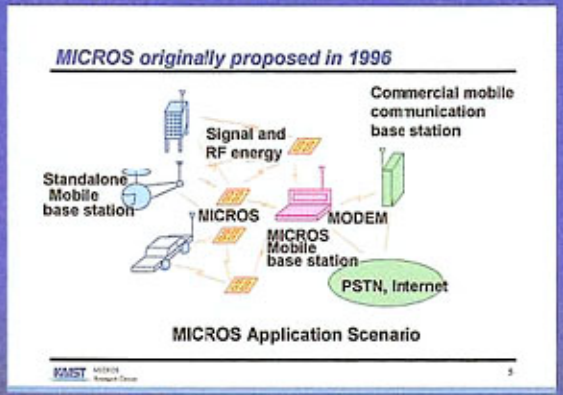
- MICROS Research Center: Micro Information and Communication Remote Object-oriented System
- Established in 1997 and supported by KOSEF
- To Develop Programmable, Adaptive, Wearable, Coin-sized Wireless Terminal with Extremely Low Power Consumption for Distributed System such as Sensor Networks

- MICROS : Micro Information Communication Remote Object-oriented Systems
- KOSEF : KOrea Science and Engineering Foundation

MICROS proposed in 1996: Node

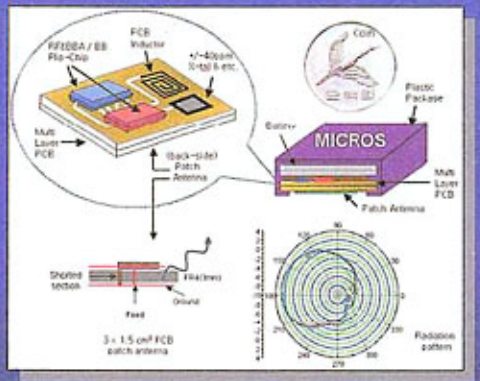


MICROS proposed in 1996: Network



MICROS: A Pioneering Concept for Ubiquitous Network

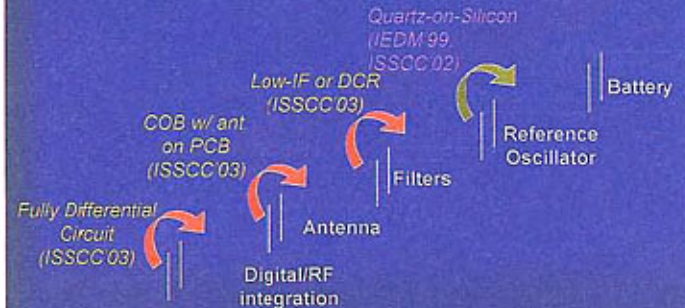
MICROS Node in 2002



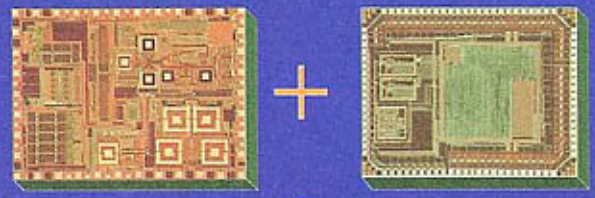
Design Focus for MICROS

- Low Cost
  - *Single chip radio using low-IF or DCR*
  - *Direct integration on PCB using COB technology*
- Low Power
  - *Network level power management*
  - *Simple node and highly sensitive base station*
  - *Linearity/power optimization than sensitivity*
  - *PLL power optimization*
- Digital
  - *Programmability*
  - *Self calibration – No tuning!*
  - *Lower signal processing power at lower frequency*

MICROS Breakthrough's for Single Chip Barrier



The 1st IEEE802.15.4 Prototype



2.4GHz RF Receiver / Transmitter

- Active Power Consumption (@1.8V)
  - 21mW in receive mode
  - 30mW in transmit mode
- 3MHz Channel Spacing / 8 Channels
- 2.2Mcps (200kbps data rate)
- Digital Trimming Circuits

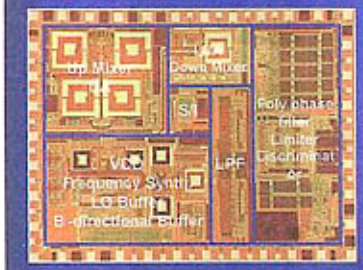
Single Chip Radio (ISSCC 2003 Paper)

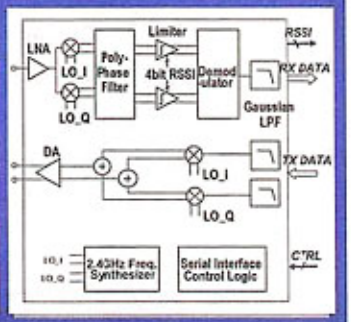
Digital Modem, MCU / DSP Core

- 500uW @ 4.4MHz clock
- Modem : Supporting PHY Layer
- MCU : Supporting MAC Layer
- System Controller : Power Management (0.1% duty for 1mW average power consumption)

RF Transceiver

2.4GHz RF Receiver / Transmitter
(TSMC 0.18um RF CMOS : 3.5mm x 2.5mm)

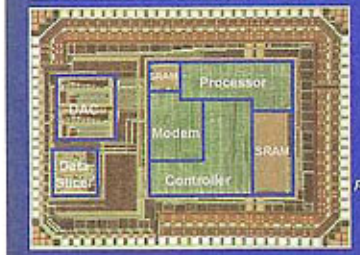




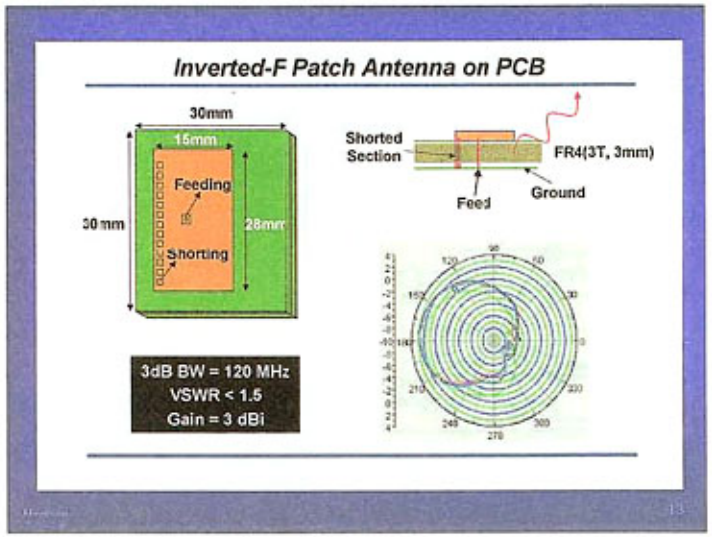
- Receiver : Low-IF (4MHz) architecture / Image rejection in poly-phase filter / LD non-coherent detection
- Transmitter : ROM based I/Q direct modulation / differential nonlinear drive amplifier
- Frequency Synthesizer : Fully integrated & fully differential integer N PLL

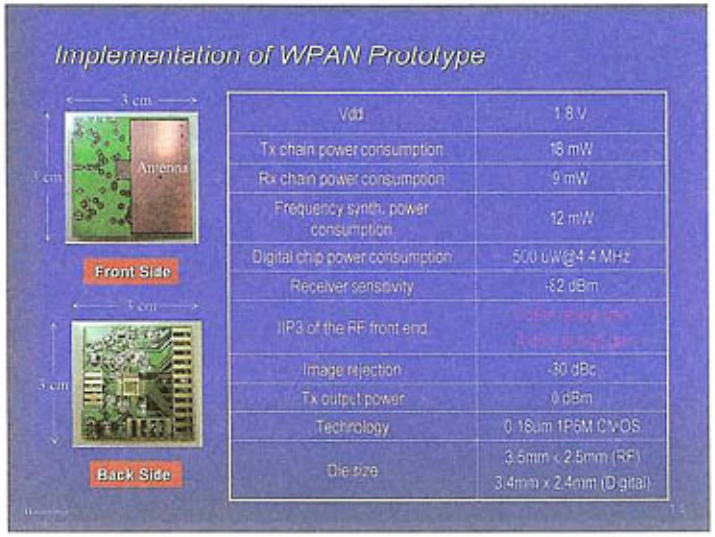
Digital Baseband Processor

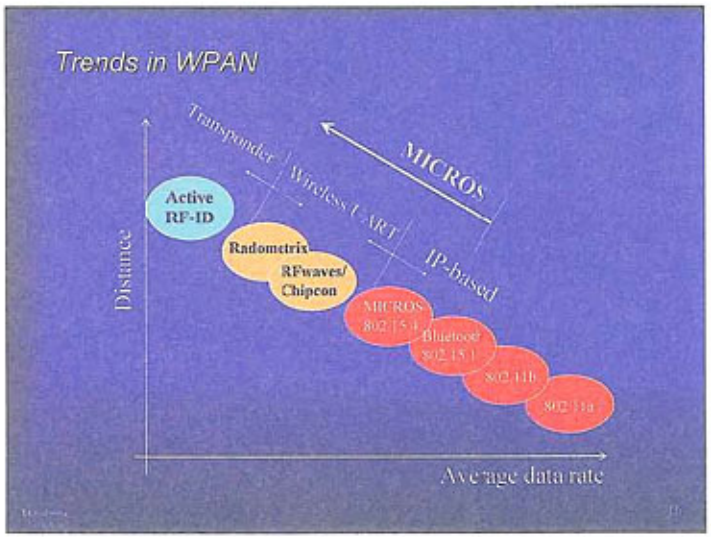
Digital Modem, MCU / DSP Core
(TSMC 0.18um CMOS : 3.4mm x 2.4mm)

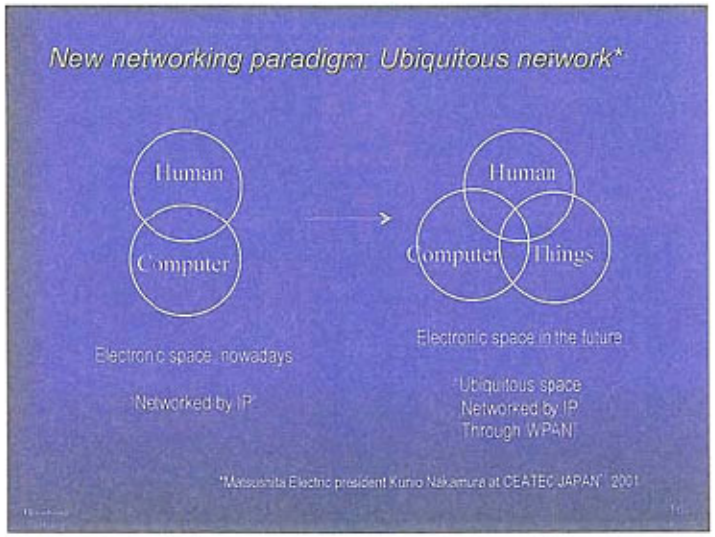


- MODEM (Supporting PHY Layer) : Modulation / Spreading / Error correction coding
- MCU (Supporting MAC Layer) : Simplified CSMA-CA
- System Controller : Power management


Inverted-F Patch Antenna on PCB
30mm
15mm
Feeding
30 mm
28mm
Shorting
Shorted Section
FR4(3T, 3mm)
Feed
Ground
3dB BW = 120 MHz
VSWR < 1.5
Gain = 3 dBi


Implementation of WPAN Prototype
3 cm
3 cm
Antenna
Front Side
3 cm
3 cm
Back Side
Vdd 1.8 V
Tx chain power consumption 18 mW
Rx chain power consumption 9 mW
Frequency synth. power consumption 12 mW
Digital chip power consumption 500 uW@4.4 MHz
Receiver sensitivity -82 dBm
IIP3 of the RF front end
Image rejection -30 dBc
Tx output power 0 dBm
Technology 0.18um 1P6M CMOS
Die size 3.5mm x 2.5mm (RF)
3.4mm x 2.4mm (Digital)


Trends in WPAN
Transponder
Wireless UART
MICROS
IP-based
Active RF-ID
Radiometrix
RFwaves/ Chipcon
MICROS 802.15.4
Bluetooth 802.15.1
802.11b
802.11a
Distance
Average data rate


New networking paradigm: Ubiquitous network*
Human
Computer
Electronic space nowadays
"Networked by IP"
Human
Computer
Things
Electronic space in the future
"Ubiquitous space
Networked by IP
Through WPAN"
*Matsushita Electric president Kunio Nakamura at CEATEC JAPAN' 2001

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2003.3

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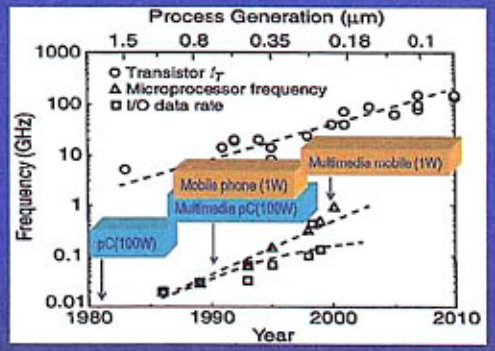
Semiconductor scaling removes the energy barrier for personal information services



10x improvement in 10 years has introduced new generations of service

Ref [Kle00]

Impact of Active Device Scaling on RF Circuits and System

CMOS Scaling for RF analog

$I = W/L \cdot \mu Cox \cdot (Vgs-Vth)^2$

$= K \cdot W/L \cdot (Vgs-Vth)$

where $\mu Cox (Vgs-Vth)$ is almost technology independent, due to mobility degradation, Rs, etc

$Gm = 2K \cdot W/L$

$=$ constant

In RF circuit,

i) $1/Gm \sim Zo = 50$ Ohm

ii) Vgs-Vth cannot scale due to the required voltage headroom

Thus

$I \sim (Vgs-Vth) \sim$ constant

$Gm =$ constant

$Cg \sim \lambda$

$f_T \sim 1/\lambda$

$f_{max} \sim 1/\lambda$

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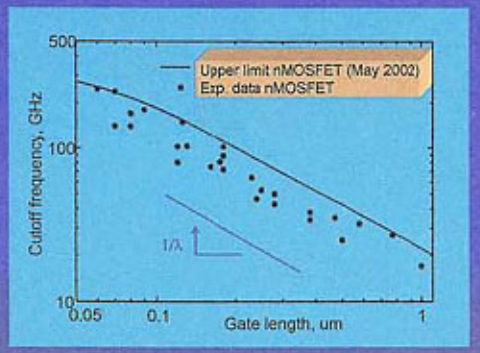
f_T scaling of RF CMOS



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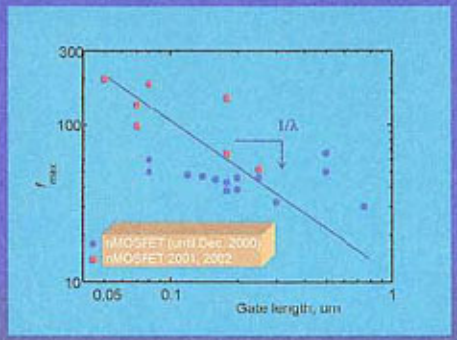
* Figure prepared by Prof. Lisoo

f_{max} scaling of RF CMOS



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* Figure prepared by Prof. Lisoo

CMOS Scaling for LNA

- $NF_{min} = 1 + K_f \cdot f/f_T$

  $= 1 + K_f \cdot \lambda$

  NF_{min} = scales as λ in dB scale

- $NF = NF_{min} + Rn/Gs \cdot [(Gs - Gs,opt)^2 + (Bs - Bs,opt)^2]$,

  where $Rn \sim \lambda$, $Gs,opt \sim 1/\lambda$, and $Bs,opt \sim 1/\lambda$

Optimum matching becomes tougher by $1/\lambda$ times.
But the noise circle becomes broader by $1/\lambda^2$ times.

↓

Over-ally much better from LNA circuit design point.

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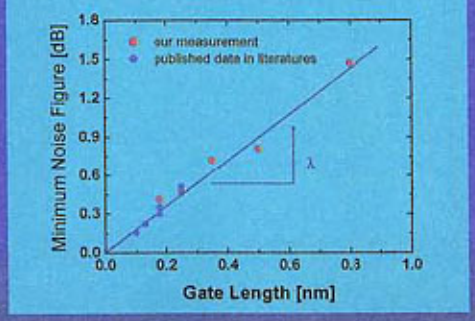
Minimum Noise Figure (NFmin) Scaling



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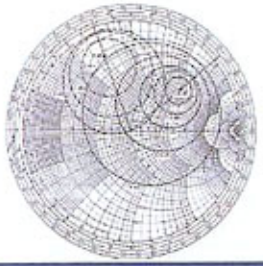
* Data sources from K.S. Han

Both power and noise cannot be matched in CSFET

- Need to comprise between impedance matching and noise matching
- Both gain and noise circles together can be used to find an optimum point for source impedance

Gonzalez [17]



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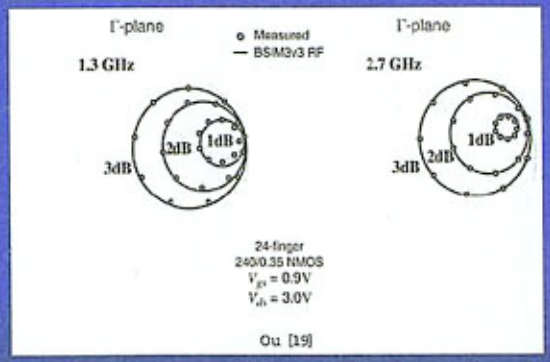
The impact of Rn/Gs in gain/power matching



Large circle means less sensitivity on noise (mis)-match.

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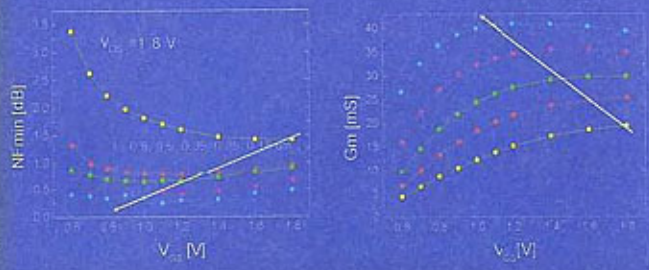
Minimum Noise Figure (NFmin) of NMCSFETs



- Scaling leads smaller NF_{min} as well as less bias sensitivity

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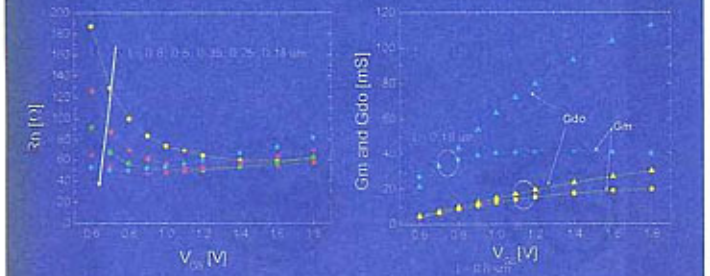
* Data sources from K.S. Han

Noise Resistance (Rn) of NMOSFETs



- Rn scales down, leading to smaller NF_{min} as well as less noise matching sensitivity.

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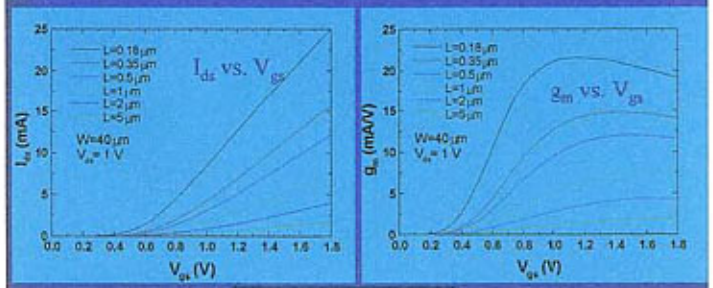
* Data courtesy from K.S. Han

I_{ds} and g_m vs. V_{gs} with Gate Length

- Measurements : TSMC 0.18 μm foundry NMOS



$$I_{ds} = g_m v_{in} + \frac{1}{2} g_m^{'} v_{in}^{2} + \frac{1}{6} g_m^{''} v_{in}^{3}$$

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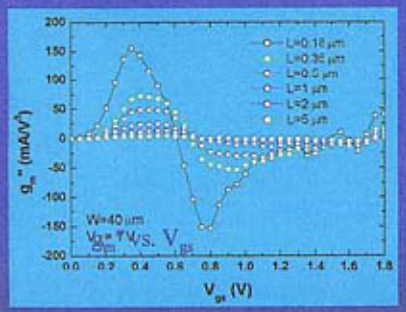
* Data courtesy from J.I. Kwon

g_m'' vs. V_{gs} with Gate Length

- Measurements : TSMC 0.18 μm foundry NMOS



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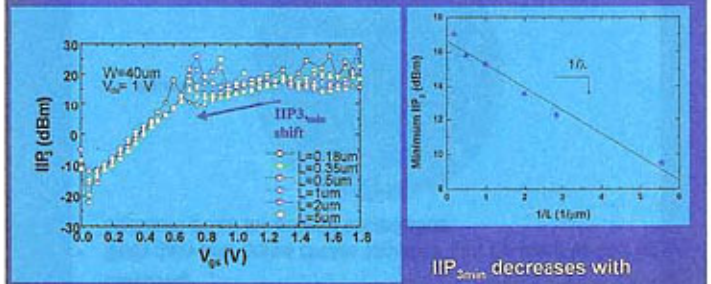
* Data courtesy from J.I. Kwon

IIP_3 vs. V_{gs} with Gate Length



IIP_{3min} decreases with device scaling !

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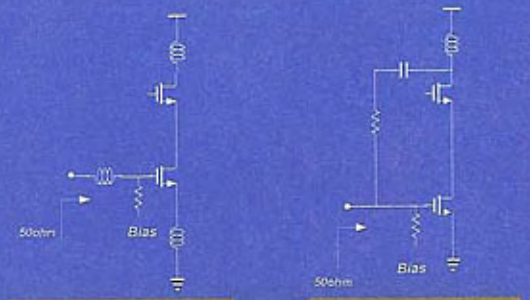
* Data courtesy from J.I. Kwon

Linearity improvement methods

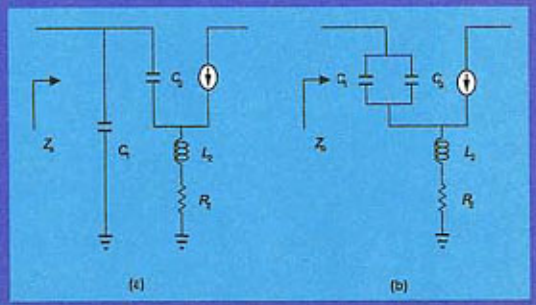
- Linearity scales adversely.
- However, higher gain (Gm) and lower noise in scaled device, allows us to make trade-off these to improve linearity using various desensitization techniques, exactly as in operational amplifier circuits, such as
  - Source degeneration using resistor
  - Source degeneration using inductor
  - Cascode resistive feedback
  - Add extra input capacitance

Desensitization using negative feedback



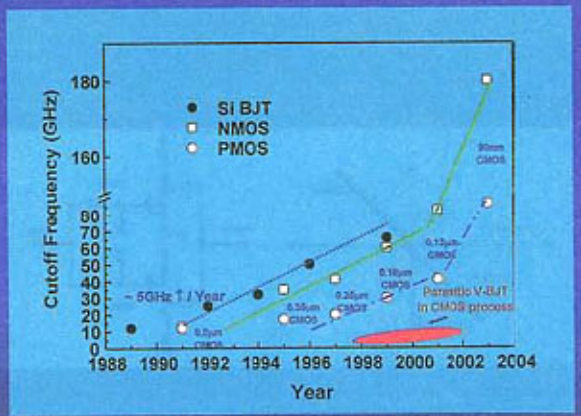
Source Degeneration LNA | Cascode Feedback LNA

Desensitization using extra capacitance



Two ways to add extra capacitences to the gate.

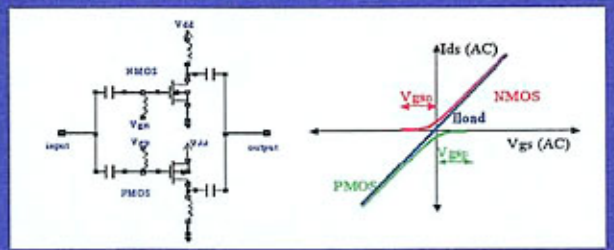
High Frequency Performance of Scaled Si Devices



Complementary Push Pull RF circuits

- Advantages of complementary push pull circuits
  - Push pull action (Famous Static CMOS logic)
    - Symmetric pull up and down
    - Less power consumed
  - Inherently single ended differential
    - Even harmonic cancellation
    - Single balanced mixer without balun
    - Double balanced mixer with 1 balun

Concept of CCPP(Complementary CMOS Push-Pull)*



- Single-ended input, differential operation without large-size baluns
- Immune to even order distortion
  - Adequate for DCR & low-IF receivers

* This is patented by MICROS

NMOS vs. CCPP Amplifier: Experimental Results

	CCPP amplifier	NMOS CS amplifier
Gain	12.4dB	12dB
NF	2.0dB	1.9dB
IIP2	56dBm	43dBm
IIP3	8.1dBm	7.5dBm
Power consumption	14.91mW @1.8V	14.04mW @1.8V
F.O.M. (Linearity) $10\log\frac{OIP_3(mW)}{P_{DC}(mW)} + 10\log\frac{OIP_2(mW)}{P_{DC}(mW)}$	53.4dB	51.6dB

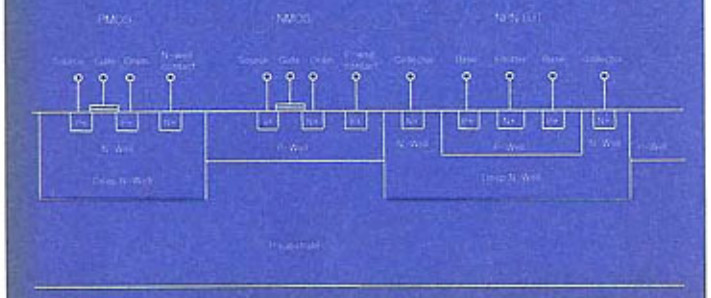
* Data courtesy from D. K. Nam

Complementary Resistive Mixers

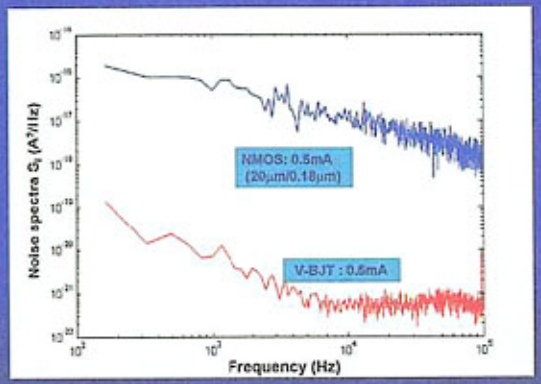
	Conventional unbalanced NMOS resistive (UNR) mixer	Unbalanced complementary resistive (UCR) mixer	Single-balanced complementary resistive (SCR) mixer
DC power consumption	0	0	0
LO power	4dBm	4dBm	4dBm
Conversion gain	- 8.5dB	- 7.9dB	- 8dB
NF	8.9dB	8.4dB	8.4dB
IIP2	42.4dBm	47dBm	53dBm
IIP3	11.5dBm	13dBm	13dBm
LO-to-IF isolation	25dB	43dB	46dB
LO-to-RF isolation	21dB	17dB	39dB

* Data courtesy from D. K. Nam

Parasitic V-NPN in Triple-Well CMOS Technology

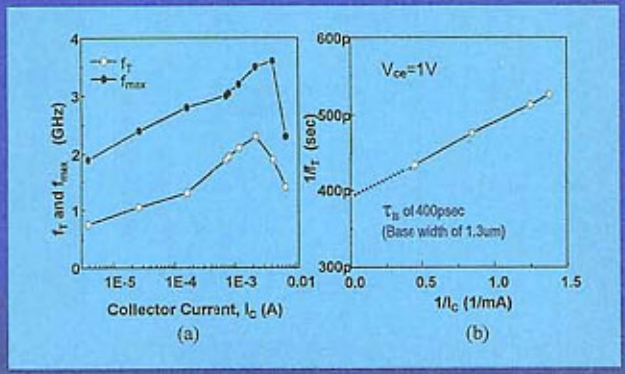


Flicker Noise Measurement

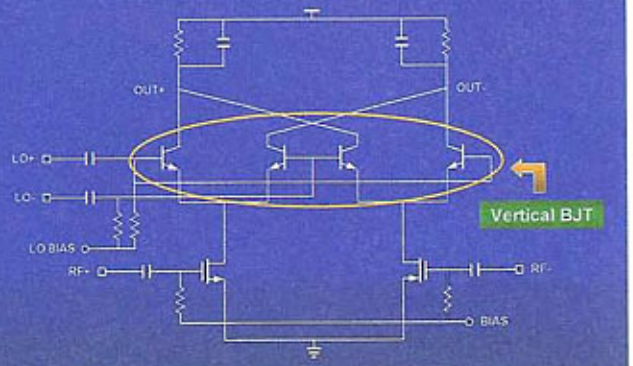


* Data courtesy from I.K. Nam

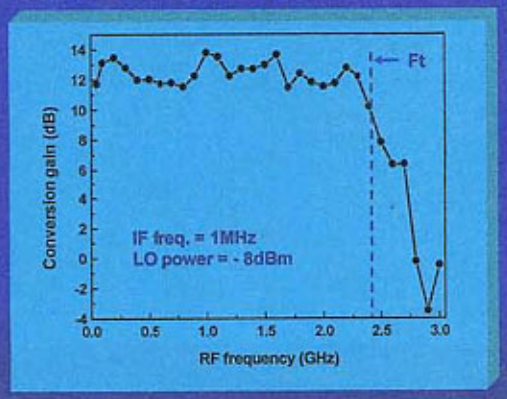
f_T and f_{max} of V-NPN



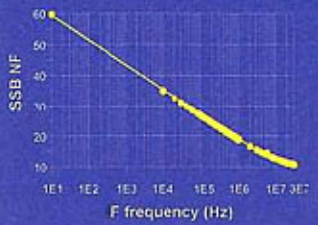
Gilbert Mixer Using CMOS and V-NPN for DCR



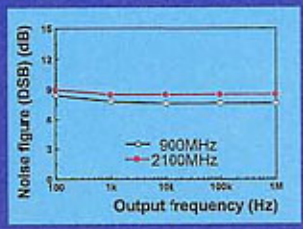
Conversion gain vs. frequency



NF Comparison of Two RF Front-ends

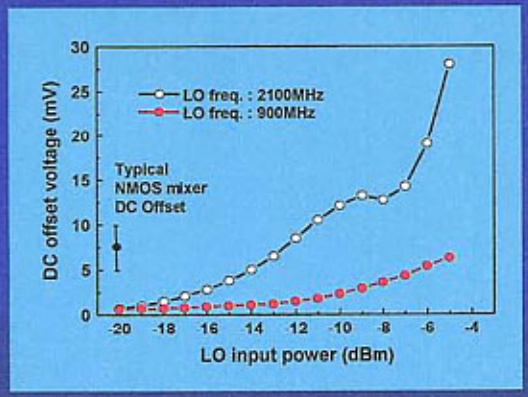


CS LNA + Mixer with NMOS switching pair - Simulated



CS LNA + Mixer with V-NPN switching pair - Measured

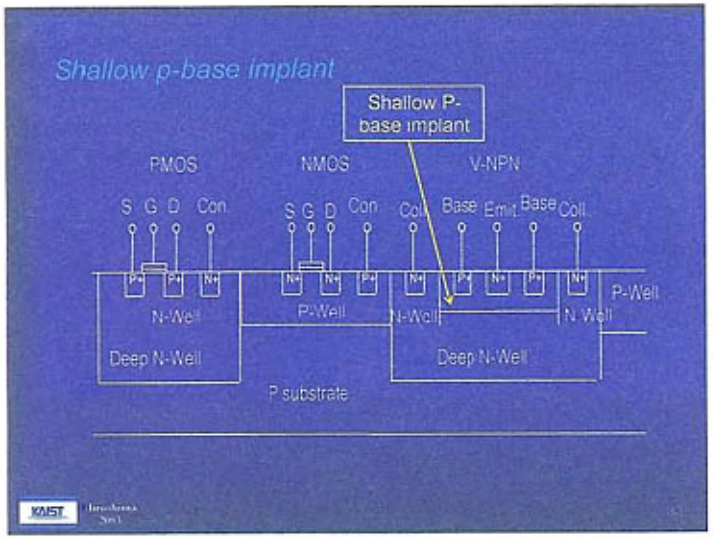
Measured DC Offset Voltage



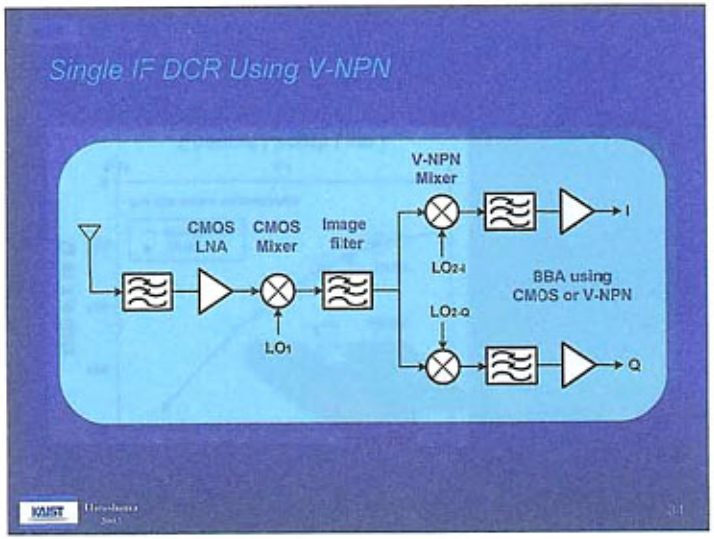
Two ways to increase operating frequency

- Process change:
  - Currently f_T is dominated by the base transit time across p-well (1.3 um for 0.18 um CMOS process).
  - Thus with an additional process step for shallow base p type implant, higher cutoff frequency of V-NPN can easily obtained.
- Receiver architecture change:
  - Single IF DCR
  - Weaver DCR

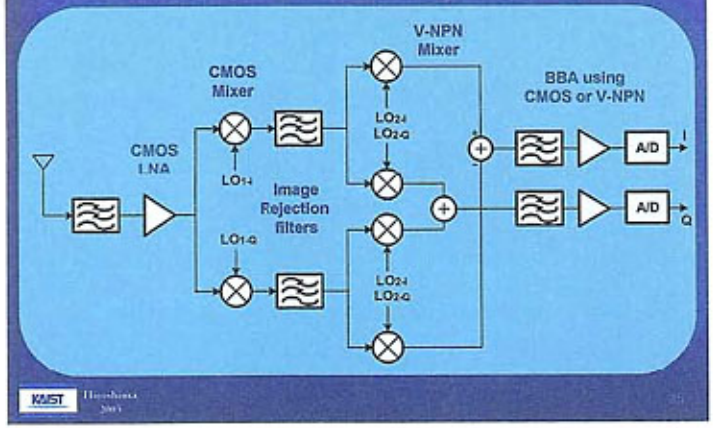
Shallow p-base implant



Single IF DCR Using V-NPN



Weaver DCR Using V-NPN



Interconnect Technology Impact on RF Performance of Passive Devices

Passive devices scaling

- Technology Roadmap for Interconnect
- Impact on RF Performance of Passive Devices
  - Inductor
  - MOS Varactor
  - MiM Capacitor
  - MOS Switch & Switched-Capacitor
- Summary
- References

Technology Roadmap for Interconnect

- SoC Interconnect Technology SIA Roadmap

Year	1999	2001	2002	2003	2004	2005	2008	2011	2014
ASIC gate length (μm)	0.15	0.15	0.13	0.12	0.11	0.10	0.07	0.05	0.035
# of metal levels	6	7	7	7-8	8	8	8	9-10	10
Interlevel metal insulator – effective dielectric constant (κ)	3.5-4.0	2.7-3.5	2.7-3.5	2.7-3.5	2.2-2.7	1.6-2.2	1.5	<1.5	<1.5

Expected by KAIST

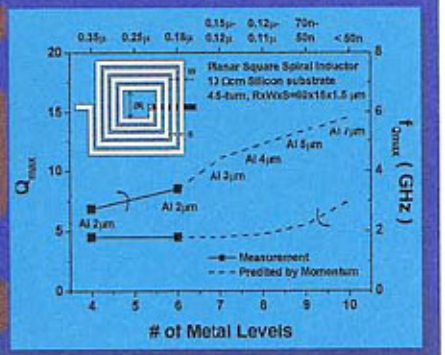
Year	1999	2001	2002	2003	2004	2005	2008	2011	2014
Top-level to sub. distance (μm)	7.5-8.5	8.5-9.5	8.5-9.5	8.5-10.1	10.1-11.1	10.1-11.1	11.4-12.4	11.4-13.1	12.7-13.1
Top-metal thickness with RF option (μm)	2.0	2.0-3.0	3.0	3.0-3.5	3.5-4.0	4.0-5.0	5.0-6.0	6.0-7.0	>7.0
					or Cu interconnection				

On-Chip Inductor

Technology scaling

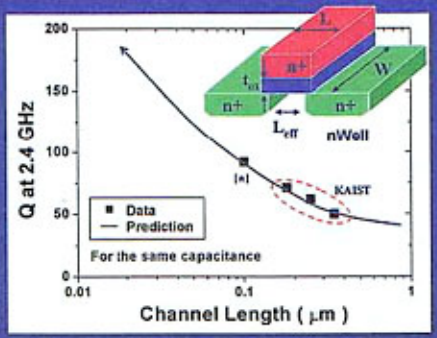
# of Metal layers ↑
Top metal thickness ↑
Dielectric constant ↓
Top level to substrate distance ↑

Series resistance ↓
Substrate parasitics ↓



- As # of metal layers increases, Q_{max} and f_{Qmax} increase.

MOS Varactor

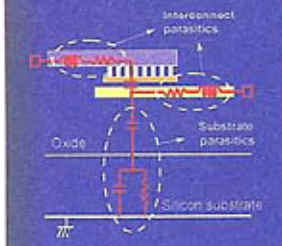


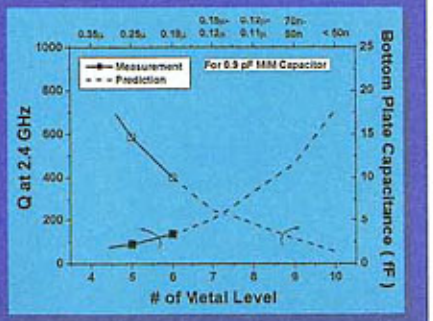
$L \rightarrow \lambda \times L$

$\Rightarrow \begin{cases} Rch \sim \lambda \\ Cox \sim 1/\lambda \\ L \times W/Tox \approx \text{constant} \end{cases}$

- Scaling leads to increase Q and layout density
- For constant L×W/Tox, tuning-range is constant or slightly increases.

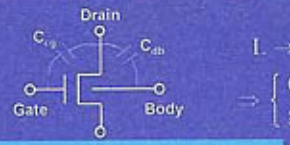
MiM Capacitor



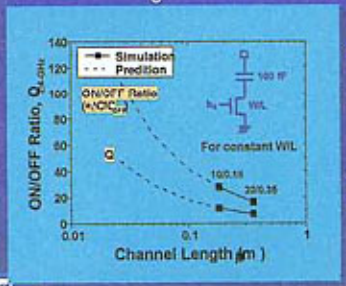


- Parasitics will reduce as increasing of metal levels.
- As # of metal levels increases, the Q increases and the bottom-plate capacitance reduces.

MOS Switch & Switched Capacitor



$$L \rightarrow \lambda \times L \Rightarrow \begin{cases} C_J (= C_{db} + C_{gb}) \sim \lambda \\ g_{ds} \sim 1/\lambda \end{cases}$$



- ON/OFF ratio of switched capacitor will be larger.

$$ON/OFF\ Ratio = \frac{C_{ON} - C_{OFF}}{C_{OFF}}$$

- Q increases.
- Combining the improvement of the MiM capacitor, Q becomes much larger.

The Impact of Device Scaling for Digital Circuits on RF System

Scaling law for CMOS Digital Circuit

- No voltage scaling:

  V = 1
  I = 1
  C ~ λ
  f ~ 1/λ
  P ~ I
  E ~ λ

  Energy required to do the given job scales as λ.

- With voltage scaling:

  V = λ
  I = λ
  C ~ λ
  f ~ 1
  P ~ λ²
  E ~ λ³

  Energy required to do the given job scales as λ³.

Analog vs. Digital Radio

- Digital communication : the carrier is modulated by a digital BB signal
- Digital radio : DSP is used in (over-sampled) BB, IF, RF signal processing and controls

Advantages of Digital Communication

1. Source coding
   - Compression / Decompression
2. Signal modulation / demodulation
   - Spectral efficiency
   - Easy to adopt highly sophisticated channel codec (Modem, Equalizer, ECC,)
   - Programmability and adaptability
   - Encryption / decryption
   - Frequency spread / despread
3. Control
   - Various communication protocol
   - Adaptability, expandability, compatibility

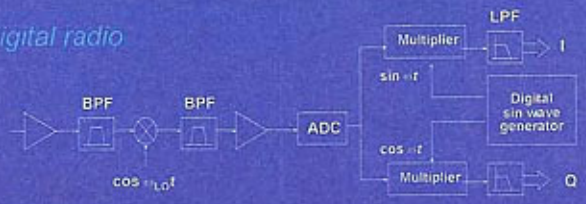
- Robustness, Immune to noise and multipath fading
- Supported by the enormous momentum of digital markets

Why Digital Radio ?

1) Accuracy
   6dB/bit and ppm accuracy of clock
2) Adaptability
3) Flexibility
4) Programmability

- Sophisticated signal processing: selectivity and sensitivity up to Shannon's limit
- Auto calibration (trimming) of non-ideal analog circuits, mismatch, distortion, etc.
- Precise waveform shaping
  - Bandwidth/BER/power efficiency optimization
- Software defined radio

Digital radio

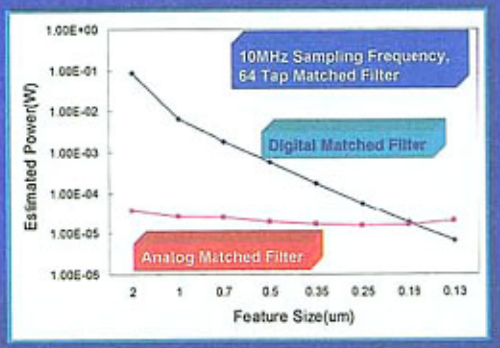


- Similar to the dual-IF superheterodyne
- Second IF processing is performed in the digital domain
- Advantage
  - Much better signal processing accuracy
  - Programmability and Flexibility -> SDR (Software defined radio)
- Issue
  - A/D converter performance : Quantization, thermal noise, dynamic range, power consumption of ADC
  - DSP processing power

New Wireless Technology – Software Defined Radio (SDR)

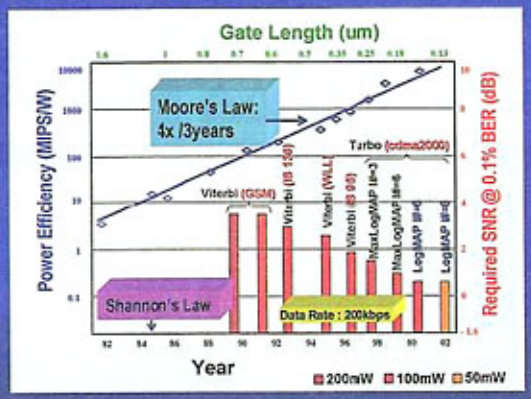
- *Classifications of SDR*
  - Software Defined Radio
    - One H/W platform & several S/W s for each communication standard
    - Ex : dual-mode phone
  - Software Radio
    - A part of analog signal processing => software
    - Most popular among the three SDRs
  - Ideal Software Radio
    - RF amplifier + ADC + software
    - General purpose digital radio

Power Consumption Comparison: Analog and Digital Matched Filter Example



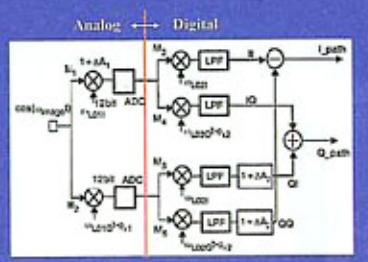
* Figure prepared by B-I. Seo based on the paper by M.D. Halan, IEEE Trans. CAS-I, 1997

Impact of Moore's law on Shannon's sensitivity law



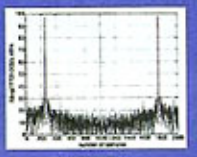
* Figure prepared by S.C. Park

Digital I/Q Mismatch Compensation-I

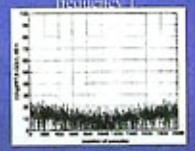


Weaver architecture with digital cancellation block of gain/phase mismatch

=> Improve Image Rejection Ratio (IRR)



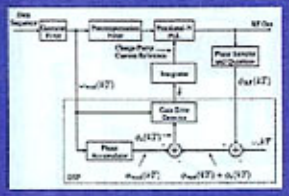
[I for data frequency]



[I for image frequency after compensation, 70dB IRR]

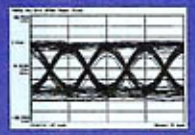
*Ref. Y.J. Kim et al. Electronics Letters, 2004

Digital I/Q Mismatch Compensation-II



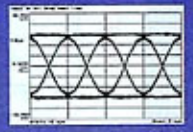
Automatic Calibration of Modulated Frequency Synthesizer

=> **Improve Demod. Eye Pattern**



[Gain too low]

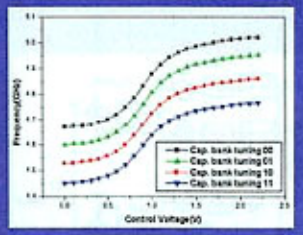
[Gain too high]



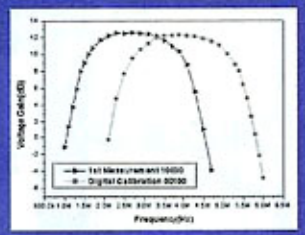
[Auto calibration enable]

*Ref. Daniel, IEEE Trans. CAS 2002

Digital Trimming



Digital Calibration of VCO Oscillation Frequency

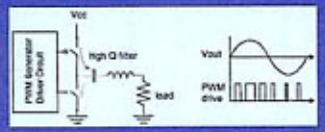


Digital Calibration of IF Filter Response

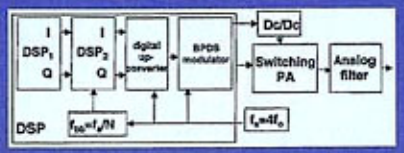
* Figure prepared by S.-H. Kim

Full Digital Switching Mode Power Amplifier

- Class-S Power Amplifier with 100% Efficiency



Schematic structure of class-S amplifier



Possible DSP-based wireless transmitter architecture

*Ref. Asbeck, IEEE Trans. MTT, 2000

Conclusion

- Near future radio will be all digital except RF LNA, Mixer, and RF filter.
- Some day, we will have all digital radio (except LNA), such as Ideal Software Radio and UWB tranceivers.

Acknowledgement:

- This research was supported by KOSEF.
- 15 graduate students in our laboratory involved in MICROS Research Center. 10 in RF and 5 in digital circuits.