HiSIM: Present Status and Future Perspective

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1 Abstract

HiSIM, the circuit simulation model, development concept and status are summarized. Concerning our 21th COE project, the future development plan will be discussed, aiming at connecting technology to circuit for concurrent development.

2 Introduction

Requirements for circuit simulation are increasing due to two ongoing developments, namely, the downscaling of MOSFETs into the sub-100nm regime and system integration with many different functions on a single chip. To assist in the developments, models for circuit simulation should be pragmatic, but should be accurate at the same time. HiSIM (Hiroshima-university STARC IGFET Model), aiming to fulfill both requirements, is based on an iterative surface-potential determination directly related to technology applied (1,2).

3 Basic Concept of HiSIM

The basic equations for describing device characterisitcs are:

- The Poisson equation
- The current-density equation
- The continuity equation

These equations are simultaneously solved numerically in two-dimensional device simulators. On the other hand, these equations are solved analytically using transistor models for circuit simulation, yielding simplified description descriptions for device performances. The difference in comparison to 2D device simulators is that two additional approximations are applied. One is the charge-sheet approximation assuming zero thickness of the inversion charge, and the other is the gradual-channel approximation assuming smooth potential increase along the channel. These approximations allow to derive an analytical formulation for all device performances as a function of the surface potentials at source side and drain side. The surface potentials are obtained by solving the Poisson equation iteratively. In spite of the iteration the calculation time is not longer than with BSIM3v3, frequently applied. The charge-sheet approximation is not severe, since the inversion-layer thickness is at most a few nanometers.

A better circuit model has less model parameters, without compromising accuracy. The model parameters should be connected to device parameters and should be measurable independently. To realize this concept, we have developed the model HiSIM based on the same ideas as 2D device simulators (3) under the collaboration with STARC. Namely, to treat the potential distribution in the device as the core of the model and not the applied voltages as conventional models. Thus, HiSIM is the first MOSFET model for circuit simulation based on the complete surface-potential description, and the source code and the manual have been released for the public since the end of 2001. The total number of model parameters is 72 for performing circuit simulations. Typical features of simulation results with HiSIM are demonstrated in Figs. 1-3.

3.1 HiSIM Generations

The HiSIM development plan is summarized in Table 1. Modeled phenomena observed for 100nm-MOSFET technologies included in HiSIM1 are summarized in Table 2. The development of HiSIM1 will be completed by the end of this March with the version HiSIM1.2, and HiSIM2 will be released as a β-version also this spring. HiSIM2 focuses on RF applications dealing with carrier response under high-speed operation. Table 3 summarizes the phenomena included in addition to HiSIM1. Figs. 4,5 demonstrate the features. In parallel, we have been developing HiSIM-SOI (Silicon-On-Insulator) for SOI-MOSFET based on the same concept as the original HiSIM. Till now the β-version of HiSIM-SOI has been proven to allow good reproduction of DC measurements and stable ring-oscillator simulations.

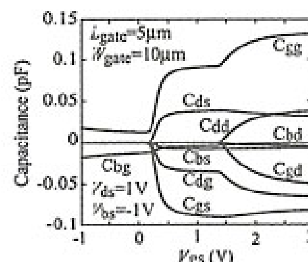

Fig. 1: Calculated of all independent intrinsic capacitances as a function of the gate voltage V_{gs}.

3.2 Towards 3D Integration

Our COE project briefly consists of two aspects: (1) Integration of electronic and optical devices, (2) Three-

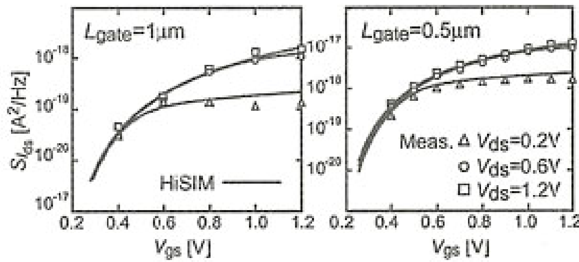

Fig. 2: Comparison of calculated $1/f$ noise at 100Hz with measurements.

dimensional integration of SOI-devices. Our role for the project is to connect technology development and its utilization for final applications, realizing concurrent rapid technology and circuit developments. Following are subjects aimed to fulfill the role:

- Modeling of optical response
- Inter-device coupling effect
- Inter-chip coupling effect

Table 1: HiSIM generations and their features.

Generations	Features
HiSIM1	100nm-MOSFET generation
HiSIM2	RF generation
HiSIM-SOI	SOI-MOSFET
HiSIM-MW	Optical Response

Table 2: Device characteristics modeled in HiSIM1.

V_{th} (L, W)	I_{bs}
Gate-Poly Depletion	I_{gate}
Quantum Mechanical Effect	I_{GIDL}
Channel-Length Modulation	**1/f Noise**
Temperature Dependences	**Capacitances**
I_{ds}	**Source/Drain Symmetry**
	Diode

4 Conclusion

The circuit simulation model HiSIM has been developed on the basis of the same concepts as 2D device simulators. Thus it can provide precise connections between technology features and circuit performance. We extend the model further to realize the 3D integration system.

References

(1) HiSIM User's Manual, STARC, 2002.

(2) M. Miura-Mattausch et al., Tech. Digest IEDM, 109, 2002.

(3) MEDICI User Manual, Synopsys, 2002.

Table 3: Device characteristics modeled in HiSIM2.

Thermal Noise
Non-quasi-static Effect
Harmonic Distortion

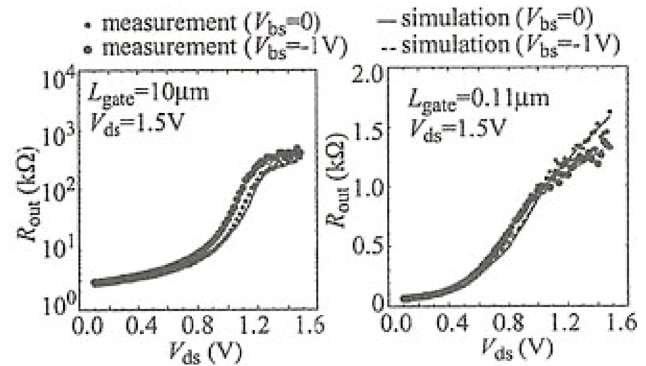

Fig. 3: Comparison of calcurated output registances with measurement.

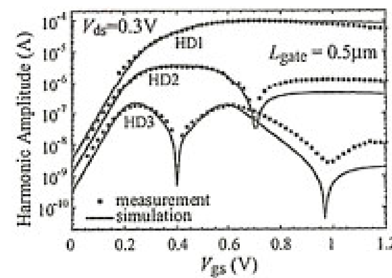

Fig. 4: Comparison of calculated harmonic amplitudes with measurements. Model parameter values used for the calculation are fitted only to measured drain current.

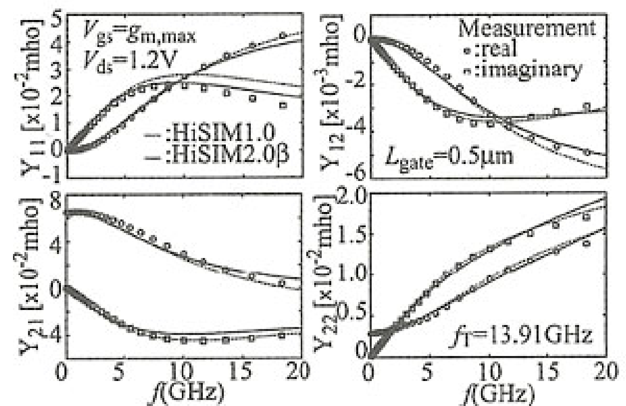

Fig. 5: Comparison of calcurated y-parameters with measurement.

HiSIM: Present Status and Future Perspectives

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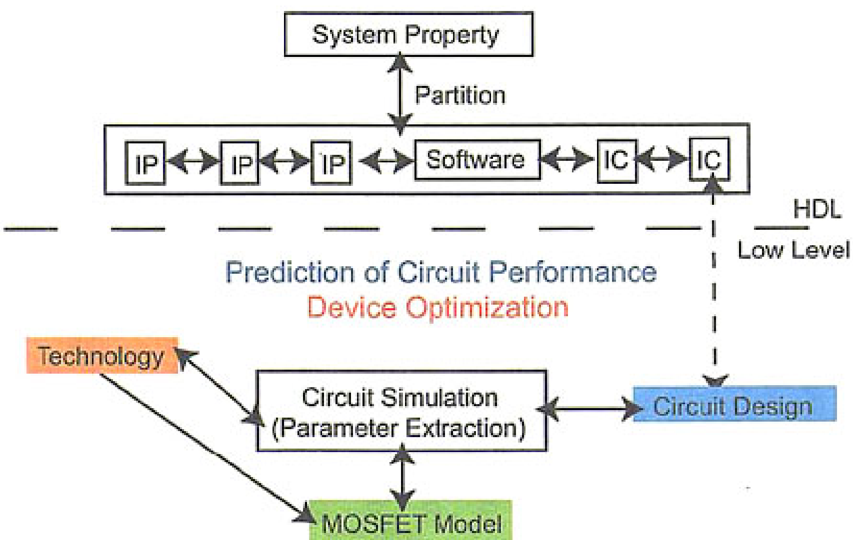
I. Introduction
II. Basic Concept of HiSIM
III. HiSIM Generations
IV. Towards 3D Integration

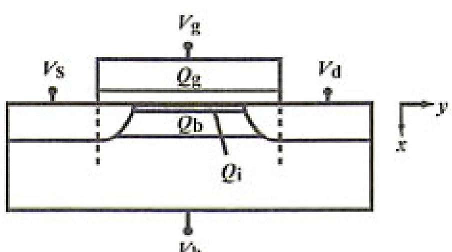
HiSIM (Hiroshima-university STARC IGFET Model)



Model Requirements

- Accurate Description of MOSFET-Characteristics
  - Charge-Based Modeling for keeping consistency among device characteristics
  - Surface-Potential-Based Modeling for realizing connection to technology
- Short Simulation Times
  - Simple Model Equations ⟷ 2D-Device Simulator
- Applicable for any Type of Advanced Technology
  - Digital, Analog, RF and Mixed-Signal Applications

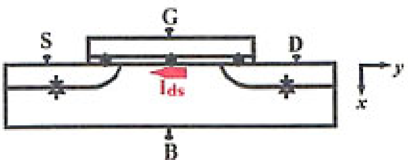
Charge-Based Model



$I_{ds} = q\frac{W}{L}\int vQ_i dy$ ⟵ Q ⟶ $C_{jk} = \frac{dQ_j}{dV_k}$

current — charge — capacitance

Conventional MOSFET Model

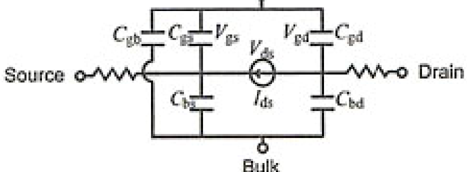


$$I_{ds} = f(V)$$

$$I_{ds} = \mu \frac{W}{L} C_{ox}\, nE$$

$$I_{ds} = \mu \frac{W}{L} C_{ox} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$ ⇨ The Pao-Sah Model

The Meyer Model



Basic Equations

-Poisson: $\nabla^2 \phi = -\frac{q}{\varepsilon_{Si}}(N_D - N_A + p - n)$

$$n = n_i \exp \frac{q(\phi - \phi_n)}{kT}$$

$$p = n_i \exp \frac{q(\phi_p - \phi)}{kT}$$

-Current Density: $j_n = q\mu_n n \frac{\phi}{y} + qD_n \nabla n$

$$j_p = q\mu_p p \frac{\phi}{y} - qD_p \nabla p$$

$q\phi$

log(I_{ds}), diffusion, drift, V_{gs}

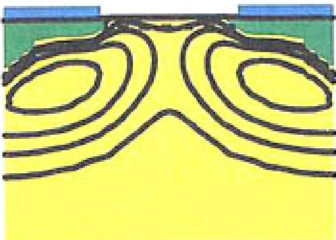
-Continuity: $\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q}\nabla j_n = 0$

$\frac{\partial p}{\partial t} = G_p - R_p + \frac{1}{q}\nabla j_p = 0$: Quasi-static Approximation

$I(t) = I_0(t) + \frac{dQ}{dt}$: Circuit Simulator

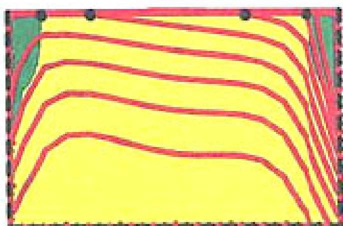
2D-Device Simulator (MEDICI)

[Impurity Profile]



Pocket Implantation

[Potential]



Impurity profile determines device performances.

Potential distribution determines device performances.

Analytical Solutions

2D → Approximations → 1D

Charge-Sheet Approximation

$\phi_S(y)$:

Charge-Sheet Approximation

Poisson's Equation:

$$Q_b(y) = -qN_{sub} \times W_d = -\sqrt{\frac{2\varepsilon_s qN_{sub}}{\beta}} \left\{\beta\left(\phi_s(y) - V_{bs}\right) - 1\right\}^{-\frac{1}{2}}; \quad \beta = \frac{q}{kT}$$

Gauss's Law:

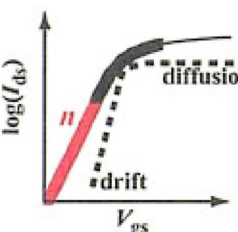
$$Q_g(y) = C_{ox}\left(V_G' - \phi_s(y)\right) \qquad ; \quad V_G' = V_{gs} - V_{fb}$$

$$Q_g(y) = -\left(Q_i(y) + Q_b(y)\right)$$

$$Q_I = W\int_0^L Q_i(y)dy; \qquad Q_B = W\int_0^L Q_b(y)dy$$

$$Q_S = W\int_0^L \left(1 - \frac{y}{L}\right)Q_i(y)dy; \qquad Q_D = W\int_0^L \frac{y}{L}Q_i(y)dy$$

Importance of Surface-Potential-Based Modeling



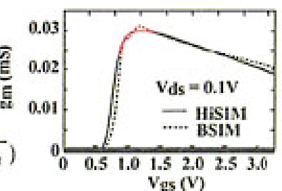
$$I_{ds}/\left(\frac{1}{\beta}\mu\frac{W}{L}\right)$$
$$= C_{ox}(1+\beta V_G')(\phi_{SL} - \phi_{S0}) - \frac{\beta}{2}C_{ox}(\phi_{SL}^2 - \phi_{S0}^2)$$
$$-\frac{2}{3}\sqrt{\frac{2\varepsilon_s qN_{sub}}{\beta}}\left[(\beta\phi_{SL}-1)^{\frac{3}{2}} - (\beta\phi_{S0}-1)^{\frac{3}{2}}\right]$$
$$+\sqrt{\frac{2\varepsilon_s qN_{sub}}{\beta}}\left[(\beta\phi_{SL}-1)^{\frac{1}{2}} - (\beta\phi_{S0}-1)^{\frac{1}{2}}\right]$$

BSIM Description:

$$V_{gseff} = \frac{2nv_t \ln\left[1 + \exp\left(\frac{V_{gs} - V_{th}}{2nv_t}\right)\right]}{1 + 2nC_{ox}\sqrt{\frac{2\Phi_B}{q\varepsilon_{si}N_{ch}}}\exp\left(-\frac{V_{gs} - V_{th} - 2V_{off}}{2nv_t}\right)}$$

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right)$$

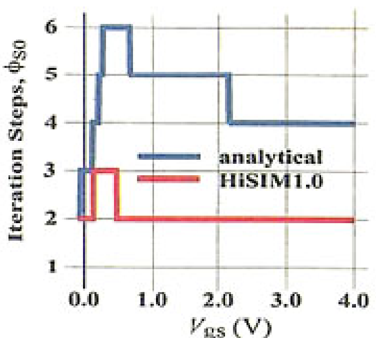
n: subthreshold swing

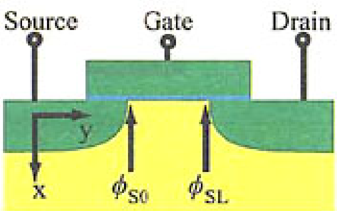


HiSIM: Surface-Potential-Based Model

- Charge-Sheet Approximation
- Gradual-Channel Approximation

ϕ_S: Solution of the 1D Poisson Eq. solved iteratively

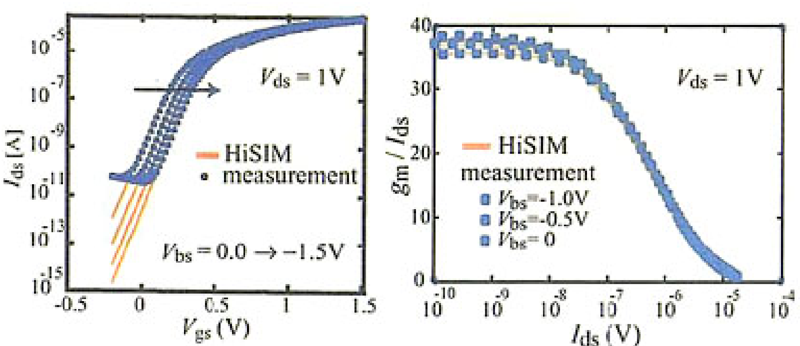




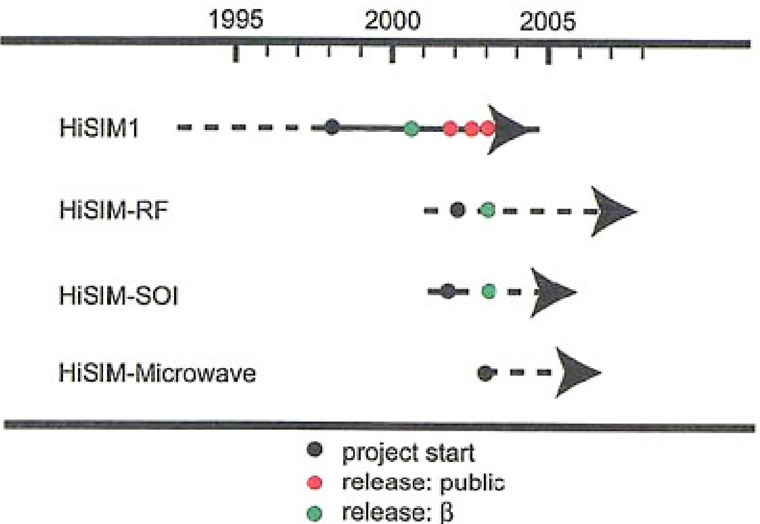
Dependent on Device Parameters (e.g. C_{ox}, N_{sub})

Simulation time: Comparable to BSIM3v3

Advantage of Surface-Potential-Based Model

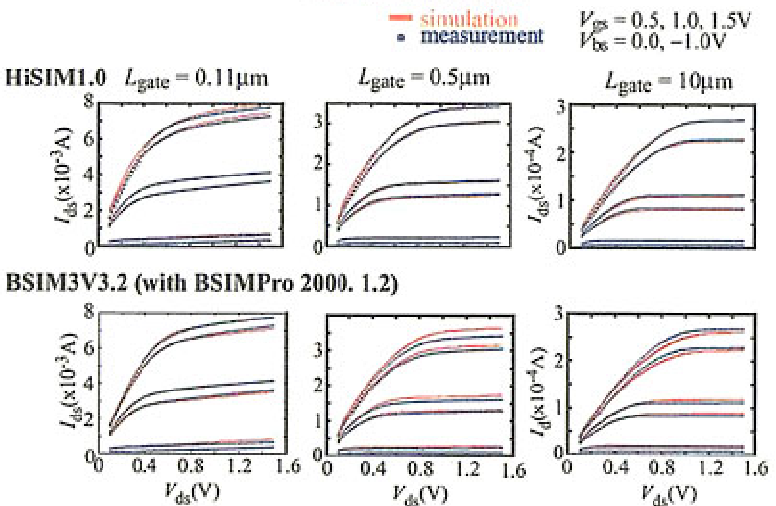


III. HiSIM Generations

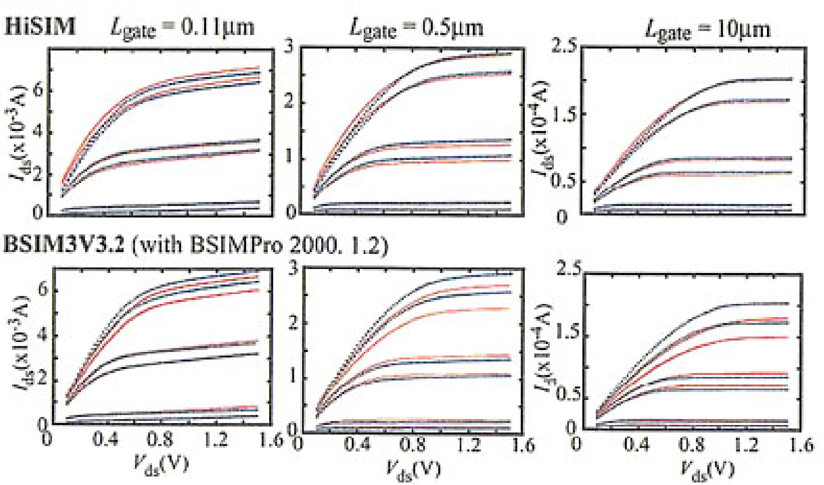


<HiSIM1>

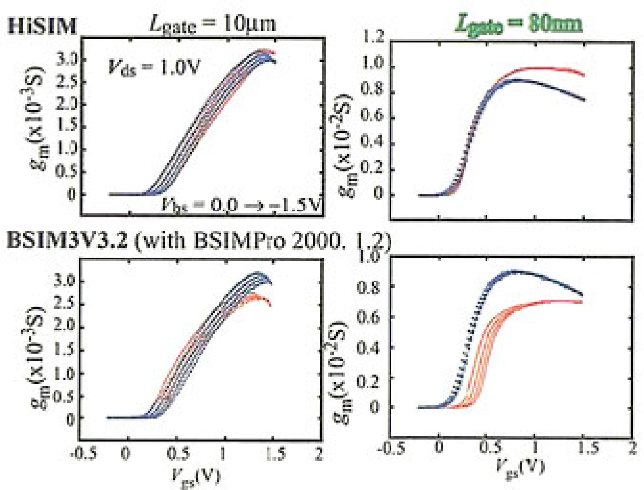
n-MOS at 300K



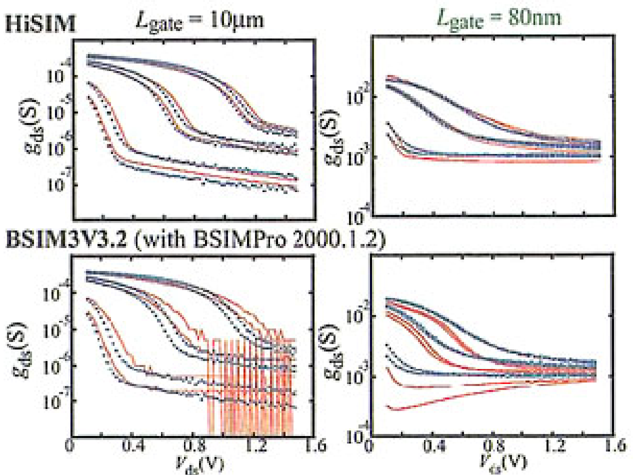
n-MOS at 363K



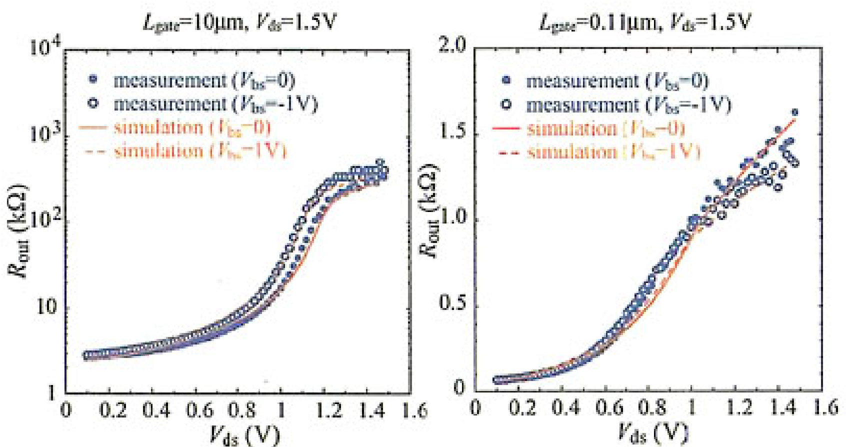
n-MOS g_m (not optimized)



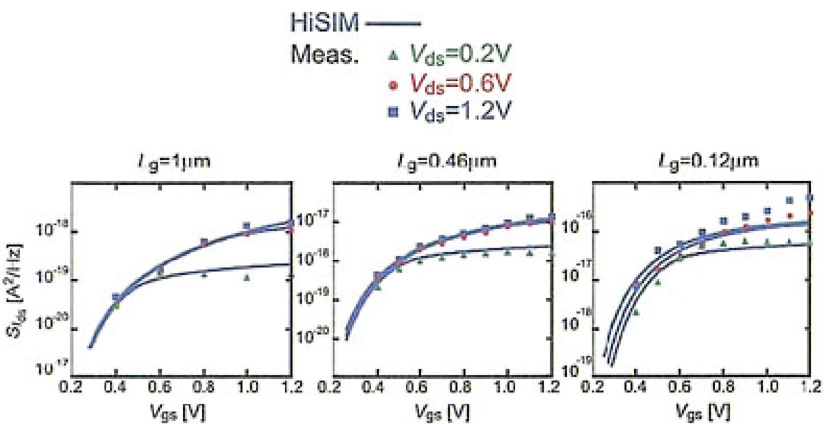
n-MOS g_{ds} (not optimized)



Output Resistance (not optimized)

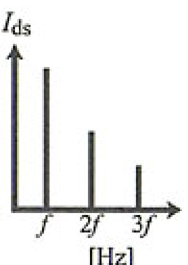


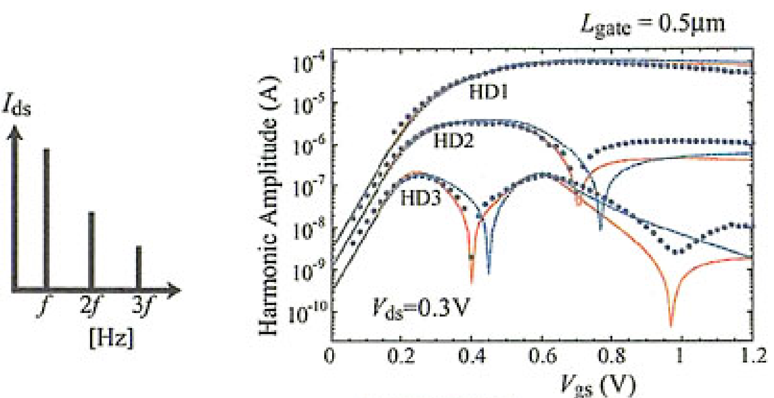
1/f-Noise



S. Matsumoto al., to be submitted for publication

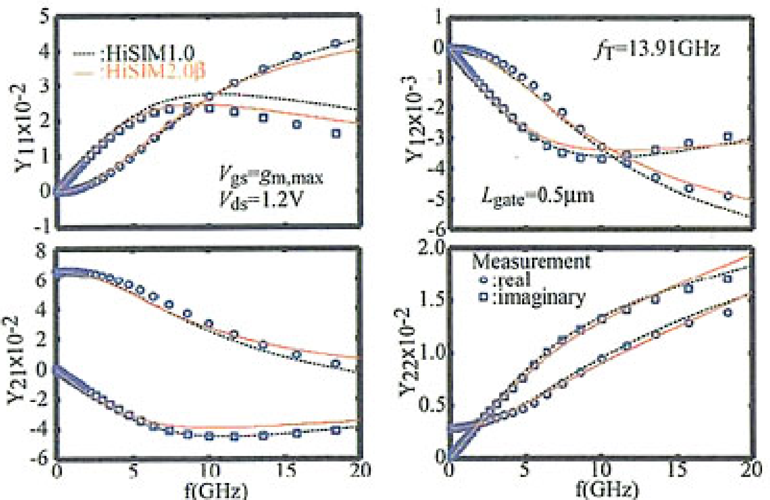
<HiSIM-RF>
Harmonic Distortion: Parameter Fine Tuning





S. Mitaniet al., to be submitted for publication

Small-Signal Analysis

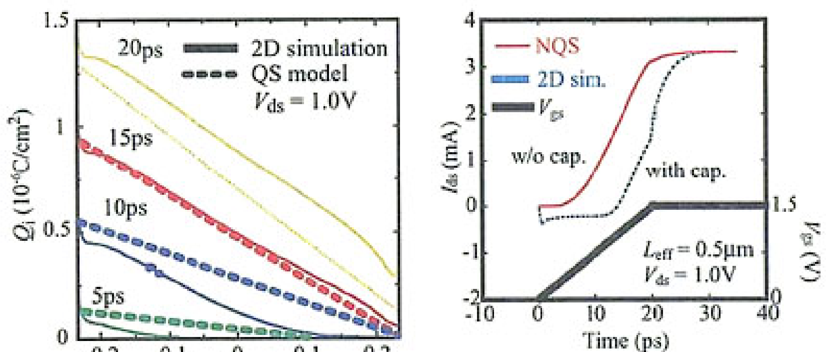


H. Kawano et al., Proc. IMS, 2002

Large-Signal Analysis

Circuit Simulator: $I(t) = I_0(t) + \frac{dQ}{dt}$

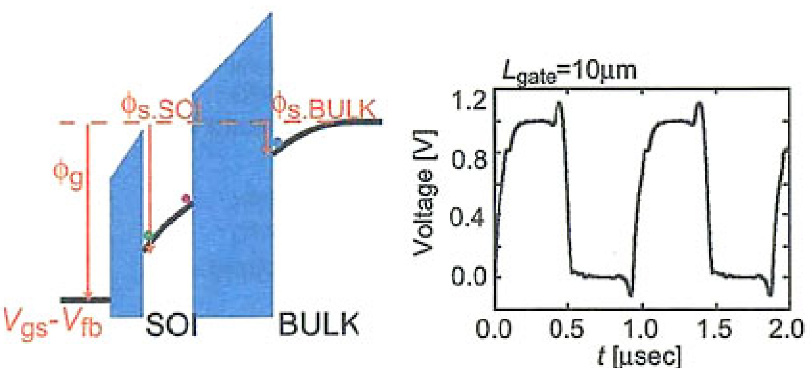
Modeling $Q(y,t)$



N. Nakayama et al., Jpn. J. Appl. Phys., April 2003.

<HiSIM-SOI>

Surface-Potential-Based Model

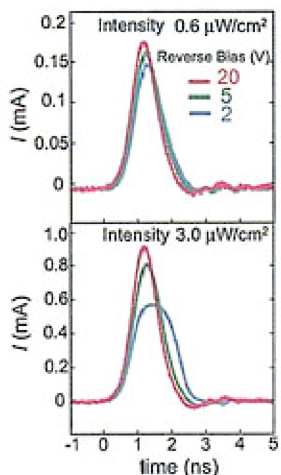


D. Kitamaru et al.
HiSIM-SOI: The First SOI-MOSFET Model for Circuit Simulation Based on the Complete Surface-Potential Description (Poster)

<HiSIM-Microwave>

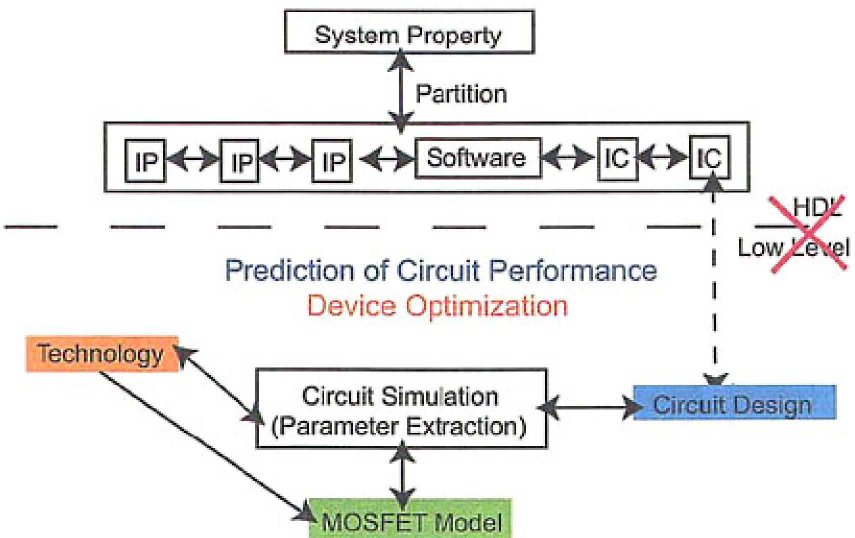
Optical Response

- Time-of-Flight Measurement
  M. Tanaka et al.
  High-Electric-Field Electron Transport at Si/SiO2 Interface Inversion Layer (Poster)
- Photo-Current Measurement



IV. Towards 3D Integration

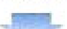
- Modeling of Optical Response
  - Delay Analysis
  - Noise Analysis
- Intra-Deivce Coupling Effect
  - Optical Leakage
  - Noise Coupling
- Inter-Chip Coupling Effect
  - Signal Integrity



Summary

HiSIM: Surface-Potential-Based Model

Connection to Technology



Prediction of Circuit Performance
Device Optimization

Towards 3D Integration

- **Modeling of Optical Reponse**
- **Intra-Device Coupling Effect**
- **Inter-Chip Coupling Effect**