Proposal of Three-Dimensional MOS Transistors with High Drivability for Area-Conscious Applications

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1. Introduction

To achieve higher performance of MOS FET, V-shaped FET [1] and vertical channel FET [2] were proposed in early 1970's however, the device scaling in planar area has only been a long lasting trend up to date except a case of trench-capacitor DRAM utilizing vertical trenches formed into silicon substrate [3]. Extending this trend, DELTA [4] and fin FET [5] have recently been proposed.

In this presentation, 3-D transistors with relatively tall beams are proposed. These are named Beam-Channel Transistor (BCT) or Corrugated-Channel Transistor (CCT) [6] after their characteristic structures which are formed vertically on silicon substrate. Figure 1 illustrates structural difference between the fin FET and the BCT. The basic concept of these 3-D transistors with increased effective-channel width is shown in Fig. 2.

2. Fabrication Processes

A key process to realize 3-D transistors with tall beams is the anisotropic etching. It is the orientation-dependent etching with TMAH (tetra methyl ammonium hydroxide) which can etch {110} at least 30-times faster than {111} resulting in crystal-flat {111} surface. Etched multi-beams are shown in Fig. 3. An obtained aspect ratio is about 17 in this case. Even if the selectivity is big enough, it rapidly gets worse with the increase in angle deviation of mask edge from the exact [112] direction. Precise control of mask-edge direction is inevitable for good reproducibility.

Another key process is to obtain narrow gate surrounding tall and steep beams. Since the conventional directional dry etching gives rise to etching residues on side walls, isotropic gate etching techniques are inevitable. This may be one of the biggest obstacles hindering very-short channel formation for 3-D transistors.

3. Device Characteristics

Thus, CCT's having 1-μm tall and 54-nm wide beams were fabricated on {110} substrate. There exists no distinguishable problem in device characteristics. It is obvious that CCT achieves almost 5 times bigger drivability, as shown in Fig. 4, than that of planar at the same planar area of 100 μm^2. When the beam density becomes higher, its commensurate device performance can be expected.

In these CCT, the effective channel length was obtained to be around 2 μm due to the lack of scalability of wet-etching with TMAH. To lessen the channel length, at least isotropic dry etching technique should be developed in submicron regime.

To obtain sub-μm gate length, isotropic dry etching was utilized for polysilicon gate films surrounding tall beams. Then, phosphorus-doped polysilicon gate was covered with its own oxide which was formed by 750C wet oxidation. Relatively low temperature wet oxidation gives strongly enhanced oxidation rate for heavily-doped silicon. In this caqse, 100-nm thick oxide was formed on polysilicon and 10-nm, on substrate. Source and drain were formed by $POCl_3$ gas source. An SEM cross-sec- tion of the transistor is shown in Fig. 5.

Drain current vs. gate voltage characteristics are shown in Fig. 6. An effective channel length of 0.7 μm was achieved for 1-μm tall, 40-nm wide beam. Sub threshold characteristics are almost satisfactory as shown in the figure.

One of the biggest problems for these thin beam transistors is parasitic source and drain resistance due to the very thin layer. Figure 7 shows one example suggesting the existence of the source and drain resistance. Silicided and/or relatively thick source and drain are essential to achieve high drivability.

4. Conclusion

A novel 3-D MOS transistor, named CCT (Corrugated-Channel Transistor), with 1-μm tall and 54-nm thick multi-beams has been realized utilizing crystal orientation anisotropic TMAH etchant on {110} silicon substrate. Realized effective channel length is 2 μm. With the increase in number of beams, drivability increases almost proportional to that number suggesting. area-conscious applications with the use of CCT.

Furthermore, a Beam-Channel Transistor with 0.7-μm effective channel length and 40-nm beam width has been achieved in 1-μm thick SOI layer. In these thin body SOI transistor, it is clarified source and drain parasitic resistance is a big obstacle for high drivability.

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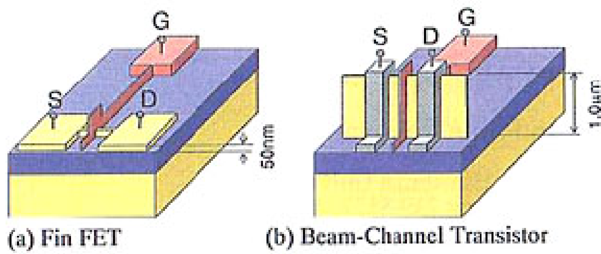

Fig. 1 Structural difference between fin FET and Beam-Channel Transistor.

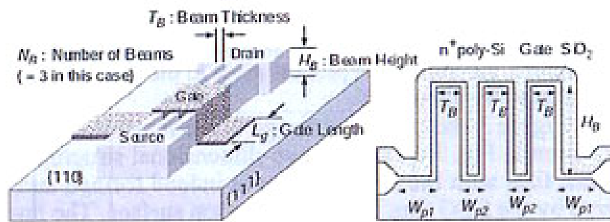

Fig. 2 A basic structure of CCT (Corrugated-Channel Transistor) and its effective-channel width increase with number of beams.

Total effective gate width, $W_{g-t} = 2W_{p1} + 2W_{p2} + 3T + 6H_B$,
Projected planar gate width, $W_{g-p} = 2W_{p1} + 2W_{p2} + 3T_B$,
thus, $W_{g-t} = W_{g-p} + 6H_B$.

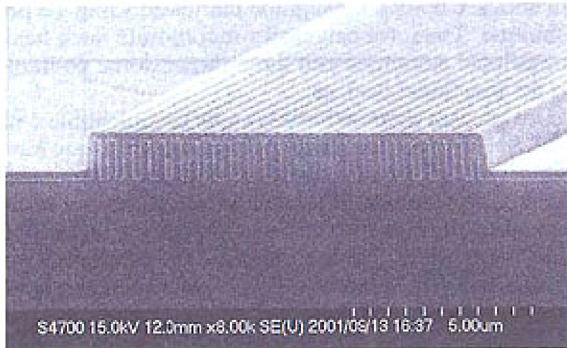

Fig. 3 Corrugated channels covered by polysilicon gate consist of 24 beams of 54 nm in thickness and 900 nm in height obtained by TMAH anisotropic wet etching.

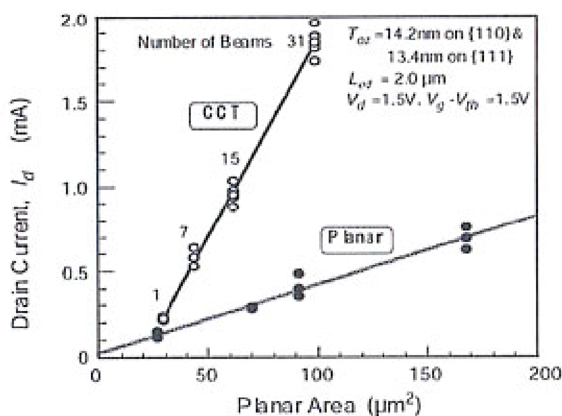

Fig. 4 Drivability increase with increasing number of beams in CCT.

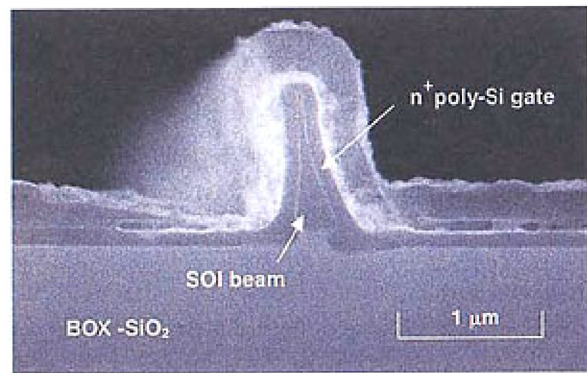

Fig. 5 An SEM cross-section of Beam-Channel Transistor with dry etched 1-µm tall beam formed on SOI substrate.

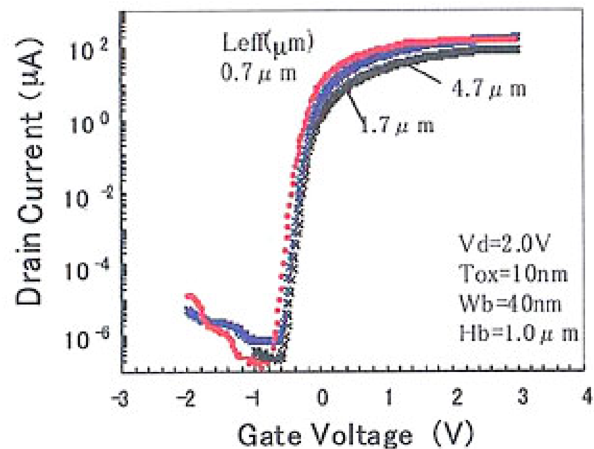

Fig. 6 Drain current vs gate voltage characteristics for 40-nm beam width SOI transistor. H_b and W_b are beam height and beam width, respectively. Subthreshold slopes are 60-70mV / decade.

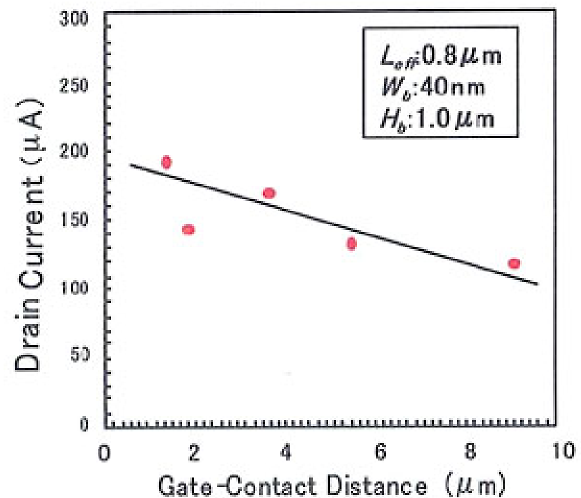

Fig. 7 Drain current decrease with the increase of gate to contact distance. This result indicates that the intrinsic transistor without source and drain resistances is evaluated to be around 200 µA.