



Hiroshima University
21st Century COE Program

**Proceedings of
First Hiroshima International Workshop on
Nanoelectronics for
Terra-Bit Information Processing**

March 17, 2003

**Hiroshima University
Faculty Club**

Preface

Recently, the Japanese Ministry of Education, Culture, Sports, Science and Technology has elected Hiroshima University as a Center of Excellence (COE) on "Nanoelectronics for Terra-Bit Information Processing" in its 21st Century COE Program. The scientific core of this COE is formed by the Research Center for Nanodevices and Systems (RCNS) and cooperating members from the Graduate School for Advanced Sciences of Matter.

The purpose of this workshop is to offer the forum for discussing future prospects of silicon nanoelectronics and nanodevice technologies with the experts in the related fields.

Our main goals are:

- * Unification of silicon-based system, circuit, device-modeling and device-fabrication research
- * Solution of the persistent 3-dimensional-integration problems by a wireless integration methodology
- * Realization of integrated systems with high-level recognition and learning capabilities by innovative circuits and architectures

Our research fields and present research subjects are summarized as follows:

I. Electronic circuits and system architecture

- I-1. High frequency analog circuits
Prof. A. Iwata & Assoc. Prof. M. Sasaki
- I-2. Associative-memory-based systems with recognition and learning capability
Prof. H. J. Mattausch & Assoc. Prof. T. Koide
- I-3. Processing system with highly cognitive level
Prof. A. Iwata

II. Device Modeling

- II-1. Integration of electronic and optical devices
Prof. M. Miura-Mattausch & Res. Assoc. Dr. H. Ueno
- II-2. Three-dimensional SOI-MOS device integration
Prof. M. Miura-Mattausch & Res. Assoc. Dr. H. Ueno

III. Nanodevices and Processes

- III-1. Fundamental miniaturization techniques for Si-MOS transistors
Assoc. Prof. K. Shibahara
- III-2. Three-dimensional ultra-small SOI-MOS transistors
Prof. H. Sunami & Prof. M. Miura-Mattausch
- III-3. Functional devices with nanostructure
Prof. S. Miyazaki & Res. Assoc. H. Murakami
- III-4. Integration technologies for wireless interconnect systems
Prof. T. Kikkawa & Assoc. Prof. M. Sasaki
- III-5. Optoelectronic integrated systems using optical interconnection on a Si chip
Prof. S. Yokoyama & Assoc. Prof. A. Nakajima



Atsushi Iwata
Leader of the 21st Century COE program on
Nanoelectronics of Tera-bit Information Processing
Director of the Research Center for Nanodevices and Systems
Hiroshima University
1-3-1 Kagamiyama, Higashi-Hiroshima 739-8530
Japan
E-mail: iwa@dsl.hiroshima-u.ac.jp

CONTENTS

9:00	Opening	
	Address	1
	Univ. President Prof. Taizo Muta	
9:05	Overview & Keynote	
	-Targets and research plan of 21st century COE-	2
	Prof. Atsushi Iwata, Hans Juergen Mattausch, Mitiko Miura-Mattausch and Hideo Sunami	
10:00	(Invited) Industry-Academia Cooperation for Advanced Semiconductor Technology	15
	Dr. Masataka Hirose (AIST, MIRAI)	
11:00	(Invited) Strategic directions of semiconductor consortia and expectation to COE program	30
	Dr. Toyoki Takemoto (STARC)	
13:30	(Invited) Challenges and opportunities in the design of future systems on chip	44
	Prof. Tobias G. Noll (Aachen Univ. of Technol.)	
14:30	(Invited) The impact of nm CMOS technology on wireless circuit and system	72
	Prof. Kwyro Lee (KAIST)	
15:30	(Invited) Silicon microphotonics - Photons meet LSIs	92
	Prof. Kazumi Wada (MIT)	
16:30	HiSIM: Present status and future perspective	102
	Prof. Mitiko Miura-Mattausch	
17:00	Poster Presentations by COE Members	
	P-1 3dimensional global/local wireless interconnection for hierarchical processing systems	111

	Atsushi Iwata and Mamoru Sasaki	
P-2	Image segmentation/extraction using nonlinear pixel-parallel networks and thier VLSI implementation	117
	Hiroshi Ando, Takashi Morie and Atsushi Iwata	
P-3	An analog VLSI chip calculating high-precision spatial and temporal derivatives of the vertebrate retina	121
	Seiji Kameda and Tetsuya Yagi	
P-4	Associative memory -based systems with recognition and learning capability	123
	Tetsushi Koide and Hans Juergen Mattausch	
P-5	Fully-parallel associative memory for fast pattern matching	129
	Yuji Yano, Minoru Honda, Masahiro Misokami, Tetsushi Koide and Hans Juergen Mattausch	
P-6	Digital-CMOS-based real-time color-motion picture segmentation	134
	Takashi Morimoto, Youmei Harada, Tetsushi Koide and Hans Juergen Mattausch	
P-7	HiSIM-SOI: The first surface-potential-based fully-depleted SOI-MOSFET model for circuit simulation development and future tasks	139
	Daisuke Kitamaru, Yasuhito Uetsuji and Mitiko Miura-Mattausch	
P-8	Electron transport in MOSFET's inversion layer under high electric field	145
	Masayasu Tanaka, Hiroaki Ueno, Osamu Matsushima and Mitiko Miura-Mattausch	
P-9	Optical interconnection technology at RCNS Hiroshima University	151
	Shin Yokoyama, Kazutaka Umeda and Anri Nakajima	
P-10	Silicon integrated antennas for wireless interconnects	158
	Takamaro Kikkawa, ABM Harun Rashid and Shinji Watanabe	

P-11	Photosensitive low-dielectric-constant films for ULSI interconnects	168
	Shin-ichiro Kuroki and Takamaro Kikkawa	
P-12	Proposal of three-dimensional MOS transistors with high drivability for area-conscious applications	174
	Hideo Sunami and Akira Katakami	
P-13	Technology and application of photonic crystal	176
	Anri Nakajima, Masaru Wake and Shin Yokoyama	
P-14	Atomic-layer deposition of ZrO₂ gate dielectrics with a Si nitride barrier layer	179
	Hiroyuki Ishii and Anri Nakajima	
P-15	Workfunction tuning technique for dual-gate CMOS with single metal gate	182
	Kentaro Shibarara	
P-16	Self-assembling of Si quantum dots and their application to memory devices	188
	Seiichi Miyazaki	
P-17	Multiple-step electron charging in Si quantum-dot floating gate MOS memories	195
	Mitsuhisa Ikeda, Yusuke Shimizu, Hideki Murakami and Seiichi Miyazaki	
P-18	Electronic charged state of single Si quantum dots with and without Ge core as detected by AFM/Kelvin probe technique	200
	Yudi Darma, Kohei Takeuchi, Hideki Murakami and Seiichi Miyazaki	
18:30	Closing Remarks	
	Prof. Hideo Sunami	