Associative-Memory-Based Systems with Recognition and Learning Capability

- Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search in Large Reference-Pattern Space -

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1. Research Target

In order to realize intelligent data processing such as feature extraction, recognition, rough judgment and learning, which are usually done in the human brain, a memory-based, flexible system architecture is necessary. The intelligent-system target requires breakthrough solutions for circuits realizing two basic functions: dense, high-interconnectivity data-storage as well as fast, low-power pattern matching. Therefore, we are developing area-efficient multi-port memories and fully-parallel mixed analog-digital associative memory architectures.

The associative-memory functionality is to find the nearest-match between an input-data word of W bit length and a number R of reference-data words. Since this functionality is a basic operation for such applications as image or voice pattern recognition [1], codebook-based data compression [2, 3, 4], routing-table-lookup for network routers, and authentication parts in security system (Fig.1), it is important to find efficient solutions for its practical realization. For the example of codebook-based image compression, shown in Fig. 1(b), the pattern of a 4 x 4 macro block of pixels is approximated by the nearest-match pattern in a codebook, storing the reference patterns of blocks typically occurring in real images as templates. Only the code-number of the best matching pattern, called winner-pattern number, is transmitted. The decompression is achieved by restoring the corresponding pattern at each location of the image from the codebook [3, 4]. Since the pattern matching is a very computationally expensive process, a hardware solution is preferable for real-time applications.

The nearest-match or winner is defined by the minimum with respect to a distance measure. Practically important distance measures are the Hamming (data strings, voice patterns, black/white pictures) and the Manhattan (gray-scale or color pictures) distance. In general, the distance measures can be represented by eq. (1),

$$D_i = \sum_{j=1}^{w} | IN_i - REF_{ij} | \qquad (1)$$

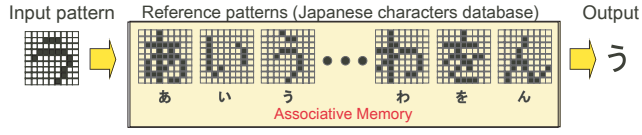
where $IN=\{IN_1, IN_2, \ldots, IN_w\}$ and $REF_i=\{REF_{i1}, REF_{i2}, \ldots, REF_{iw}\}$ are input-data and ith reference-data word, respectively. D_i is called Hamming distance, when IN and REF_i consist of 1-bit binaries, as e. g. for pixel groups from black-and-white pictures. $|IN_i - REF_{ij}|$ can be implemented with a simple EXOR gate and D_i represents the number of non-matching bits. D_i is called Manhattan distance, when IN_i and REF_i consist of n-bit ($n>1$) binaries, as e. g. for pixel groups from gray-scale or color pictures. $|IN_i - REF_{ij}|$ requires subtraction plus absolute-value function and has thus substantially higher integration complexity.

Both software and hardware solutions for the associative-memory function are possible. However, a hardware solution is preferable for applications where the search time is the major issue.

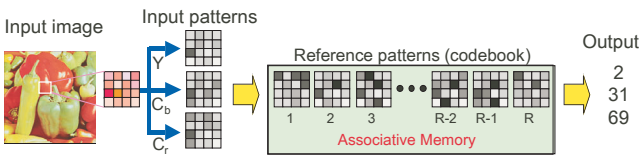
The purpose of this project is to provide a new hardware solution for the associative-memory function with the Hamming distance and the Manhattan distance measures. The solution should improve the performance of previous hardware solutions by at least 1 order of magnitude and combine short nearest-match (or winner) search times with the possibility of compact implementation in conventional CMOS circuit technology on a single chip. In particular the nearest-match circuitry should not scale with the square of number of reference words but should be only a linear function of the number of reference words.

Conventional methods for nearest distance-search have been based on: (a) analog neural networks [5], (b) SRAMs and a separate digital winner-take-all (WTA) circuit [3], (c) an analog WTA based on MOSFETs in source follower configuration [6] or a time-domain concept [7]. Problems of these solutions are: Large area-consumption [3, 5, 6] because the search circuits are of order R^2 ($O(R^2)$) or $O(R*W)$ complexity. Long search-times of about 1μs or more [3, 5]. Restricted applicability to small W [6].

To overcome these drawbacks, we have proposed a dedicated mixed analog-digital fully-parallel associative-memory architecture for nearest Hamming/Manhattan-distance search. Moreover, for the reliable handling of a large number of reference-patterns, we also have presented a bank-type associative-memory architecture as a reliable solution to the remaining issue of nearest-match search in a large reference-pattern space. Additionally, we disclose an efficient circuit for implementing the Hamming/Manhattan-distance-search function



(a) Image pattern recognition (Hamming-Distance).



(b) Codebook-based data compression (Manhattan-Distance).

Figure 1: Application examples of the associative-memory-based system. (a) pattern recognition (Hamming-distance-measure) (b) vector quantization for image compression (Mannhattan-distance measure).

within the memory field. Designed minimum Hamming/Manhattan-distance-search associative memories have high-performance at low-power dissipation.

2. Research Results

2.1 Associative-Memory Architecture for minimim Hamming/Manhattan-Distance Search

Figure 2 shows the block diagram of our proposed compact associative memory with fast fully-parallel match capability according to the Hamming/Manhattan distance. The memory part on the left side consists of conventional read/write periphery for storing the reference-data words and for reading out the nearest-match data. The search word is supplied from above, preferably on the bit-lines of the memory field, when the associative-memory function is carried out. A row of the memory field contains W storage units (SC), each which k bits plus the circuitry for unit (UC) - and word (WC) -comparison. The word-comparison results C_i are transferred to the winner-search circuit on the right side consisting of the winner-line-up amplifier (WLA) and a winner-take-all circuit (WTA). Important is the closely coupled interaction of WLA and WCs, by which the desired maximum amplification of winner-loser distances for all search cases is achieved. The output signals LA_i of the WLA are finally evaluated by the WTA to decide on the row, which contains the winner data.

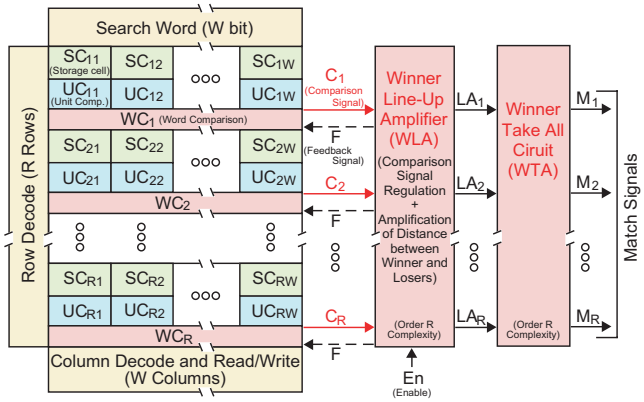


Figure 2: Block diagram of the compact-associative-memory architecture with fast fully-parallel match capability according to the Manhattan distance.

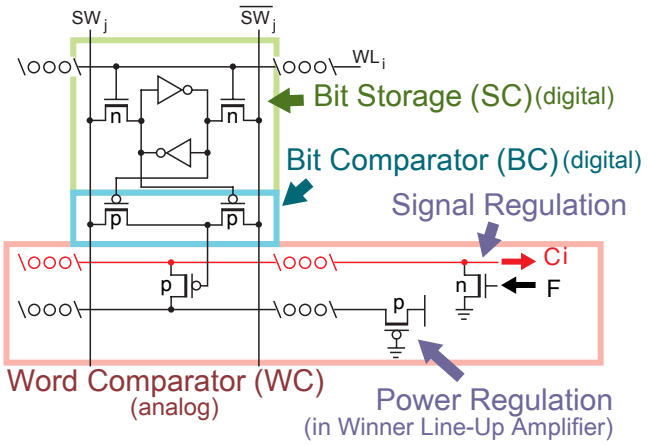


Figure 3: Architecture of the memory-field of a mixed digital/analog associative-memory for Hamming-distance search.

The concept for the memory-field for Hamming/Manhattan-distance search is illustrated in Figs. 3 and 4, respectively. For Manhattna-distance search, digital k-bit subtraction and absolute-value calculation units (UC) compare the W binaries, each with k-bit, in all rows of the memory field in parallel with the reference data. The k-bit subtraction circuit can be realized on the basis of a ripple carry adder circuit. In the test chip design, we use a newly devised compact circuit to minimize its design area. Fig. 5 shows the circuit diagram for our k-bit subtraction and absolute-value calculation unit. The transistor number of the this optimized circuit is only 20k-2. On the other hand, that of the conventional implementation needs 50k-18 transistors. So nearly 60% reduction of the transistor number can be achieved by using our newly developed circuit.

The word comparator (WC) circuit for Manhattan distance is implemented as shown in Fig. 4. To realize the WC function for Manhattan distance, the gates of the WC-transistors are connected to the corresponding k-bit output-signal lines of the unit comparator (subtractor and absolute value circuits), while their drains are connected to the corresponding output-signal line C_i. The gate width of each WC-transistor, $2^{k-1} * W_0$, varies depending on the bit position of the k-bit binary so as to distinguish each bit-weight. Since UC outputs are 0 for matching bits, WC-transistors are "off" for matching and "on" for non-matching bits. Thus small current-sink capability corre-

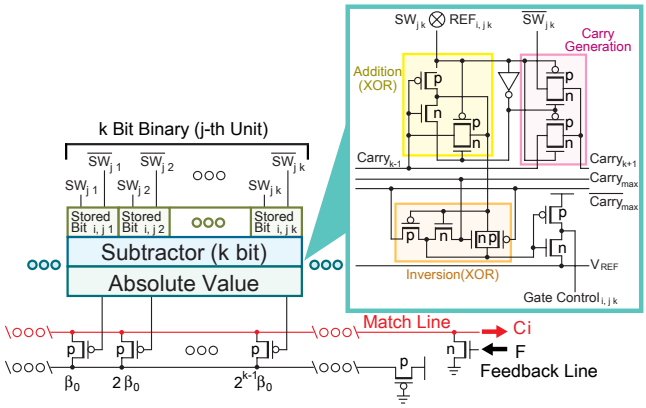


Figure 4: Architecture of the memory-field of a mixed digital/analog associative-memory for Manhattan-distance search.

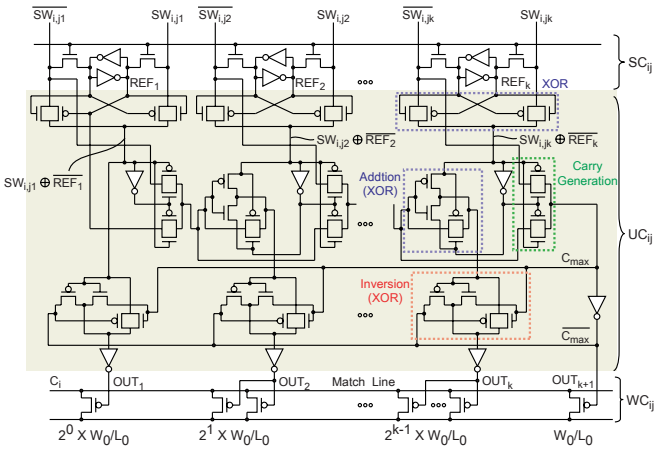


Figure 5: Newly developed circuitry for k-bit subtraction and absolute-value-calculation.

sponds to “good” matches, while large current-sink capability corresponds to “bad” matches.

Figure 6 explains the principle of self-adapting winner line-up amplification, which was implemented in an improved winner-line-up amplifier. In a previous design, the maximum gain region of the WLA was fixed and the WC output of the winner-row had to be aligned to this narrow region. This constraint limited the design freedom for the WLA quite significantly and included the danger of over- or under-regulation. In the current design, we eliminated this problem with an adaptable maximum-gain region of the WLA, which follows automatically the input voltage C_i of the winner-row. Exploiting this new design freedom leads to a drastically improved performance of the WLA. We will explain the implementation of this important new principle of a self-optimizing WLA circuit

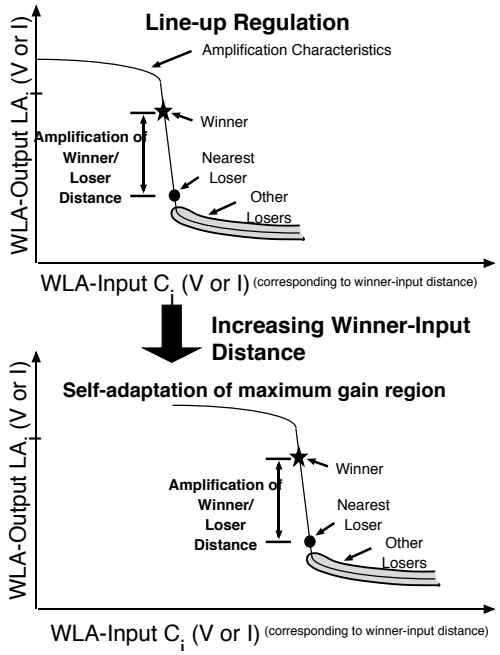


Figure 6: Selef-adapting winner line-up amplification principle. Regulation of WC outputs so that the winner-loser distance is amplified by the maximum gain follows automatically the input voltage C_i of the winner-row, that is the increasing of winner-input distance, for all possible search cases.

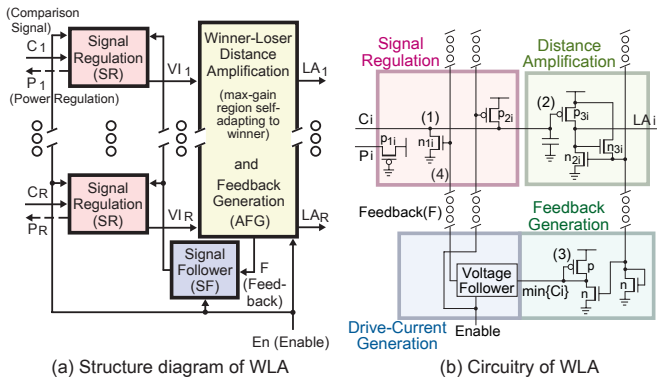


Figure 7: Winner line-up amplifier (WLA) (a) Structure diagram, (b) Circuitry of WLA with self-adapting maximum-gain region, following automatically the winner-row output C_{win} and thus eliminating the inefficient possibilities of under- or over-regulation.

in detail with Fig. 7.

First, the structure diagram of the winner-line-up amplifier (WLA) is shown in Fig. 7 (a). The WLA consists consequently of signal-regulation (SR) units for each row and a common distance-amplification/feedback-generation (AFG) unit. The feedback (F) controls the SR-units in such a way, that the generated, intermediate signal VI_{WIN} of the winner row is just within the narrow maximum-gain region of the distance amplifier in the AFG-unit. The signal follower provides the necessary high driving current for scaling to a large number of reference patterns R. We improved the WLA circuit proposed previously in [8] so as to obtain a large regulation range for feedback stabilization and relatively low power dissipation. The new WLA achieves this larger regulation range for feedback stabilization and eliminates the inefficient possibilities of under- or over-regulation by a maximum-gain region which self-adapts to the winner input C_{win}. Low power dissipation is achieved by an individual power regulation from the signal-regulation units for each input-signal source.

Fig. 7 (b) shows a circuit, which implements the new WLA according to Fig. 7 (a) in CMOS technology. The transistor-count is only 6 transistors per row, that is, O(R) complexity. A modified version of the fast minimum circuit proposed by Opris et al [9] is applied for combined feedback generation and distance amplification. The minimum function is used in the feedback loop and an intermediate node in each row circuitry is used for the distance-amplified WLA-output LA_i.

Distance amplification and self-adaptation of the maximum-gain region work as follows: Since the winner-row's WC-output C_{win} is lowest, transistor p_{3win} has the largest current-source capability, which must be balanced by the current-sink capability of transistor n_{2win}. Thus the gate voltage F_a of n_{2win}, common to all rows, has to rise appropriately and is controlled by the winner row. This in turn is only possible, if the gate voltage of the source follower n_{3win}, being also the output voltage LA_{win}, rises highest. The mechanism works independent of the absolute value of C_{win} and provides the self-adaptability of the maximum-gain region. A gain of about 20-50 over a wide range of absolute C_{win} input voltages is thus achieved. The voltage follower in Fig. 7 (b) is equivalent to the signal followers in Fig. 7 (a) and provides a sufficient driving current for scalability to large row numbers, which are necessary especially for codebook-based data-compression systems.

The WTA-circuit implemented in the test chip is depicted in Fig. 8. It is of O(R) complexity and needs just 17 transistors

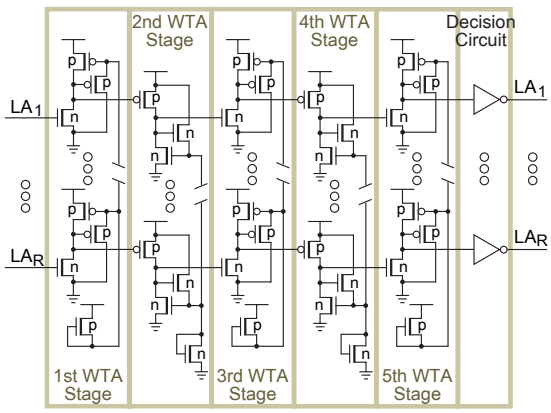


Figure 8: Winner-take-all (WTA) circuit with 17 transistors per row of the associative memory as used for the test chip.

per row. In the first design, we used 3 stages of the common-source WTA-configuration proposed by Lazzaro et al. [10], which amplify winner-loser distances by voltage-current-voltage transformations. In order to reduce the negative effects form fabrication induced miss-match of corresponding transistors in different rows and to improve the reliability for large winner-input distances, we adopt 5 stages of the common-source WTA-configuration. In the 1st stage, the current for the winner row is highest, because it has the largest WLA-output voltage. This highest current is then transformed into the lowest output-voltage of the 1st stage, while the output voltages of all other rows are substantially suppressed. The intermediate stages perform a similar voltage-current-voltage transformation and a further amplification of the winner-loser differences. The winner voltage is again lowest after the 5th stage. The final decision circuit consists of inverters with an adjusted switching threshold. It generates a "1" for the winner row and a "0" for each loser row. In this WTA-circuit, a gain of about 5 - 20 over per 1 stage is achievable.

2.2. Bank-Type Associative Memory Architecture in Large Reference-Pattern Space

The proposed bank-type associative memory architecture is shown for the case of 4 banks in Fig. 9. This system has 4 local winner-search units, implemented as banks which apply the above described fully-parallel architecture, and a global digital minimum-distance-winner selection circuit. Each local-winner is decided by fully-parallel minimum distance search in the banks in parallel. In addition to the associative memory core, each bank has a priority encoder (PE) and a circuit for digital-distance calculation of the local winner. The minimum-distance-winner selection circuit determines the global winner among the local-winners by digital calculation in a tournament-selection way and outputs the global winner's bank number as well as bank-internal address. With this bank-type approach our fully-parallel associative memory architecture can be applied to search problems in an in principle infinite space of reference patterns. For example, in the application case of code-book based vector quantization for video compression a typical code-book size is 1024 reference patterns. This could be realized with an 8-bank structure and 128 reference patterns per bank. Local winner search in each bank and global winner selection circuit could be pipelined, so that the search throughput would be determined only by the local search time of a single bank.

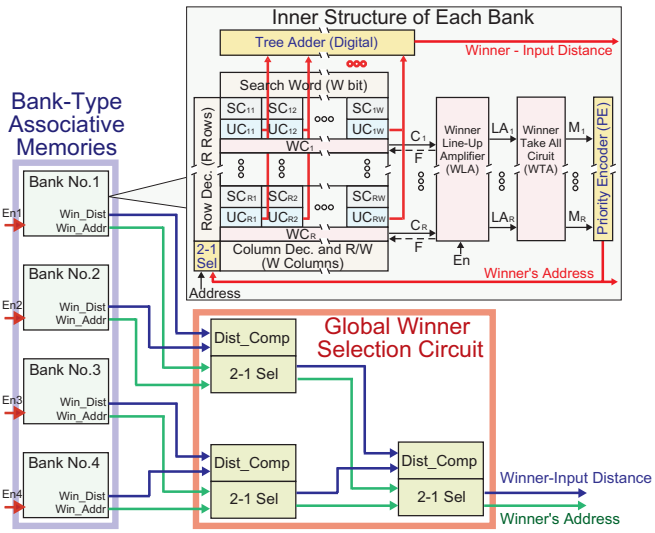


Figure 9: Bank-type associative memory architecture with fully parallel search in each bank and global winner determination by tournament search.

2.3. Chip-fabrication and Measurement Results

The Hamming-distance test chip is designed in 0.6μm CMOS with 3-metals and contains 32 reference words with 768 bit binaries (Fig. 5). Design area is 9.75mm^2 and a high performance of < 70nsec minimum distance search at low-power dissipation of 43mW are achieved. The Manhattan-distance test chip was designed in 0.35μm CMOS with 3-metal layers and contains 128 reference words with 16 binaries each 5-bit long. Fig. 6 (a) shows the photomicrograph of the fabricated Manhattan-distance test chip. Fig. 6 (b) depicts the measured average nearest-match times of this chip as a function of the distance between winner and input-data word. The data for winner to nearest-loser distances of 1 and 10 bit are plotted. Some of the chosen row combinations of winner and nearest

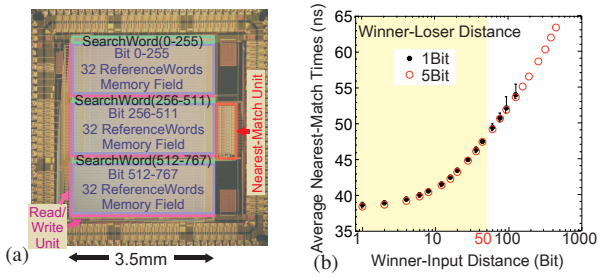


Figure 10: Minimum Hamming-distance-search associative memory. (a) chip photo (b) measured average search times

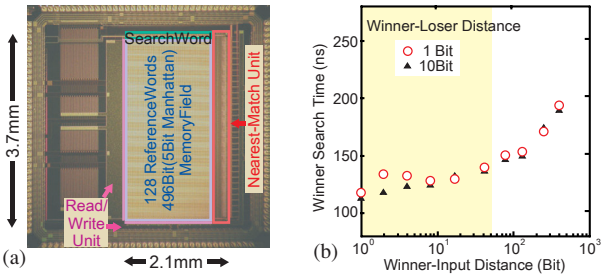


Figure 11: Minimum Manhattan-distance-search associative memory. (a) chip photo (b) measured average search times

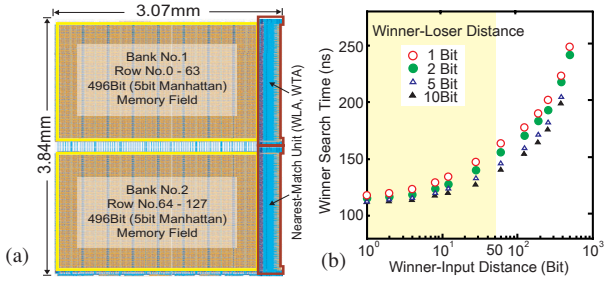


Figure12 : 2-Bank minimun Manhattan-distance search associative memory. (a) chip layout (b) simulated average search times

Table 1: Performance data of designed associative memory test chips.

Distance Measure	Hamming	Manhattan (5 bit)
Memory Field	32 x 768	128 x 80
Technology	0.6µm CMOS	0.35µm CMOS
Area	9.11 mm^2	8.6 mm^2
Search Range	0 - 400 bit	0 - 480 bit
Winner-Search Time (Measured)	< 70 nsec	< 190 nsec
Performance	1.34 TOPS	160 GOPS
Power Dissipation	43 mW	91 mW
Supply Voltage	3.3V	3.3V

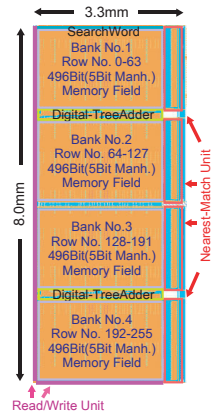


Figure 13: Layout image of the 4-bank, 256 reference-pattern Manhattan-distance- search memory.

Table 2: Characteristics of the bank-type Manhattan-distance associative memories.

Distance Measure	Manhattan (5 bit)	
	2-Bank	4-Bank
Reference Number	128 (64 x 2)	256 (64 x 4)
Design Area	11.8mm^2	26.5mm^2
Search Unit Area	0.99mm^2	1.97mm^2
Search Range	0 - 496bit	0 - 496bit
Winner-Search Time (Simulation)	< 260nsec	< 280nsec
Power Dissipation (Simulation)	< 330mW	< 640mW
Performance	128 GOPS	229 GOPS
Technology	0.35µm 3-metal CMOS	0.35µm 3-metal CMOS
Supply Voltage	3.3V	3.3V

loser delivered unreliable match results for large winner-input distance. However, this causes no practical problem because vector-quantization (VQ) simulations of real images confirmed that almost all winner-input distances are less than 50bit. In the practical case with optimized codebook winner patterns with larger winner-input distance are in general expected to be very seldom. Therefore, the measured performance of the designed test-chip is already sufficient for VQ application with a nearest match time < 140nsec. Taking into account that the area for the input-pattern circuit remains the same, we extrapolate an area of about 17.2mm^2 and a power-dissipation of about 180mW for a nearest Manhattan-distance-search memory with 256 reference patterns in 0.35µm CMOS technology. If we furthermore extrapolate the test-chip data to a state-of-the-art 0.13µm CMOS technology with 1.2V power-supply, we expect an integration area of about 6.4 mm^2 and a power dissipation of about 71.7mW. Table 1 shows the data of fabricated test chips for minimum Hamming/Manhattan distance search.

Multi-bank associative memories have been also designed in 0.35µm CMOS technology. Fig. 7 (a) shows the layout of a 2-bank associative memory for minimum Manhattan-distance search with 128 reference pattern number. Fig. 7 (b) depicts the simulated average nearest-match times of this layout, indicating that high-speed search time can be expected. The layout of a 4-bank associative memory with 256 reference patterns is shown in Fig. 8 and the photomicrograph of the fabricated chip is shown in Fig. 9. Table 2 summarizes performance data of designed 2 and 4 bank associative memories. In addition to the scalability of the bank number N, the introduction of a bank-selective activation methodology can reduce the power dissipation of the whole chip. This is in particular useful if the reference-pattern space can be categorized, so that the bank (or banks) which must contain the winner can be identified in a preprocessing step. Consequently, only 1 bank has to be activated for local winner search in the best case, reducing the power dissipation by approximately a factor 1/N.

3. Conclusion

Associative memory architecture for fully-parallel minimum distance search is proposed and test chips are designed in 0.6µm (Hamming) and in 0.35µm (Manhattan) CMOS technologies. The 9.75mm^2 Hamming test-chip with 32 reference patterns and 768 equivalent bit per pattern, has a performance of < 70nsec nearest-match time, equivalent to a 32bit computer with 150GOPS/mm^2, at a power dissipation of 43mW. The 8.6mm^2 Manhattan test-chip with 128 reference patterns and 496 equivalent bit per pattern, has a performance of < 190nsec nearest-match time, equivalent to a 32bit computer with 20GOPS/mm^2, at a power dissipation of 91mW. These data are sufficient for application in high-performance mobile real-time systems such as systems for image compression by vector-quantization.

Moreover, a bank-type associative memory architecture for fully-parallel minimum distance search is presented and verified by test chips in 0.35µm CMOS technology. The proposed architecture extends the possibility of fully-parallel nearest-match search to an in principle infinite space of reference patterns. Designed 1-, 2- and 4-bank test chips in 0.35µm CMOS verify nearest-match times below 280nsec, a performance between 120GOPS and 230GOPS, and a power dissipation between 90mW and 150mW per bank. For search problems with categorizable reference-data space the power dissipation can be reduced to the value for one bank in the best case. These data are sufficient for application in high-performance mobile real-time systems such as image-compression systems by vector-quantization.

4. Future Plan

Although search time and power dissipation are already very competitive in comparison to other associative-memory solutions, we are planning to further improve the performance of the WLA circuit with a current-comparator-based structure. Search times below 100ns per bank and at the same time a power dissipation below 100mW are expected to be possible. Since a further very important distance measure, the Euclid distance, is very popular in many high-level architectures for realizing artificial intelligent systems, we plan also to extend our Manhattan-distance-search architecture to enable nearest Euclid-distance search.

Acknowledgment
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4. Published Papers and Patents

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