Optimized Mixed Digital-Analog Nearest-Match Circuit for Fully-Parallel Associative Memories

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1. Research Target

A basic operation of pattern recognition is to find the nearest match between an input-data word of W bit length and a number R of reference-data words [1]. For fast and efficient integration of the nearest-match function a fully-parallel associative-memory has been proposed recently [2]. In this fully-parallel associative memory, the search time is primarily determined by the performance of a circuit called winner-line-up amplifier (WLA). The prime goal of the WLA circuitry is to amplify the distance between the winner and the nearest-loser sufficiently so that the following winner-take-all (WTA) circuit can decide the winner at binary logic level. Because of the internal capacitances and resistances in the MOS transistors, there is an inherent delay and the WLA needs considerable time to set at the stable operating point. Moreover, due to use of feedback loop, the WLA is prune to instability and oscillations at higher amplification.

In order to keep the average power of the whole network reasonably low, the current for the mismatched bits should be as low as possible (fraction of μA only). The WLA primarily intends to magnify the distance in the narrow range of the winner and the nearest-loser. For this purpose, the WLA has to operate relatively at higher gain for the winner and nearest-loser. A feedback loop is added in the WLA network that regulates the ml and sets the desired operating point. The feedback regulation has to be done properly, as both under-regulation and over-regulation deteriorates the network performance [2].

The task of this research project is a further improvement of the mixed digital-analog nearest-match circuitry of the fully-parallel associative memory, in particular the WLA, with respect to reduced search time and power dissipation, while maintaining sufficient stability during the search operation.

2. Research Results

2.1 WLA Network with Parallel Capacitances in Match Lines

The presently used WLA is shown in Fig. 1 [3]. A pre-charge transistor MP_{ia} is added in each match line (ml), otherwise, the network will not be able to make a fast decision because of the possibility of different initial voltages on the ml. The transistors MP_{ia} charge ml to

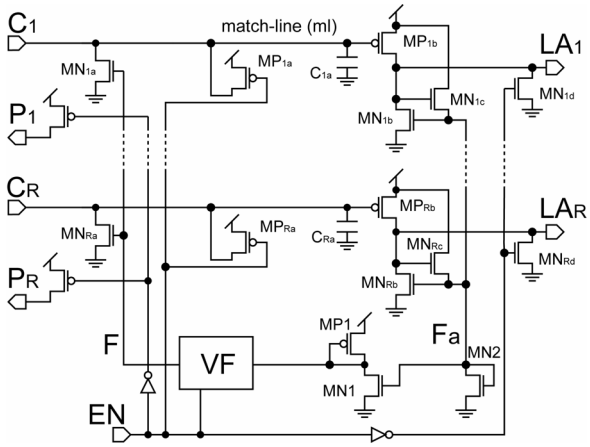

Fig. 1 WLA circuit (WLA-A) with capacitors in the match lines.

V_{DD} as the enable signal (**EN**) goes low. In the evaluation period with **EN** = HIGH, the transistors MP_{ia} turn off and the capacitances discharge through the transistors MN_{ia} controlled by the feedback loop.

2.2 Improved WLA Circuitry for Search Speed Enhancement

From Fig. 1, it is evident that the distance amplification part of the WLA-A network cannot start immediately at the positive edge of **EN**, rather, it has to wait until the capacitance voltage falls to the threshold voltage V_{th} of the transistors MP_{ib}. The search speed of the WLA-A is expected to improve by adding separate

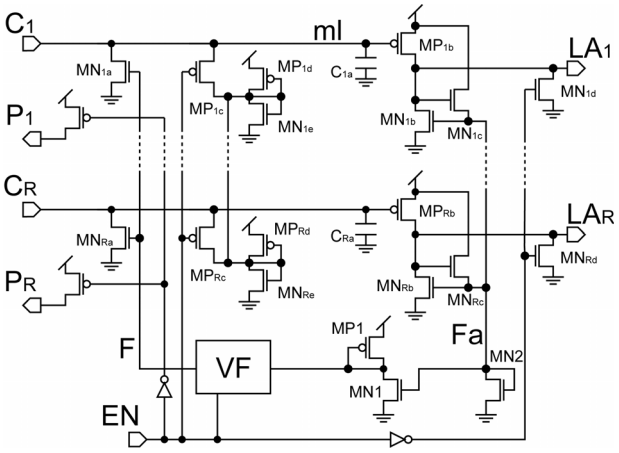

Fig. 2 WLA circuit (WLA-B) with match line pre-charged to V_{DD}-V_{th}.

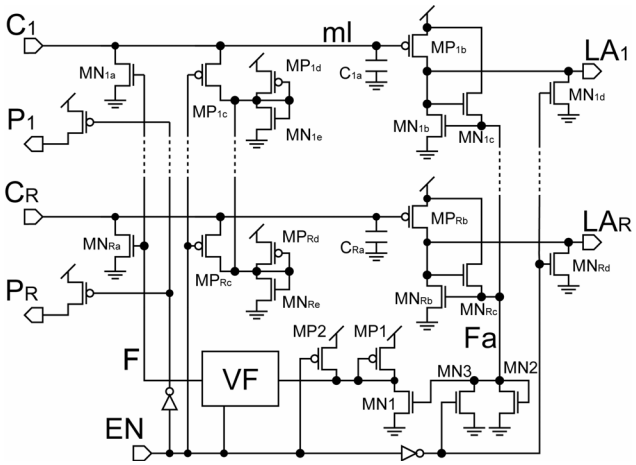

Fig. 3 Reset transistors added in the feedback path in WLA-C network to ensure same initial conditions for all searches.

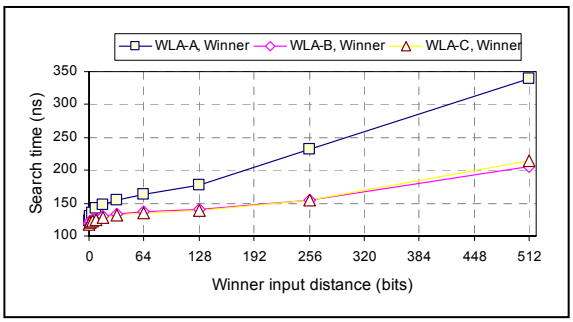

Fig. 4 Winner search times for the nearest-loser set at 1-bit apart while other-losers set at 21-bit distance.

charging sources in each ml as shown in Fig. 2. Each charging source has a pull-up diode MP_{id} connected to a pull-down diode MN_{ie}. It supplies a voltage of V_{DD}-V_{th} to the charging transistors MP_{ic} of the ml. The charging circuit parameters are adjusted to have a current drain of 3.1 µA for each ml.

For both WLA-A and WLA-B circuits, the feedback line voltage (gate voltage of MN_1) may have some residual charges whose magnitude differs at different pre-search conditions. Although it does not have significant impact on the search result, it improves search reliability to have same initial conditions in all parts of the WLA network before a search starts. A reset transistor MN_3 added in the feedback path as shown in Fig. 3, discharges residual charges thus forcing the feedback line to start from the same initial condition for all new searches. The three WLA versions (WLA-A, WLA-B and WLA-C) are compared in an 350 nm CMOS technology for an associative memory with Hamming

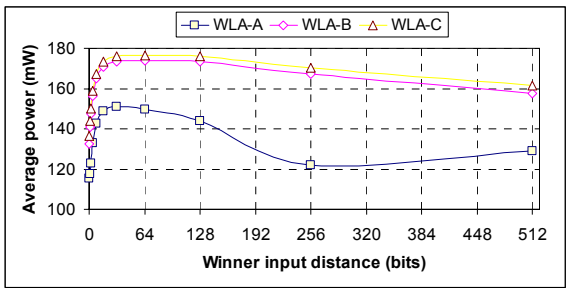

Fig. 5 Power consumption for the nearest-loser set at 1-bit apart while other-losers set at 21-bit distance.

distance search strategy having standard WTA circuits [4] in the output stage and 128 reference patterns with 512 bit length each.

Search results for the associative memory with the nearest-loser set at the most difficult 1-bit distance and all other-losers at 21-bit apart are shown in Fig. 4. The search-time reduction with WLA-B is about 37% to less then 180ns. The additional reduction with WLA-C is less than 1%. The cost of the shorter search times in terms of increased power dissipation is depicted in Fig. 5. Circuit WLA-B increases maximum average power dissipation by about 14% while circuit WLA-C adds about another 1%.

3. Conclusion

The most effective improvement of the WLA circuit in the fully-parallel associative memory was a changed pre-charging of the match-lines from V_{DD} to $V_{DD} - V_{th}$. The resulting reduction of the maximum search time was about 37% at the cost of only 17% increased power dissipation. Pre-charging of the internal nodes of the feedback loop was less effective, leading only to an additional improvement of 1%.

4. Future Plan

Kaji Mujibur Rahman finished his work as a COE researcher in April 2004 and returned Bangladesh University of Engineering and Technology. He is planning to continue cooperation with the COE and his research work on improved nearest-match circuits for the fully-parallel associative memories in Bangladesh. One important idea for a further reduced search time at even lower power dissipation is the application of a WLA circuit based on match-line-current comparators.

References

[1] D. R. Tveter, The Pattern Recognition Basis of Artificial Intelligence, Los Alamitos, CA: IEEE Computer Society, 1998.
[2] H.J. Mattausch et al., IEEE J. Solid-State Circuits, vol. 37, pp.218-227, 2002.
[3] H.J. Mattausch et al., Symposium on VLSI Circuits, pp. 252-255, 2002.
[4] J. Lazzaro et al., in Advances in Neural Information Processing Systems, I.D.S. Touretzky Ed., San Mateo, CA: Morgan Kaufmann, 1989.

3. Published Papers and Patents

① Proceedings

1. K. M. Rahman, K. Kamimura, T. Koide and H. J. Mattausch, "Improved Mixed Digital-Analog-Match Circuit for Fully-Parallel Associative Memories," Second Hiroshima International Workshop on Namoelectronics for Terra-Bit Information Processing, pp. 40-41, 2004.

2. K. Kamimura, K. M. Rahman, T. Koide and H. J. Mattausch, "Optimized Multi-stage Minimum-Distance-Search Circuit with Feedback Stabilization for Fully-Parallel Associative Memories" Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2004), in press, 2004.