Development of Digital-CMOS-Based Real-Time Color-Motion Picture Segmentation Architecture and its LSI Chip Verification

Takashi Morimoto (Graduate School of Advanced Sciences of Matter, D1),
Tetsushi Koide (Assoc. Prof., Research Center for Nanodevices and Systems,
Graduate School of Advanced Sciences of Matter),
Hans Jürgen Mattausch (Prof., Research Center for Nanodeivices and Systems,
Graduate School of Advanced Sciences of Matter)

1. Research Target

Image segmentation is the extraction process of all objects from natural input images and is the necessary first step of object-oriented image processing such as object recognition or object tracking. However, conventional gray-scale and color image segmentation algorithm are implemented in software with general purpose or digital-signal processors resulting in relatively large size, large power dissipation, and high cost for application hardware.

Objective of this research is the proposals of a hardware-oriented segmentation algorithm and it's digital CMOS implementation.

2. Research Results

We propose a highly-parallel digital algorithm for gray-scale/color image segmentation of real-time video signals and a cell-network based implementation architecture in state-of-the-art CMOS technology. The segmentation algorithm uses a region-growing approach, which can be viewed as a simplified digital version of a locally-excitatory globally-inhibitory oscillator network (LEGION). Color and gray-scale picture segmentation differ only in the expressions for the connection-weight calculation between the network cells. Fig. 1 shows an explanation of our segmentation algorithm with 3×3 gray-scale example image. The proposed VLSI implementation architecture (Fig. 2) based on a digital-algorithm consists of 4 functional stages for connection-weight calculation, leader-cell determination, image segmentation and segmentation-result restoring, respectively. The image-segmentation network, which is the core of the proposed architecture, consists of cells (Fig. 3) and connection-weight registers (Fig. 4). Each cell represents a pixel of the original picture. In this network, the self-excitation and excitation steps of the algorithm of Fig. 1 are carried out for all pixels of the picture in parallel. As shown in Fig. 5, the complete cell network can be implemented by alternately laying a cell, corresponding to a pixel, and a horizontal or vertical connection-weight register block. Thus the connection weights can be efficiently shared among neighboring cells, and the wiring length and circuit area can be minimized. Since the cell structure becomes simple and compact, high speed and high density implementation is achieved.

The test-chip of Fig. 6 for the cell-network core was designed in 0.35μm, 3 metal CMOS technology. Decoder and adder/subtractor of the network cells, which consume the largest area portion, were designed in full-custom. An integration density of 19.6 pixels/mm^2 was thus achieved. We have also estimated the possible pixel density for full-custom high-speed (Fig. 3a) and high-density (Fig. 3b) designs in scaled-down CMOS technologies, assuming just 3-metal layers. From this data we expect a one-chip integration of the proposed architecture for 300×300 pixel pictures at the 100nm technology node and for 800×600 pixel pictures at the 50nm technology node.

3. Relationship with COE Program

The research on this subject is indispensable for a "Real-Time Image Recognition System", which is one of the important COE research tasks.

4. Summary and Future Work

A real-time image segmentation for gray-scale and color images is developed. From our present results, VGA size video segmentation is expected to become possible in 50nm CMOS technology.

The future research work is concerned with the development and verification of new algorithm, which will enable low-power real-time image segmentation hardware for VGA-size (640×480) video data.

5. Published Papers and Patents

① Published Papers

1. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Efficient video-picture segmentation algorithm for cell-network-based digital CMOS implementation," IEICE Trans. on Info. & Sys., Vol.E87-D (2) (2004) pp. 500-503.

② Proceedings

1. T. Koide, T. Morimoto, Y. Harada, and H. J. Mattausch, "Digital gray-scale/color image-segmentation architecture for cell-network-based real-time applications," Proc. of The 2002 Int'l Tech. Conf. on Cir. & Sys., Computers. and Communications (ITC-CSCC2002) (2002) pp. 670 -673.
2. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Real-time segmentation architecture of gray-scale/color motion pictures and digital test-chip implementation," Proc. of The 2002 IEEE Asia-Pacific Conf. on ASICs (AP-ASIC2002) (2002) pp. 237-240.
3. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Low-complexity, highly-parallel color motion-picture segmentation architecture for compact digital CMOS implementation," Ext. Abs. of the 2002 Int'l Conf. on Solid State Devices and Materials (SSDM2002) (2002) pp. 242-243.
4. Y. Harada, T. Morimoto, T. Koide, and H. J. Mattausch, "CMOS test chip for a high-speed digital image-segmentation architecture with pixel-parallel processing," Proc. of The 2003 Int'l Tech. Conf. on Cir. & Sys., Computers. and Communications (ITC-CSCC 2003) (2003) pp. 284-287.
5. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Low-power real-time region-growing image- segmenta-

tion in 0.35μm CMOS due to subdivided-image and boundary-active-only architectures," Ext. Abs. of the 2003 Int'l Conf. on Solid State Devices and Materials (SSDM2003) (2003) pp. 146-147.
6. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "350nm CMOS test-chip for architecture verification of real-time QVGA color-video segmentation at the 90nm technology node," Proc. of the Asia South Pacific Design Automation Conf. 2004 (ASP-DAC2004) (2004) pp. 531-532.

③ Patents

1. "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus", JPN Patent Application No. 2002-152491, (2002.05.27).
2. "Image segmentation method, image segmentation apparatus, image processing method, and image processing apparatus", USA Patent Application No.10/445,247 (2003.05.26), EPC Patent Application No.03011840.0 (2003.05.26),KOR Patent Application No.2003-33324 (2003.05.26), TWN Patent Application No.92114142 (2003.05.26).

④ Awards

1. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "A real-time picture-segmentation archictecture for intelligent information processing, " 4th LSI IP Design Award, Development Encouragement Award, LSI IP Design Award Committee, 2002.5. URL http://ne.nikkeibp.co.jp/award/
2. T. Morimoto, "Research for Real-Time Image Segmentation Architecture and its Digital-CMOS Implementation," Hiroshima University Student Award, President of Hiroshima University, Taizou Muta, No. 1-0061, 2003.3.

⑤ Others

1. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "Gray-scale/color image-segmentation architecture based on cell-network," Technical report of IEICE, VLD2002-48 (2002) pp. 49-54, in Japanese.
2. T. Morimoto, Y. Harada, T. Koide, and H. J. Mattausch, "A cell-network-based image segmentation LSI for rel-time applications," The 5th IEEE Hiroshima Student Symposium (HISS) (2002) pp. 221-224, in Japanese.

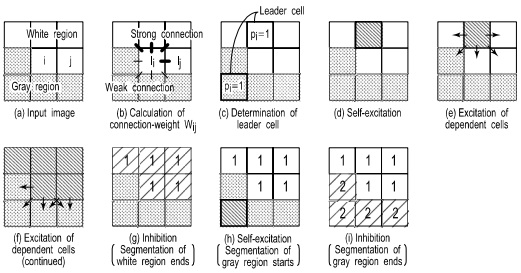

Fig.1 Explanation of our segmentation algorithm with 3×3 gray-scale example image.

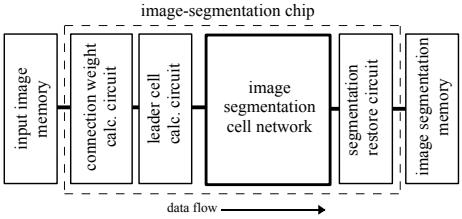

Fig.2 Block diagram of the proposed architecture.

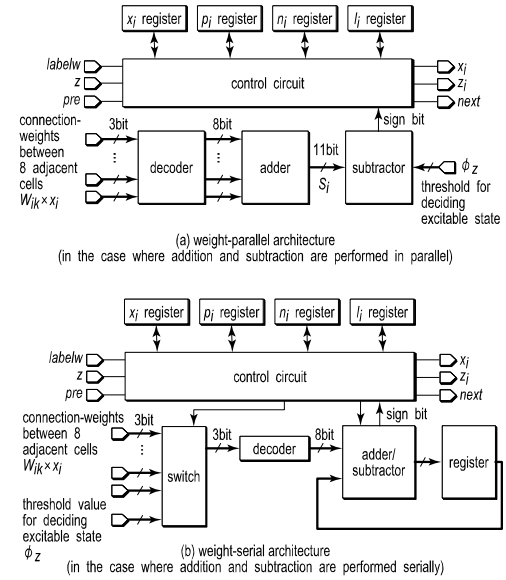

Fig.3 Structure diagram of the network cell.

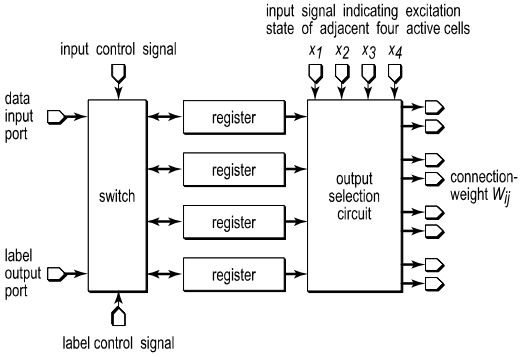

Fig.4 Structure diagram of a connection-weight-register block.

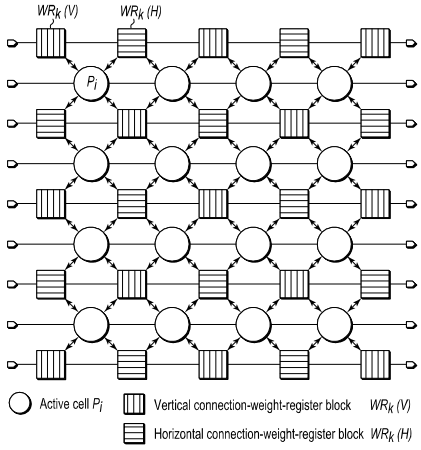

Fig.5 Block diagram of the cell-network construction for 4×4 pixels.

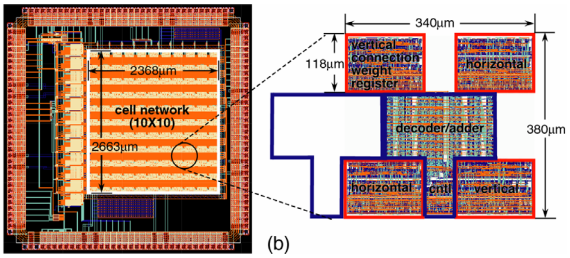

Fig.6 The layout of the test-chip with 0.35μm 3-metal layer CMOS technology.