Workfunction Tuning for Single-Metal Dual-Gate CMOS

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1. Research Target

Dual-workfunction gates with single metal are expected to replace dual-poly-Si gates that accompanies a depletion effect problem. Our target is finding flexible metal-gate workfunction-tuning technology that is applicable to CMOS fabrication maintaining compatibility to conventional CMOS fabrication process.

2. Research Results

Original workfunction tuning of Mo was achieved by nitrogen implantation [1], however, this method causes interface and oxide damage. To avoid the damage problem,nitrogen diffusion from TiN deposited on Mo was attempted. Though expected V_{th} shift due to the N diffusion was 0.45 V that is equal to V_{FB} shift of MOS diodes, the V_{th} shift of fabricated MOSFETs was 0.1 V, as shown in Fig. 1. Nitrogen depth profiles in Mo MOS structure was evaluated to discuss reason why the V_{th} shift was shrunk (Fig. 2). N pileup at the Mo/SiO_2 interface for the diode process reduces by adding source and drain (S/D) activation annealing, in other words, by changing fabrication process to FET process. Nitrogen concentration in Mo was also decreased by the annealing. These results indicate that the nitrogen pileup reduction due to the nitrogen out-diffusion through a Mo film is the origin of reversible workfunction behavior. In the case of the fabricated MOSFETs, Mo gates are surrounded by CVD grown SiO_2 during the S/D activation annealing. N atoms located at the Mo/gate SiO_2 interface are considered to redistribute to other CVD SiO_2 interfaces, as shown in Fig. 3. Based on these results we have modified nitrogen diffusion process to be combined with S/D activation annealing by maintaining a TiN/Mo stack structure to cover the Mo top interface with diffusion source TiN. As a result, the V_{th} shift value was improved, as shown in Fig.4. However, Fig. 4 shows anomalous V_{th} increase behavior for modified devices against the gate length. The Vth increase is attributable to nitrogen reduction at the Mo bottom interface in the short channel devices. Around the gate edge region, some of nitrogen atoms supplied from TiN go to the bottom interface and others go to the side interface. Therefore, nitrogen concentration at the bottom interface around the gate edge is lower than that

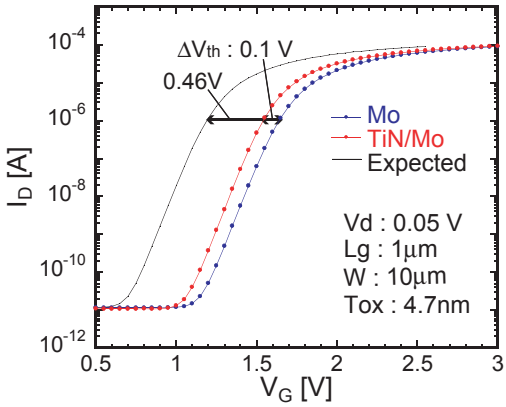

Fig. 1 I_D-V_G characteristics of TiN/Mo and Mo gate MOSFETs. Vth shift due to workfunction change is smaller than the value expected from VFB obtained with MOS diodes.

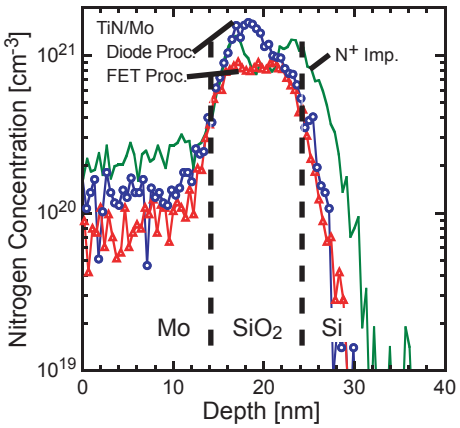

Fig. 2 Nitrogen depth profiles obtained by back-side SIMS technique. Nitrogen pileup formed at the Mo/SiO2 interface reduces by the FET-like process that includes an RTA step after TiN stripping for S/D activation.

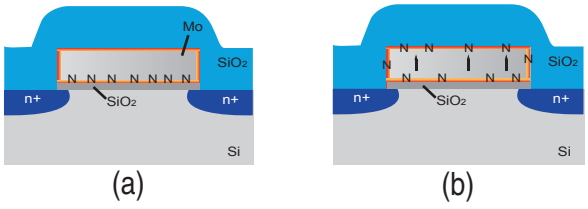

Fig. 3 Nitrogen re-distribution during Mo-gate MOSFET fabrication. (a) befor and (b) after S/D activation annealing.

at gate center. By this short channel device shows smaller workfunction shift, that is smaller V_{th} shift.

In addition to Mo, we are evaluating other materials. Workfunction shift of fully silicided poly-Si gate with Ni, in other words, NiSi gate is recently reported [2,3]. Impurities implanted into the poly-Si gate prior to the silicidation, are swept out towards the oxide interface by snowplow effect. As a result, impurity pileup is formed at the NiSi/SiO_2 by full silicidation of poly-Si (Fig. 5). We have investigated how silicidation condition affects the workfunction shift and the pileup formation with Sb. Sb depth profiles shown in Fig. 6 indicates that Sb pileup is larger for lower silicidation temperature. By lowering silicidation temperature, silicidation rate is also lowered. The snowplow effect is considered to be enhanced by slowing down silicidation rate. The amount of the pileup is reflected to V_{FB} shift evaluated with MOS diodes.

3. Summary and future plan

Workfunction tuning utilizing impurity pileup at the metal/SiO_2 interface has been investigated. In the case of N in Mo-gate, MOSFET fabrication process must be modified to reflect workfunction shift oberved with MOS diodes. We are now testing another modification, to suppress the anomalous reverse short channel effect.

In the case of Sb in NiSi gate, silicidation temperature that affects silicidation rate and the snowplow effect was the key to obtain workfunction shift. Referring this results other silicide materials are evaluated to improve the work function tuning technique.

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4. Published Papers Proceedings

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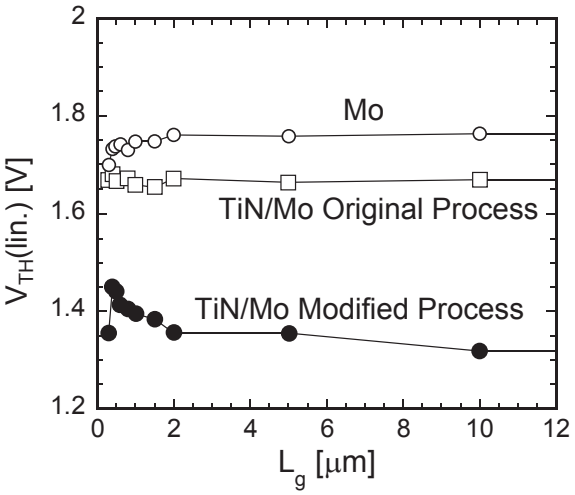

Fig. 4 Relationship between Vth and Lg for Mo gate MOSFETs. Vth was shifted by workfunction shift realized by Nitrogen incorporation into Mo gate.

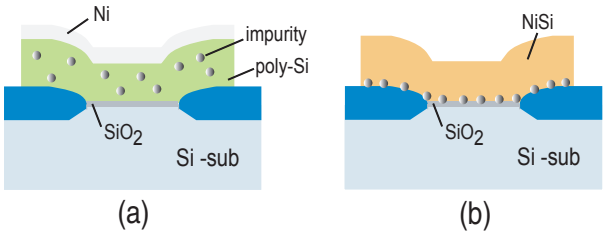

Fig. 5 Pileup formation during NiSi full-silicidation by snowplow effect. (a) before and (b) after full silicidation

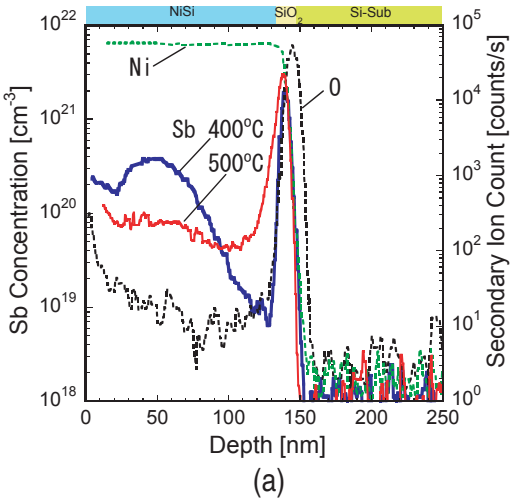

Fig. 6 (a) Sb depth profiles in NiSi-MOS structure obtained with back-side SIMS technique (a) and its closeup around the MOS interfaces. The snowplow effect and pileup formation is prpmoted by lowering silicidation temperature.

Fabrication and Evaluation Technique for Ultra-Shallow Junction

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1. Research Target

Source and drain junctions have been modified shallower and shallower as the MOSFET scaling progressed. Nowadays, the junction depth must be shallower than 20 nm for leading edge devices. Our primary research target is development of sub-10 nm junctions formation technique and precise evaluation technique for them.

2. Research Results

Short duration annealing is a key to fabricate shallow and low resistive junctions. We have succeeded 10 nm junction formation using KrF excimer laser (248 nm) annealing. In Fig. 1, B depth profiles for junctions with a depth of 9.5 nm are shown. Diffusion during annealing was smaller than 0.2 nm by utilizing short duration pulse laser with FWHM of 38 ns. Usefulness of junction must be discussed referring junction depth and sheet resistance. Even if the junction is shallow enough, high resistive junction degrade MOSFET performance. We have found that sheet resistance can be reduced less than 1 kΩ/sq. by heating a substrate to 450°C. Though Fig. 1 is an example of p^+/n shallow junction formation, n^+/p junction also shallower than 10 nm was achieved using As or Sb as dopant. This heat assist method is also effective for residual defects reduction. Figure 2 shows cross-sectional TEM images after annealing. Without the heat-assist, residual defects similar to Fig. 2(a) are usually observed. By increasing heat assist temperature, defects density was clearly reduced, as shown in Figs. 2(a) and (b). Defect reduction was further enhanced by using Ge pre-amorphization implantation that is useful to suppress long profile tail due to channeling, as shown in Figs. 2(c) and (d). To fabricate shallower junctions, dopant profiles prior to the annealing must be modified shallower. This is usually realized by reducing ion implantation energy. However, in sub-keV regime, junction depth reduction due to the energy reduction shows saturating tendency, as shown in Fig. 3. The mechanism of this tendency is not clear yet.

In addition to KrF excimer laser, we are investigating all-solid-state green laser (532 nm) annealing. All-solid-state lasers have superior equipment size and easiness of maintenance that fit to mass production. However,

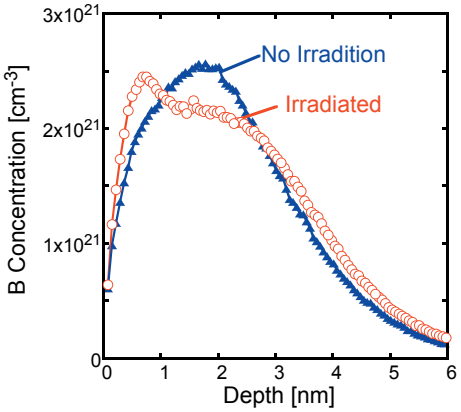

Fig. 1 B depth profiles for (a) before and (b) heat assited laser annealing.

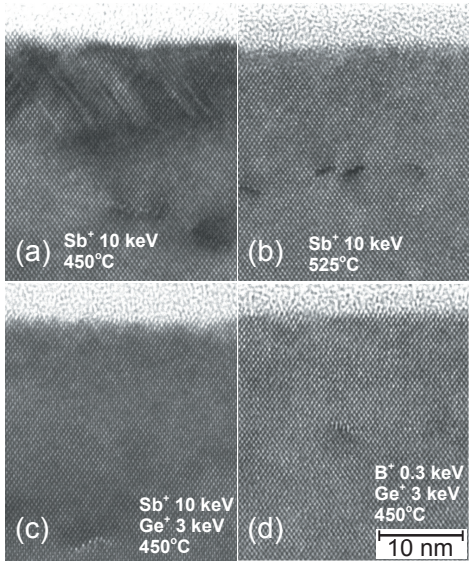

Fig. 2 XTEM photographs to evaluate residual defects after heat-assited laser annealing. Stacking faults seen in (a) are reduced by increasing heat-assist temperature or using Ge pre-amorphization.

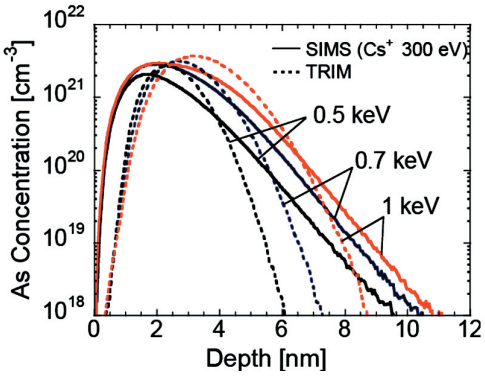

Fig. 3 As implanted As profiles for sub-keV ion implantation.

penetration depth of green light is about 1 μm and much deeper than device dimensions. This leads to wasting power for unnecessary deep area heating and high power laser equipments. Based on such background, green laser annealing utilizing light absorber have been investigated. TiN or Mo was deposited on Si after 2-nm screen oxide formation. Comparison of relationships between sheet resistance and laser energy densities in Fig. 4 showed that TiN light absorber effectively reduced the laser energy density to activate dopant but Mo increased. This result is explained by their optical characteristics. Junction depth fundamentally depended on amorphous layer depth, however, the annealing with the absorber easily lead to overmelt of c-Si (Fig. 5) probably due to absence of a negative feedback effect by reflectance increase by surface melting.

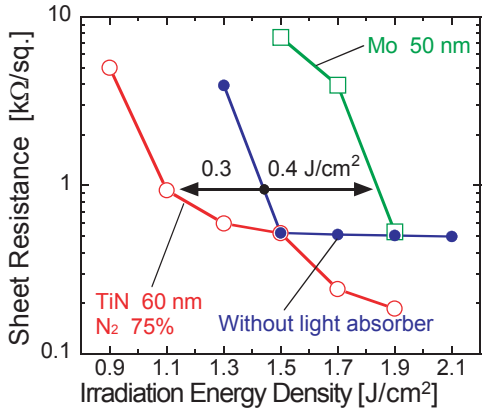

Fig. 4 Relationships between sheet resitance and laser energy density. TiN film deposited on Si as a green-laser-light absober reduces the laser energy density necessay for dopant activation.

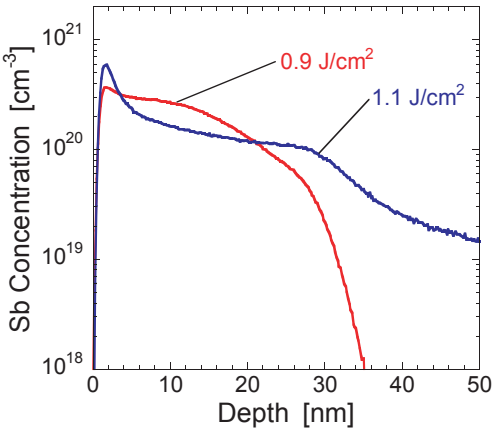

Fig. 5 Sb depth profiles after the green laser annealing with the TiN light absorber. The depth profiles for 1.1 J/cm^2 shows overmelt that makes the junction much deeper.

3. Summary and future plan

Low resistive ultra-shallow junctions were fabricated using heat-assisted KrF excimer laser annealing. This method is also effective for residual defects reduction. Investigation of another laser annealing method with green laser has started. We will improve the later importing the idea of heat-assisted method to it.

4. Published Papers and Proceedings

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