# Research and Development of Three-Dimensional MOS Transistors


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## 1. Purpose of R&D

Greater integration and higher density of integrated circuits which started around 1970 has achieved almost one million increase in performance. The strongest driving force is scaling of MOS transistor. First transistor of 10 μm in size has been scaled to 1/10 during 15 years and to 1/100 during another 15 years. Transistors of 0.1 μm in size will soon be manufactured. While, a transistor of 5 nm in size has already been presented in research stage, however, its performance is not adequate yet contrary to its size[1].

In response to its miniaturization, performance degradation due to the short-channel effects such as poor controllability of threshold voltage and increase in cut-off current have occurred.

Although precise control of impurity profiles near source and drain and thinning of the gate insulator have been developed to suppress the short-channel effects, limitations are getting close. To cope with thi problem, three-dimensional (3-D) MOS transistors such as DELTA[2], double-gate structure[3], FIN-FET[4] with very thin silicon-on-insulator (SOI) layer have been extensively developed.

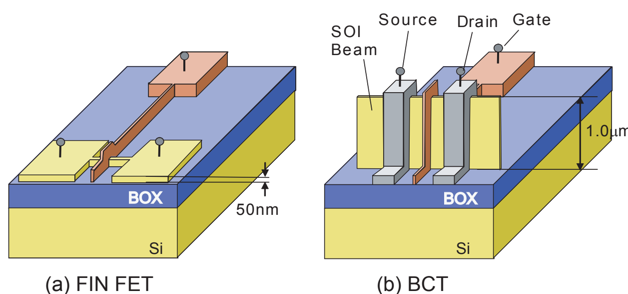



Fig. 1 FINFET (a) as a representative of 3-D transistor and a beam channel transistor, BCT under study.

A 3-D transistor with 10-nm gate length has already been presented. As the transistor has vertical channels on a Si beam, as shown in Fig. 1, drive current per unit planar area can be increased with the increase in the beam height.

To achieve higher drive current, it is planned in this study to get relatively higher beam. Major subjects are listed in Table 1. Difficulty in fabricating tall 3-D transistor rather depends on aspect ratio of the beam than absolute height of the beam.

Table 1 Purpose and subjects of this study

A. 3-D transistor with beam higher than 500 nm.
- (a-1) Delineation of high Si beam
- (a-2) Gate formation around high Si beam
- (a-3) Impurity doping to high Si beam
- (a-4) S/D contact to high Si beam

B. Highly self-aligned transistor with beam lower than 500 nm.

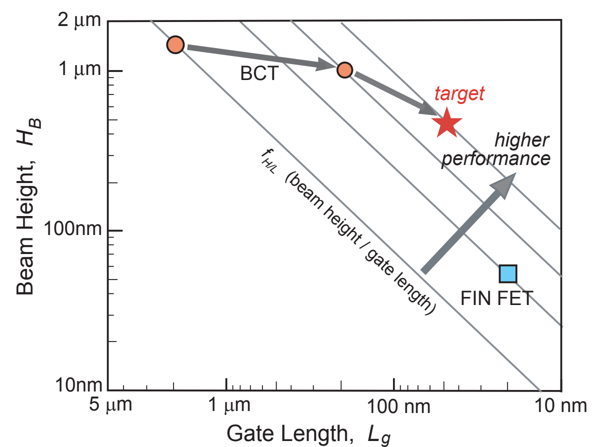



Fig. 2 A figure of merit of beam height / gate length, $f_{H/L}$ of 3-D transistor.

## 2 Experimental and the Results

### 2.1 Delineation of high Si beam

It is possible to obtain high aspect-ratio Si beam with present highly directional reactive ion etching, RIE. However, anisotropic etching with tetramethy lammoniumhydroxide, TMAH may be adequate to realize much higher and steeper beam. fabricating tall 3-D transistor rather depends on aspect ratio of the beam than absolute height of the beam. Due to its very low etch rate for (111), as shown in Fig. 3, almost perfect perpendicular sidewall can obtained on (110) Si substrate. Some etched samples are shown in Fig. 4[5] and obtained etch rates are shown in Table 2.

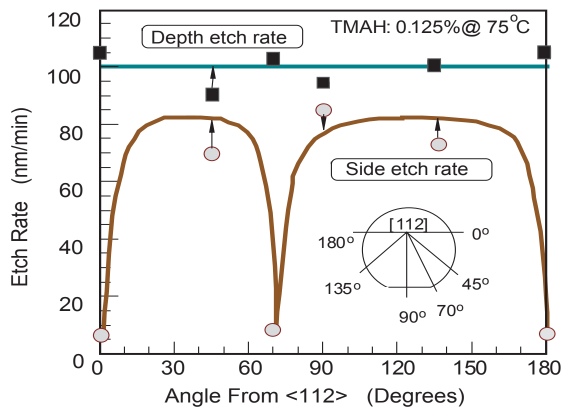
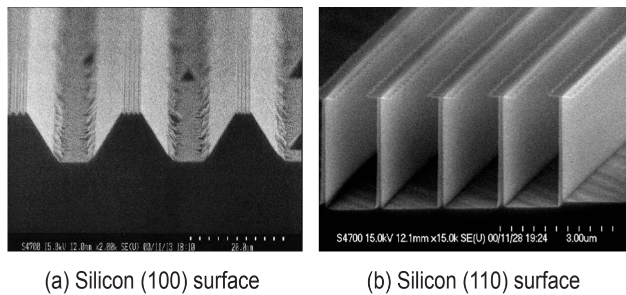



Fig. 3 Etch rate of TMAH on (110) Si surface. Extremely low etch rates correspond to those for (111) surface.




(a) Silicon (100) surface (b) Silicon (110) surface

Fig. 4 Obtained cross sections of Si (100) (a) and Si (110) with TMAH etchant.

Table 2 Etch rates of TMAH (2.5% aqueous solution at 75°C).

| Material | Etch Rate | Ratio |
|---|---|---|
| (110) Si | 606 nm/min | 30 |
| (111) Si | 30 nm/min | 1 |
| $SiO_2$ | 0.8 nm/min | 0.04 |

Using this etchant, a corrugated channel transistor with multiple Si beams has been succcessfully fabricated[6] as shown in Fig. 5. The height and the width of the beam are 900 nm and 82 nm, respectively. The $I_d$-$V_d$ characteristics of the transistor are shown in Fig. 6. While the threshold voltages are below 0 V because the substrate resistivity of 80 Ω-cm and not employing channel doping, there is no degradation concerning carrier mobility and gate oxide integrity.

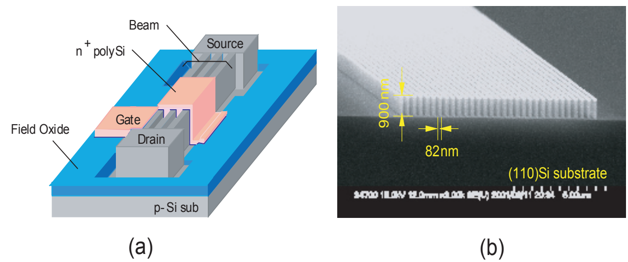



Fig. 5 A bird's eye view (a) and an SEM image of etched SI beams. surface.

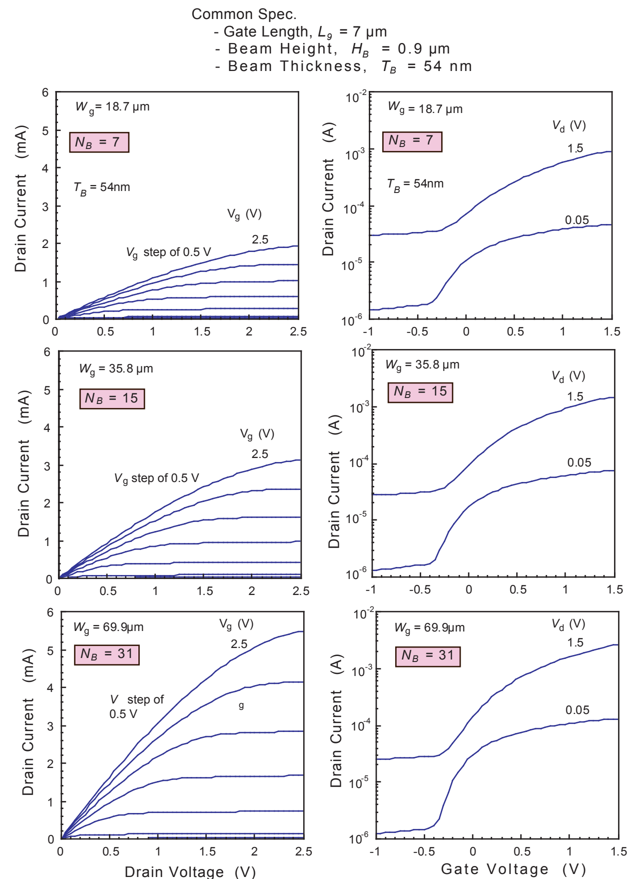



Fig. 6 $I_d$-$V_d$ and $I_d$-$V_g$ characteristics of corrugated channel transistor, CCT. Obtained threshold voltages below 0 V are due to high reistivity substrate (80 Ω-cm) and no channel doping.

Substrate bias dependence of the threshold voltage is shown in Fig. 7. Curves of beam thickness $T_B$ of below 0.96 μm are almost the same each other due to throughly depleted beam. Drain currents are shown in Fig. 8 in terms of unit planar area. CCT offers almost 5-fold current as compared to the conventional planar at a planar area of 100 $\mu m^2$.

Regarding gate oxide integrity, there may be some problem due to the oxide thinning at edges of the beam.. In fact the thinning are observed at top and bottom edges of the Si beam as shown in Fig. 9. However, there is no substantial failure because applied voltages get lower in response to transistor scaling.

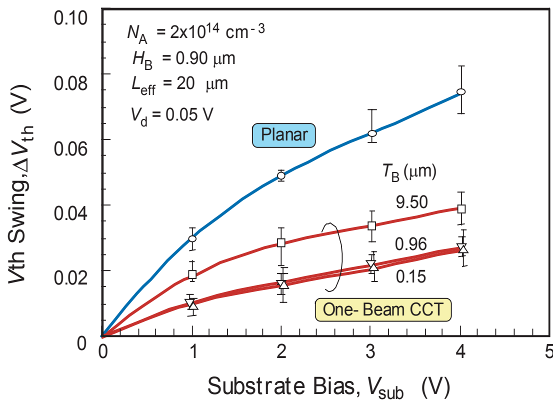



Fig. 7 Threshold voltage swings for one-beam CCT and planar transistor. Note that curves with beam thickness $T_B$ of below 0.96 μm are equivalent.

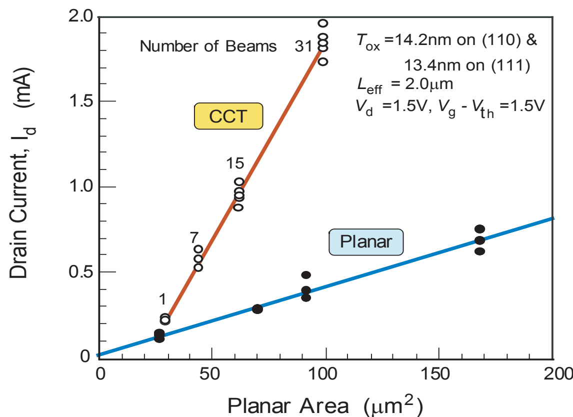



Fig. 8 Drain currents of CCT's with number of beams of from 1 to 31. Almost 5-fold increase is obtained compared to planar transistor at a planar are of 100 $\mu m^2$.

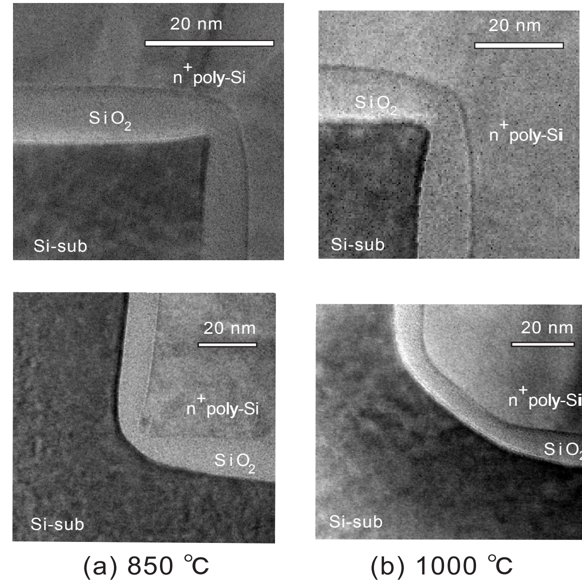



Fig. 9 Cross-sectional TEM images for oxide thinning at beam edges.

## 2.2 Delineation of gate electrode overlaying high Si beam

The use of conventional anisotropic dry etching to delineate polysilicon gate overlaying Si beam gives rise to residues on sidewalls of the beam as shown in Fig. 10 (a). Thus, isotropic etching is inevitable at present, as shown in Fig. 10 (b).

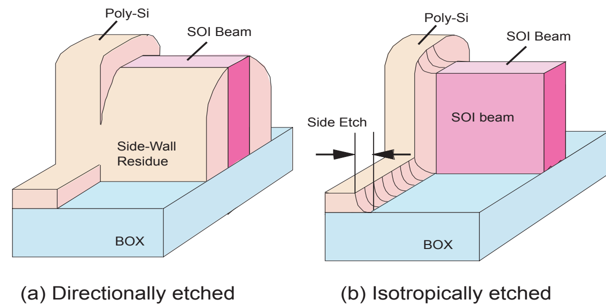
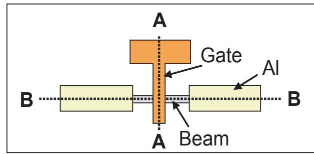



Fig. 10 Gate electrodes formed by anisotropic etching (a) or isotropic etching (b).Cross-sectional TEM images for

To overcome the problem, a novel technique has been developed[7]. This technique makes it possible to wrap the polysilicon gate with its own oxide, as shown in FIg. 11, utilizing impurity enhanced oxidation, IEO[8]. The enhancement occurs with highly doped Si at low-temperature wet oxidation. In certain condition more than 10-fold enhancement is possible. An obtained sample and the IEO are shown in Fig. 12 and Fig. 13, respectively.




(A-A cross section) (B-B cross section)

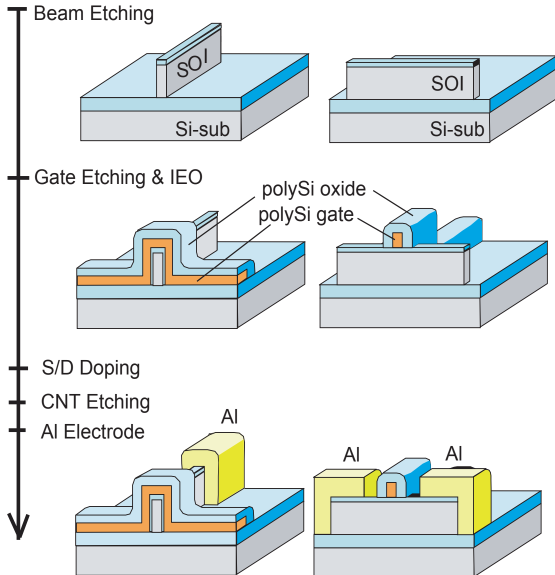



Fig. 11 A proposed process sequence of beam channel transistor.

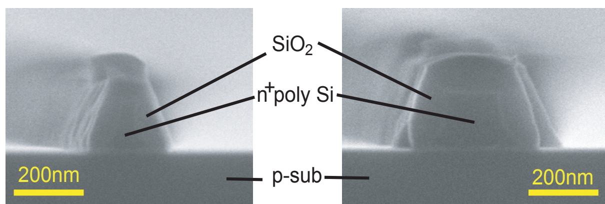



Fig. 12 Polysilicon gates wraped by their own oxide.

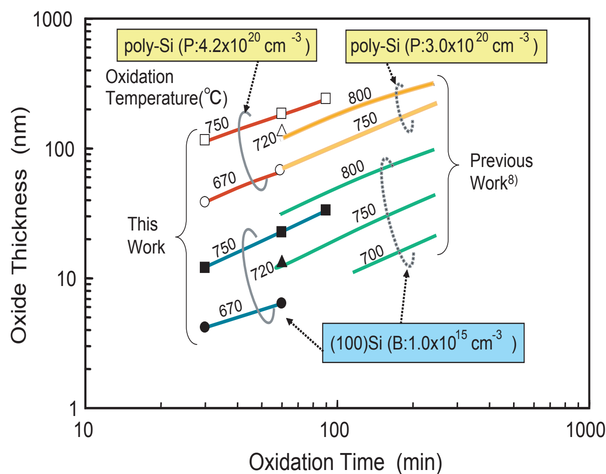



Fig. 13 Experimental results of impurity enhanced oxidation, IEO.

A cross section, $I_d$-$V_d$ and $I_d$-$V_g$ characteristics are shown in Figs. 14, 15, and 16, respectively for beam channel SOI transistors fabricated with these techniques described here. These characteristics show no deterioration.

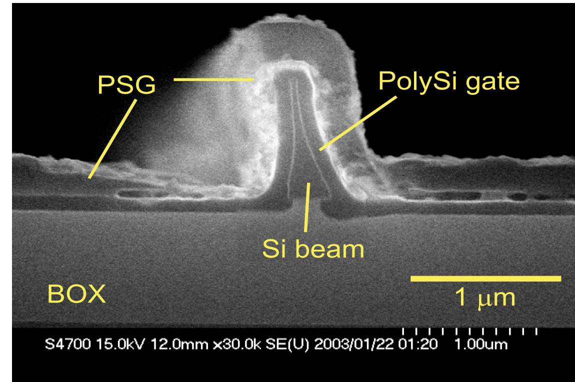



Fig. 14 A cross section of SOI beam channel transitor with 1.0-μm high SOI beam.Ω-cm) and no channel doping.

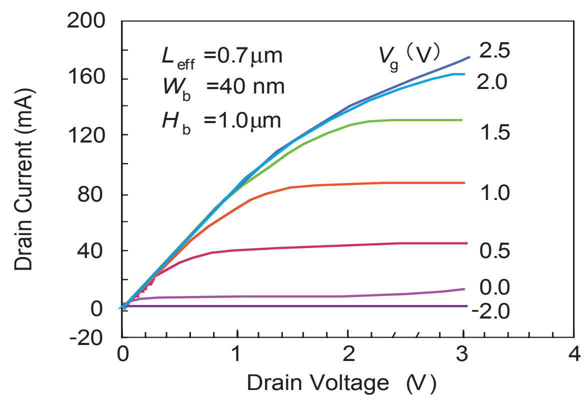



Fig. 15 $I_d$-$V_d$ characteristics for beam channel transistor with 1.0-μm high and 40-nm thick SOI beam and 0.7-μm channel length. No channel implantation causes weak cut-off.

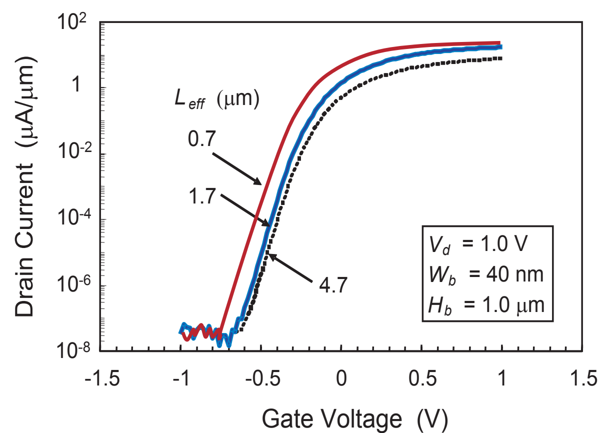



Fig. 15 $I_d$-$V_g$ characteristics for beam channel transistor with 1.0-μm high and 40-nm thick SOI beam and 0.7-μm channel length. No channel implantation causes weak cut-off.

One of performance factors of MOS transistor is a figure of merit $[I_d L_{eff} T_{ox}/W_{eff}]$ . This directly relates to field-effect mobility and integrity of the transistor. Figure 17 shows these for BCT and FIN-FET. It is because mobility decrease that the factor decreases at small beam width region. This should be an inherent problem for very thin Si beam 3-D transistor.

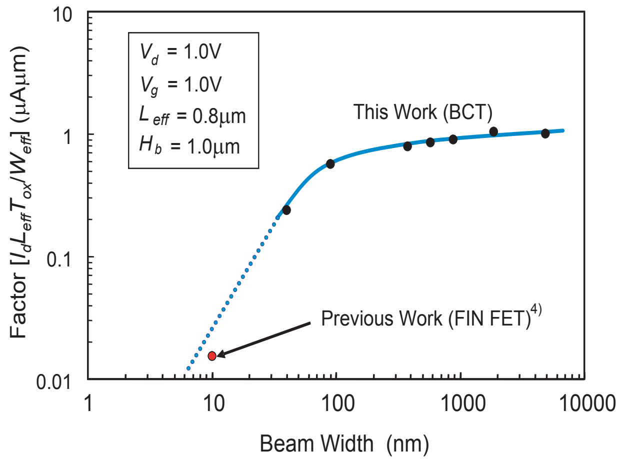



Fig. 17 Dependence of a factor, $[I_d L_{eff} T_{ox}/W_{eff}]$ on beam width. cut-off.

While, a ratio of on current to off current is shown in Fig. 18. The ratio is more important rather than on-current itself to design high performance and low power LSI. Beam channel transistor has considerable merit in therms of this performance.

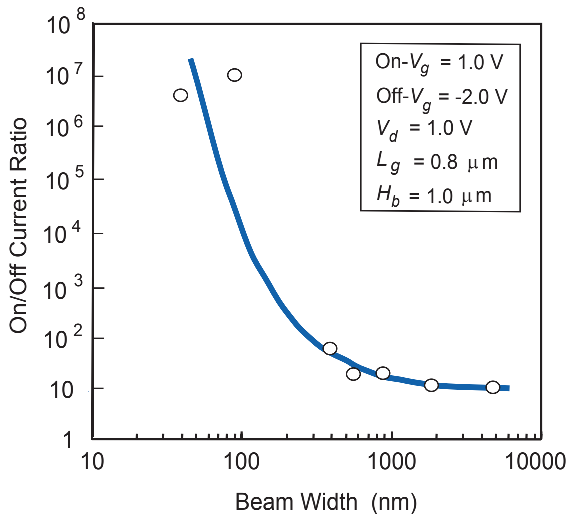



Fig. 18 Beam width dependence of on-current to off-current ratio for SOI BCT ($T_{ox}$=10 nm).

## 2.3 Impurity doping to high Si beam

Even though utilizing oblique implantation, there exists certain limitation to conventional ion implantation technique, I/I to make uniform doping to high and dense Si beams. To cope with the problem, nearly isotropic plasma doping, PD is applied in this study.

A comparison of impurity profiles of I/I and PD is shown in Fig. 19 at the same acceleration voltage of 700 V. While, the beam shape is shown in Fig. 20. It is clear that the edges are sputtered and scraped off to some extent by Ar plasma in PD.

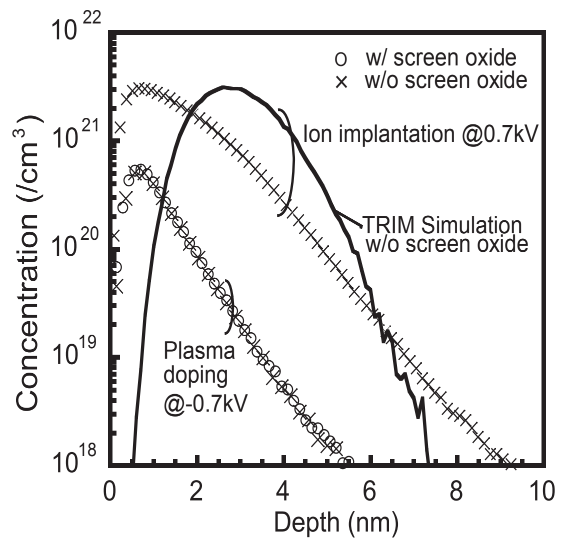



Fig. 19 Srsenc SIM profiled for ion implantation and plasma doping.

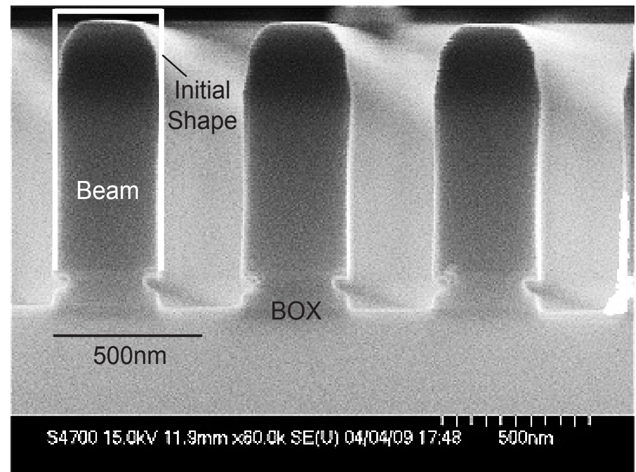



Fig. 20 Si beams doped with Arsenc by plasma doping. Top edges are sputtered and scraped off by Ar plasma at -700-V bias.

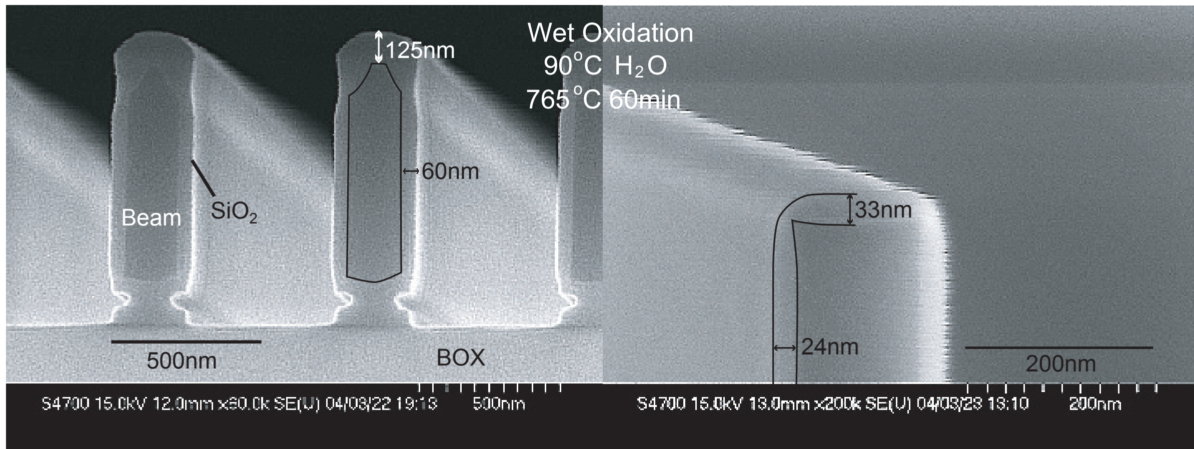



Fig. 21 Cross-sectional SEM images of As-plasma doped Si beam (a) and non-doped Si beam (b) after wet oxidation at 765°C for 60 min. Oxide thickness closely relates impurity concentration.

There is no direct measurement technique to evaluate 3-D impurity profile along vertical wall. Therefore, a novel indirect technique is proposed, which utilizes impurity enhanced oxidation. An oxide profile is shown in Fig. 21. From this profile, Arsenic concentration profile is thus evaluated and shown in Fig. 22. It is clear sidewalls are almost uniformly doped despite that top edges are doped at several times higher concentration. Both side dips in "Non-doped" curve correspond to poor uniformity of oxide, as shown in the right side of Fig. 21.

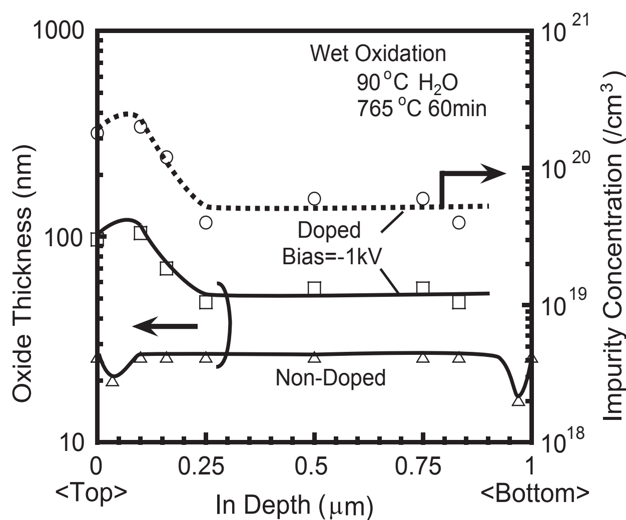



Fig. 22 Measured oxide thickness profile and doped impurity profile for 1.0-µm high Si beam, indirectly evaluated from the oxide profile.

## 2.4 S/D contact to high Si beam

When a contact to source and drain (S/D) is formed only on the top surface of the beam, a part of source currrent flowing at the bottom portion suffers form parasitic resistance of the source. This causes performance degradation of the transistor. Obtained beam resistance is shown in Fig. 23. It is observed that beam resistance becomes constant at beam width of below 300 nm. It is because thickness of phosphorus-doped region becomes constant at that rgion.

Since the thickness of S/D region of BCT is smaller than 100 nm, S/D resistance can not be neglected. To overcome the problem, some methods efficient to reduce the resistance should be employed. These are as follows:

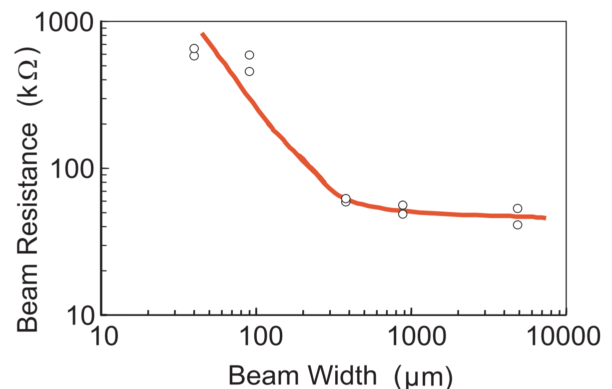


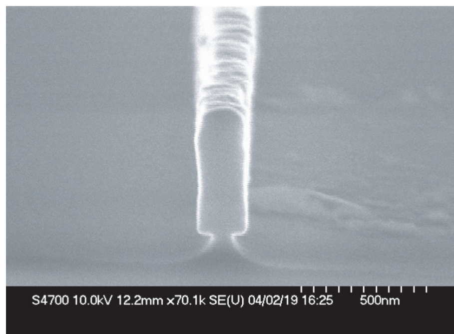

Fig. 23 Beam width dependence of beam resistance for phosphorus-doped Si beam.

(1) silicidation of S/D,
(2) elevated S/D with Si and/or Ge, and
(3) metal wrapping around S/D.

Preliminary experiment for silicidation has been carried out in this study. Phosphorus-doped Si beam is silicided with 100-nm thick sputtered Ni after vacuum baking at 500°C for 30 min, as shown in Fig. 25. Beam width dependence of the beam resistance is shown in Fig. 25.

Estimated resistivity of phoshprus-doped Si beam and its silicided layer are:

- $n^+$-Si beam resistivity = $4.2 \times 10^{-4}$ Ω-cm
- Ni silicide layer resistivity = $2.5 \times 10^{-5}$ Ω-cm




Beam height/width＝550 nm/180 nm

Fig. 24 Ni-silicided Si beam.

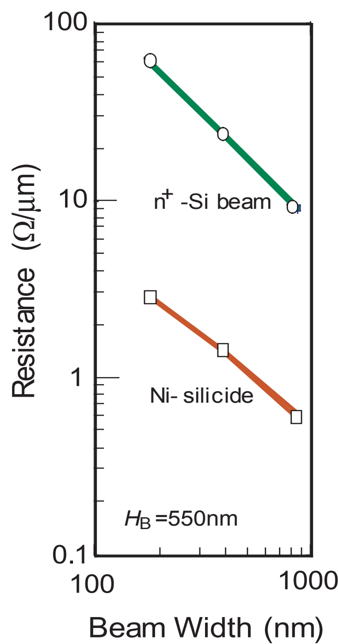



Fig. 25 Resistance of Ni-silicided S/D

Reagarding these values, it is clarified that adequate silicidation occurs. Since the data are taken only for one isolated beam, dense and multi-beams should be investigated.

## 3 Conclusion and Future Plan

In this study, one set of beam channel transistor, BCT of 1.5-μm beam height and 2.0-μm gate length, and another set of those of 1.0-μm beam height and 0.2-μm gate length are successfully developed. Since BCT with high Si beam can not provide narrow channel width, the BCT is not able to be major conponent of LSI. Therefore, the BCT is suitable to some applications with big power in small area.

They are:
(1) discrete power transistor,
(2) wireless receiver/transmitter IC integrateing RF power transistor, and
(3) power control transistor for ultra-low power.

Some example concerning item (3) is shown in Fig. 26. This is an idea that a pull-down transistor which is connected in series to a circuit block controls power and operation speed of the block in time sharing manner.[9] Since it is desirable that on-resistance of the pull-down transistor is as small as possible, BCT which can provide large current in small planar area is suitable with less area penalty.

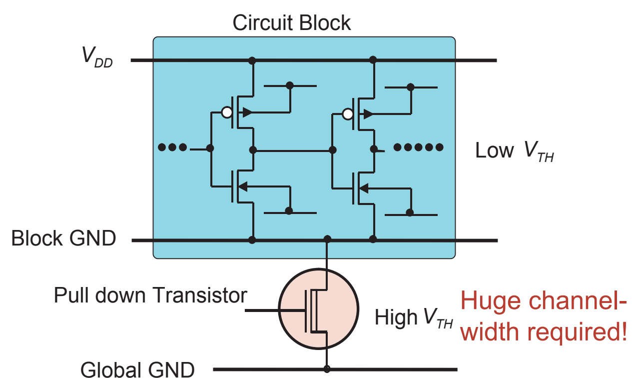



Fig. 26 An idea to control power/operation speed with each circuit block[9].

Regarding to ultra-small 3-D transistors, those of 50-nm thick beam and 20-nm gate length has been already presented by other organization. Taking the aspect ratio of the beam into consideration, our target of those of 200-nm thick beam and 20-nm gate length is not promising target any more.

Thus, highly self-aligned configuration in full use of 3-D structure is our target. One candidate is shown in Fig. 27. Since three planes of a beam act as different transistor, this configuration gives birth to ultra-small three transistors connected in parallel.

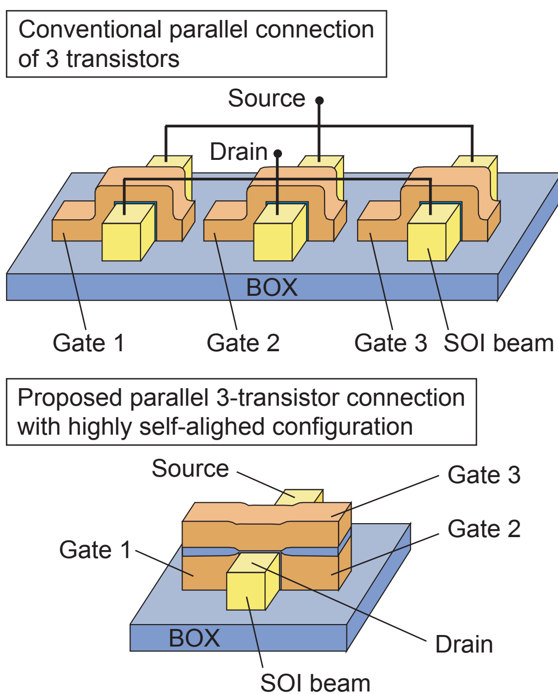



Fig. 27 Three transistors connected in pallarel with highly self-aligned configuration.

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## <Results of R&D>

### (Journal Paper)

1)T. Furukawa, H. Yamashita, and H. Sunami, "A Proposal of Corrugated-Channel Transistor (CCT) with Vertically-Formed Channels for Area-Conscious Applications," Jpn. J. Appl. Phys., Vol. 42, Part 1, No. 4B, pp. 2067-2072, April 2003.
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### (International Conference)

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