Study in 3-Dimensional new structure MOS Transistor

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1. Introduction

It is becoming difficult to control the short channel effect and to integrate conventional bulk devices up to date. To overcome this problem, three-dimensional (3-D) device structures have been proposed [1]. A FinFET of which gate electrode is 10 nm in length was already reported [2]. From now on, not only the scaling of these devices, but also the progress of new structure and/or new operation of 3-D devices become important. In this study, a new vertical structure transistor is proposed.

2. Proposed device and its fabrication processes

The structure of proposed device is shown in Fig. 1. In this structure, three transistors that are formed on a SOI beam can operate independently. This can apply to parallel part of a logic circuit, for example a part of NAND gate. Since transistors are integrated vertically, this structure has advantage from the viewpoint of area efficiency.

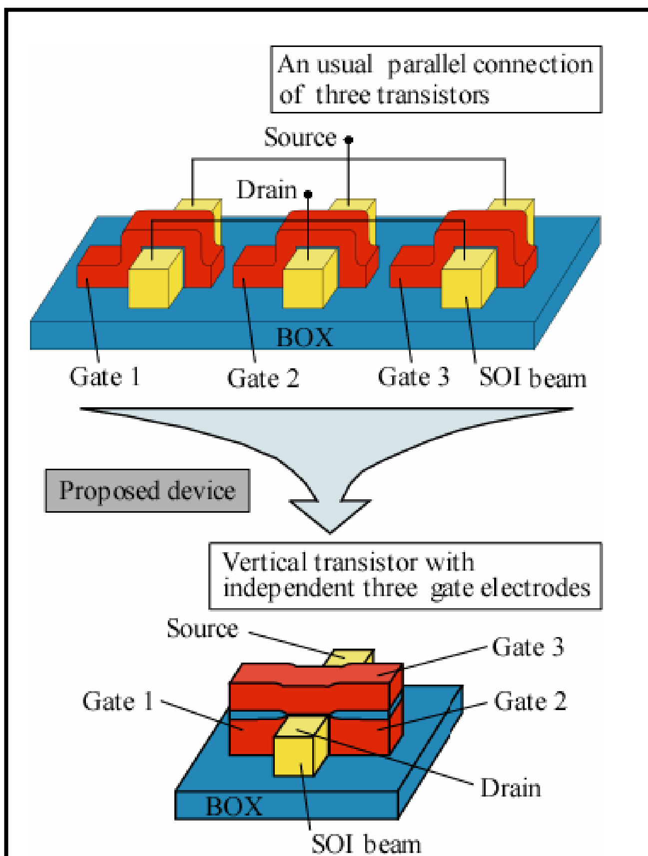

Fig. 1 A usual parallel connection of three transistors and the structure of the proposed device.

In the fabrication of this device, it is important to form three gate electrodes using self-aligned process to realize normal operation of the device. Two types of fabrication processes are devised in consideration of this point. One of these processes is shown in Fig. 2. To realize the proposed device, fabrication processes for Si-beam and gate electrode, and leveling of some kinds of materials are key techniques.

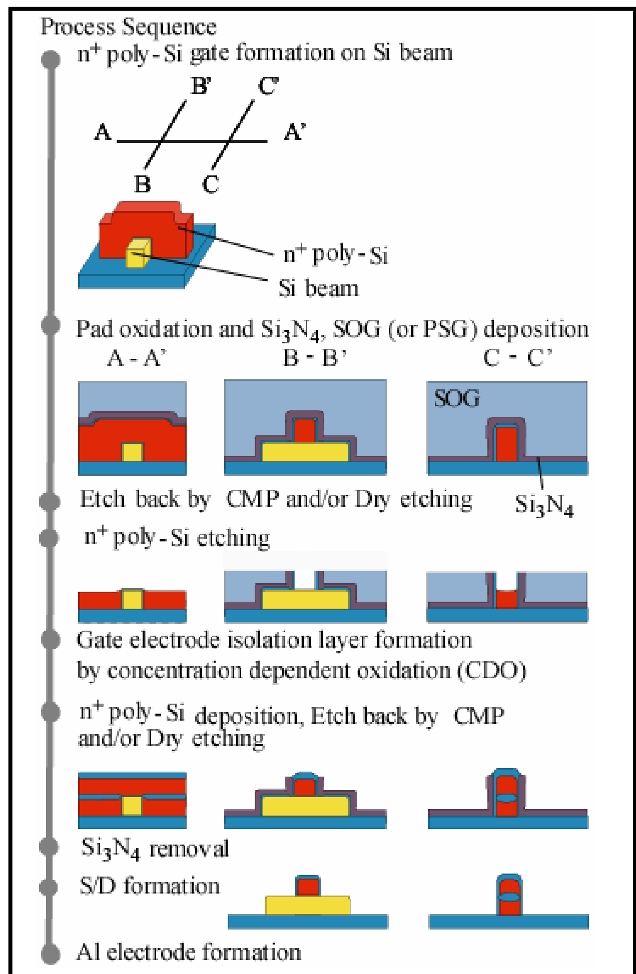

Fig. 2 A process sequence of the proposed device.

3. Experimental results and Discussion

3.1 High aspect ratio fabrication technique

Since the configuration of poly-Si patterns overlaying Si beams determines the shape of final gate electrodes in the sequence, its formation techniques are very important. During the course of the study, a Si beam of 120 nm in height and 60 nm in width and a poly-Si pattern of 100 nm in width overlaying the beam are successfully fabri-

cated (Fig. 3). Furthermore, with respect to the concentration dependent oxidation (CDO [3]) that utilized to form the isolation layer of top gate electrode, the ratio of oxidation thicknesses of phosphorous doped n^+poly-Si and Si substrate((100), boron doped, $1x10^{15}$ /cm^3) exceeds almost 14 times at 750℃ (Fig. 4). From this result, it is concluded that the CDO is applicable to the process.

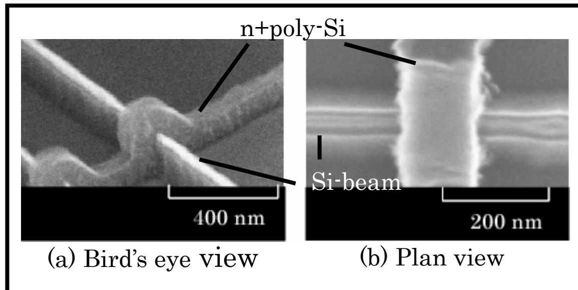

Fig. 3 SEM photographs of a Si-beam of 120 nm in height and 60 nm in width and a poly-Si gate electrode overlaying the beam.

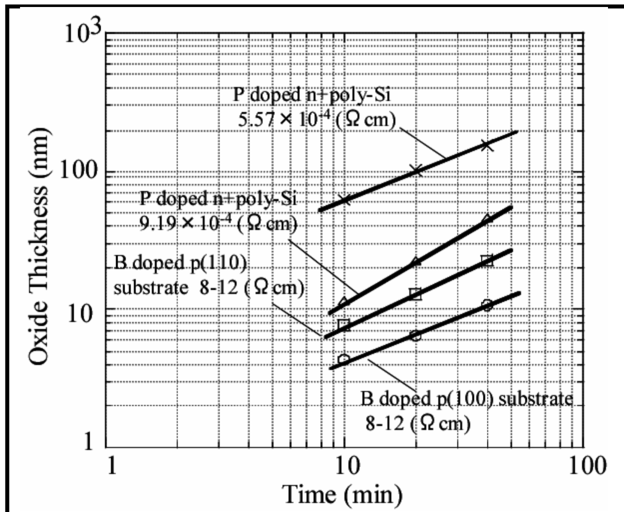

Fig. 4 Concentration dependent oxidation (CDO) at 750℃ (O_2=2 slm, 90℃ H_2O bubbling.).

3.2 Leveling process

Two kinds of methods, RIE and CMP techniques are developed as the leveling process. In this experiment, SOG was used as the leveling material. The etching characteristics of RIE are shown in Fig. 5. In this case, four kinds of materials (SOG, Si_3N_4, SiO_2, n^+ poly-Si) have to be etched with adequate low selectivity, then the etching has been performed under a condition of H_2 = 0 and 4 sccm. In the former case, it was observed that SOG and Si_3N_4 were already etched before leveling the n^+poly-Si layer. In the latter case, the roughness of n^+ poly-Si surface was degraded and the damage on the top of source and drain regions of Si beam occurred (Fig. 6).

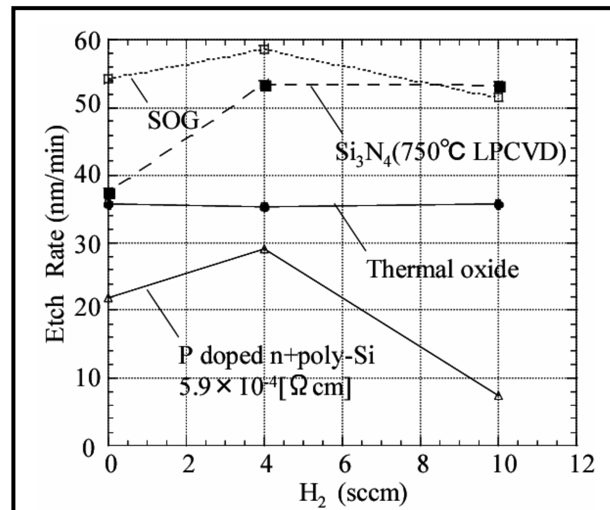

Fig. 5 Etching characteristics of RIE (CF_4 = 20 sccm, etching pressure = 30 mTorr, self bias = –410 V) .

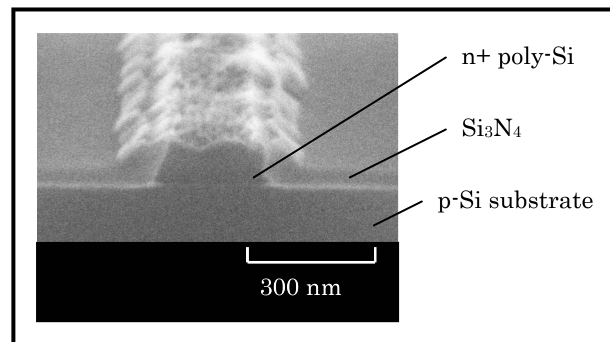

Fig. 6 SEM photograph of an n^+ poly-Si electrode after RIE etch-back.

4. Summary and future work

A novel 3-D transistor structure and its fabrication processes are proposed. With respect to the high-aspect ratio fabrication technique, poly-Si patterns overlaying Si beams are successfully fabricated. Furthermore, the result that CDO can be applicable to the isolation layer formation of the top gate electrode is obtained. Due to the difficulty of RIE etch back in leveling process, the introducing of CMP technique is planned to realize the proposed device structure.

5. References

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