Low resistive gate electrode/high-k gate dielectrics stacked structure and its electron device application

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Introduction

Continuous shrinkage of MOSFET requires the aggressive scaling of gate length and gate dielectric thickness. Shrinkage of poly-Si gate causes various problems, such as increased parasitic resistance, threshold voltage shift, and gate depletion. Poly-SiGe gate is one of the promising candidate for a gate material of next-generation MOSFETs, because of low resistivity, less poly depletion effect, control of work function and matching with conventional silicon process. However, poly-SiGe has some problems, such as reliability degradation of gate dielectric caused by Ge atoms diffusion from poly-SiGe gate into gate dielectrics when high temperature thermal process. Therefore, Thin silicon buffer layer is formed between gate dielectric and poly-SiGe. For practical application of MISFETs with poly-SiGe, we need to understand mechanism of Ge atom diffusion and control the Ge and dopant profile. In this work, We evaluate Ge diffusion and redistribution effect on poly-Si/poly-SiGe/poly-Si stacked structure. We fabricate MIS capacitor with poly-SiGe gate, and evaluate how does effect germanium redistribution to the electrical properties.

Experimental

The substrates used in this work were p-type and n-type Si(100) wafers in which the acceptor and donor concentrations are $1.5x10^{15}cm^{-3}$ and $5x10^{14}cm^{-3}$, respectively.

After conventional wet-chemical cleaning steps of these wafers, SiO_2 layers in the thickness range of 2.0-4.0nm were grown at 1000℃ in dry O_2 and then poly-Si/SiGe/Si/SiO_2 stacked structures were fabricated on the wafers by the following low-pressure chemical vapor deposition (LPCVD) steps at a substrate temperature of 570℃. First, ~30nm-thick poly-Si as a buffer layer was formed from the thermal decomposition of pure SiH_4 under 0.36torr and subsequently, ~100nm thick poly-SiGe was deposited under 0.42torr of a pure SiH_4 and 10%GeH_4 diluted with He, in which the gas molar ratio of SiH_4 to GeH_4 was varied from 2 to 10, and followed by LPCVD of ~100nm thick poly-Si film as a cap layer with the same conditions as the buffer

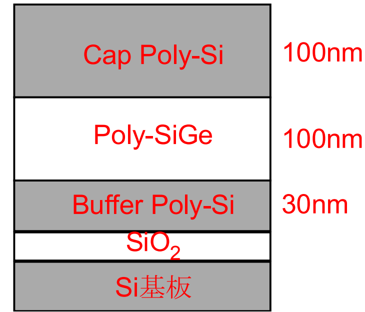

Fig1. Cap Poly-Si/Poly-SiGe/Buffer Poly-Si stacked structure.

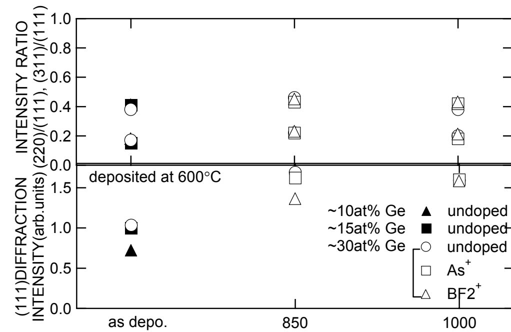

Fig. 2 The (111) peak intensity measured by XRD and the intensity ratio of (220) and (311) peaks to the (111) peak for as-deposited poly-$Si_{1-x}Ge_x$(100nm, x=0.1, 0.15 and 0.3)/SiO_2(2nm)/Si(100) formed by LPCVD at 600°C and annealed samples of x=0.3 after As^+ or BF_2^+ implantation. The annealing time was 30min.

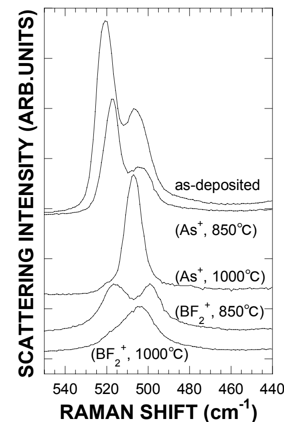

Fig. 3 Raman scattering spectra of as-deposited and N_2 annealed samples of poly-Si/SiGe/Si/SiO_2 stacked structures. The Ge concentration in the poly-SiGe layer before ion implantation was 30 at.%.

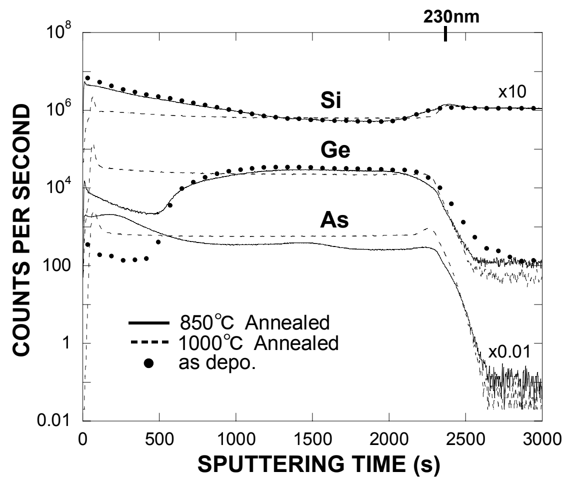

Fig. 4 : SIMS profiles for the as-deposited and N_2-annealed samples after As^+-implantation shown in Fig. 2, which were measured by using Cs^- ions.

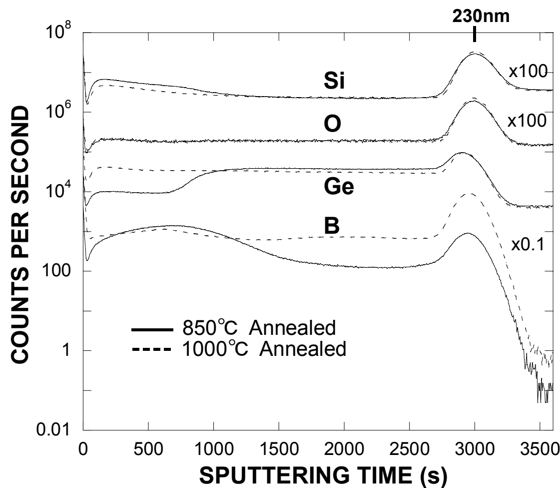

Fig. 5 SIMS profiles for the N_2-annealed sample after BF_2^+-implantation shown in Fig. 2, which were measured by using O^{2-} ions.

layer(Fig. 1). BF_2 ions or As^+ ions accelerated at 30keV or 15keV were implanted with a dose of $5x10^{15}cm^{-2}$ to the stack structures so prepared and followed by activation annealing in the temperature range of 800~1000℃ for 30 or 10 min in N_2 ambient. The crystallinity of the stacked film was evaluated by X-ray diffraction(XRD) using a Cu Kα line and Raman scattering measurements using a 441.6nm light from a He-Cd laser. The depth profiles of Ge, Si and dopant atoms in the stack structures were evaluated by secondary ion mass spectroscopy(SIMS) using Cs^+ or O^{2-} ions beam at 1kV and energy dispersive x-ray (EDX) analysis in a transmission electron microscope (TEM) operated at 200kV. The resistivity measurements for the annealed samples were performed using a four-point probe method. Also, the gate leakage current and capacitance-voltage characteristics of fabricated MOS capacitors were evaluated to check the influence of the Ge redistribution on the gate oxide.

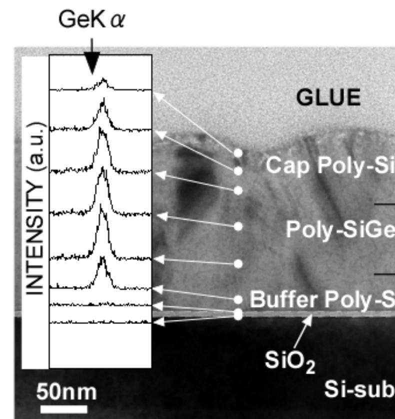

Fig. 6: Cross-sectional TEM image of the stack structures on 4nm-thick SiO_2/Si(100) annealed at 800℃ for 10min after BF_2^+ implantation and EDX spectra taken at different positions. The Ge concentration in as-deposited SiGe layer was ~30%.

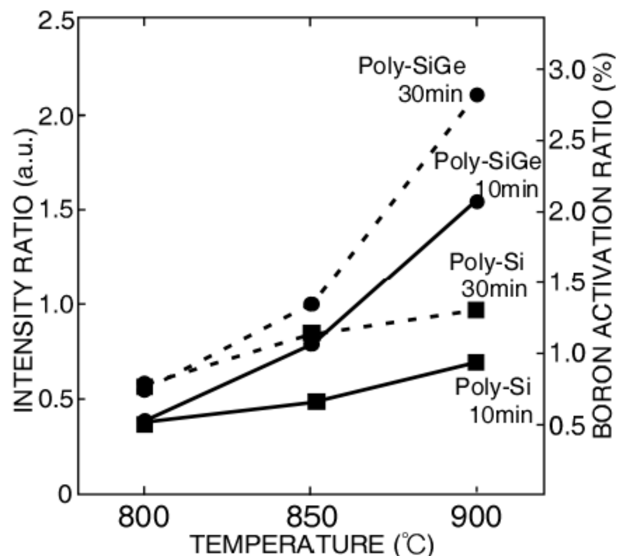

Fig. 7: The Raman intensity ratio of the peak due to acceptors to that due to the Si TO phonon mode for poly-Si and poly SiGe samples annealed at different temperatures for 10 and 30min. after BF_2^+ implantation. The ratio corresponds roughly to the boron activation ratio. The bottom oxide thickness was 4.0nm and the Ge concentration in as-deposited SiGe layer was ~30%.

Results and Discussion

XRD measurements for 250nm-thick $Si_{1-x}Ge_x$ single film formed on 2nm-thick SiO_2 confirm an improvement of the crystallinity by post deposition anneal and no significant different in the crystallinity between the annealed samples as shown in Fig. 2.

The relative intensity of the diffraction peaks due to (111), (220) and (311) planes indicates that polycrystallites are oriented preferentially to the (111) direction, but not strongly, and the preferential orientation is not changed by N_2 anneal subsequent to ion implantation. In 850℃ annealed cases, the

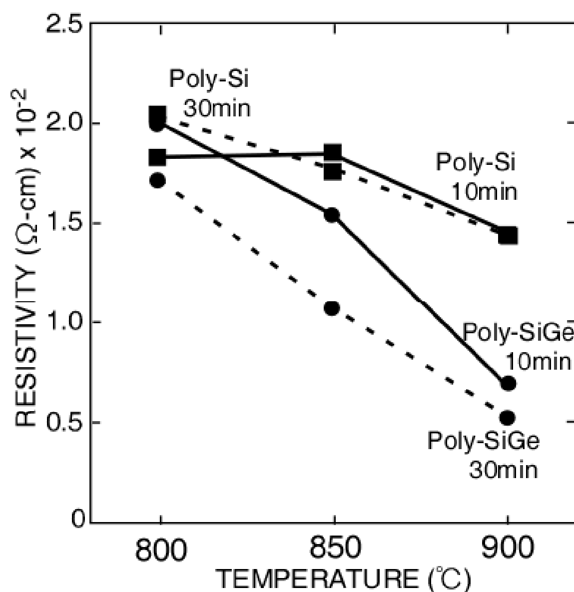

Fig. 8: The resistivity of the samples shown in Fig. 5 measured using a four-point probe.

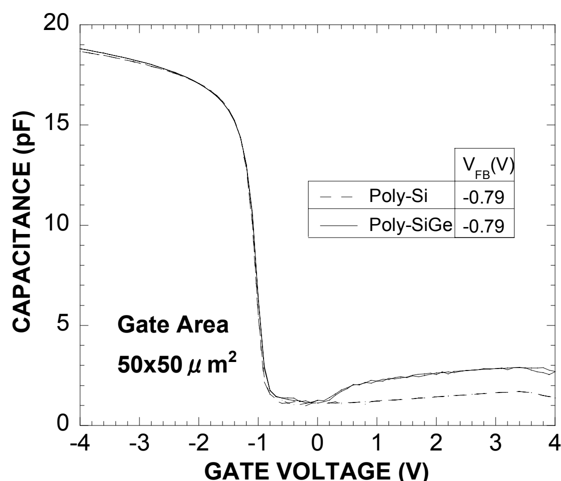

Fig. 9: C-V characteristics of MOS capacitor with n^+poly-Si gate and n^+poly-SiGe gate.

BF_2 implanted sample show a slightly degraded crystallinity in comparison with undoped and As+ implanted samples.

This can be interpreted in terms of a negative impact of implanted fluorine atoms on the crystallization.

Changes in the Raman scattering spectra for poly-Si(100nm in thickness)/poly-$Si_{0.7}Ge_{0.3}$(100nm)/poly-Si(30nm) /SiO_2(2nm)/Si(100) show the diffusion and incorporation of Ge atoms in the Si layer by N_2 anneal as represented in Fig. 3. For as-deposited sample, two sharp peaks due to TO phonons involving Si-Si stretching motions in the poly-Si cap and in the poly-SiGe layers are clearly observable at ~520cm^{-1} and ~505cm^{-1}, respectively, where the signals from the bottom poly-Si layer can not be detected because of the probing depth of the

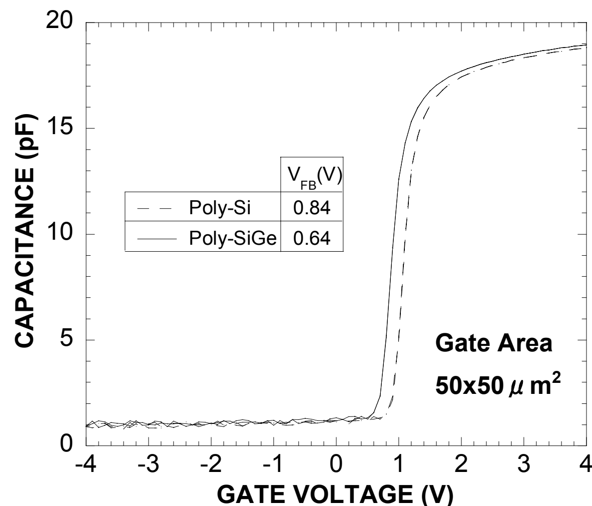

Fig. 10 C-V characteristics of MOS capacitor with p$^+$poly-Si gate and p$^+$poly-SiGe gate.

excitation laser light.

After 850℃ anneal, the TO phonon peaks are shifted towards the lower wavenumber side. The observed peak shift implies the diffusion of Ge atoms into the poly-Si cap layer.

Since, for the BF_2 implanted case, the TO phonon peak at the higher wavenumber side is significantly decreased, the Ge incorporation to the cap is likely to be more pronounced than the As^+ implanted case.

Notice that, by N_2 anneal at 1000℃, the signals from TO phonons in Si-Ge network becomes dominant, suggesting that Ge atoms diffuse uniformly in the cap layer as also confirmed by SIMS measurements.

As shown in SIMS profiles of Figs. 4 and 5, in both BF_2^+ and As^+ implanted cases, the Ge concentration in the cap layer is increased remarkably by 850℃ anneal. Obviously, by 1000℃ anneal, a quite uniform depth profile for Ge atoms is obtained as also seen in that for B or As atoms.

In addition, EDX measurements indicate that, even at annealing temperature as low as 800℃, Ge atoms can diffuse into the cap and bottom Si layers and some reaches near the top surface through the 100nm thick cap layer, presumably because point defects generated by ion implantation can enhance the atom diffusion, and that no incorporation of Ge atoms in the SiO_2 layer was detected as displayed in Fig. 6.

In the Raman scattering measurements, the signals due to the electron transition between acceptors and the valence band appear at ~610cm^{-1}[8]. For BF_2^+ implanted samples, the intensity ratio of the acceptor-derived peak to the Si TO phonon peak is thought to be related to the amount of ionized acceptors. As indicated in Fig. 7, the boron activation in poly-SiGe with annealing temperature is remarkable compared with the poly-Si case. By 900℃ anneal, the boron activation level in the poly-SiGe becomes about twice as large as that in poly-Si although there is no significant difference in the boron activation between poly-Si and poly-SiGe

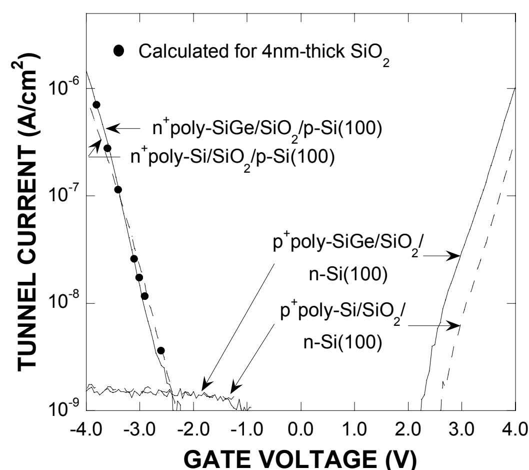

Fig. 11:I-V characteristics for the samples same as fig. 11 and the theoretical curve.

in 800℃ anneal. In consistency with this result, reasonably lower resistivities were measured for poly-SiGe annealed at temperatures higher than 850℃ in comparison to the cases of poly-Si (Fig. 7).

Capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MOS capacitors with n^+ and p^+ poly-SiGe stack structures on 4nm-thick SiO_2 were compared to those of controlled MOS capacitors with poly-Si gate in order to confirm less impact of the Ge redistribution in the stack gate on gate SiO_2 in the annealing condition at 850℃ for 30min (Figs. 8). For the cases with n^+ gate, no difference in flat-band voltage(V_{FB}) between poly-Si and poly-SiGe gates was observed. On the other hand, for the cases with p+ gate, a decrease in the V_{FB} of 0.2V was measured for the poly-SiGe gate in comparison to the poly-Si gate, being interpreted in terms of the Fermi level shift attributable to the energy shift of the valence band edge as predicted by the Ge concentration [9]. Thus, the result of Fig. 8 indicates that, by 850℃ for 30min, Ge atoms are diffused well near the interface between the buffer layer and SiO_2.

As for I-V characteristics of the MOS capacitors, the gate leakage current due to Fowler-Nordheim(F-N) tunnel is only observed, indicating the impact of Ge redistribution in the gate stack on the gate leakage is negligible(Fig. 9). In addition, for p^+ poly-SiGe gate, an increase in current level at positive gate voltages, which reflect the V_{FB} shift of 0.2V, is measured compared with the p^+poly-Si gate case, while no difference in the leakages current level at negative gate biases is obtained because the tunneling current is limited by hole generation rate in the substrate. For n^+ poly-Si and poly-SiGe gates the I-V characteristics are almost identical as seen in the C-V characteristics.

Summary

The Ge redistribution in the poly-SiGe stack structure, which consists of 100nm-thick poly-Si cap, 100nm-thick poly-SiGe and 30nm-thick poly-Si buffer, on ultrathin SiO_2/Si(100) by N_2 anneal in the temperature range of 800-1000℃ has been studied. By 1000℃ anneal for 30min, a uniform depth profile of Ge atoms throughout the whole sack structure was obtained. By 850℃ anneal for 30min, expected I-V and C-V characteristics of MOS capacitors with p^+ and n^+ poly-SiGe stack gate with a Ge content of ~30at.% were confirmed. The flat band voltage shift of 0.2V was evident only for p^+ poly-SiGe, being attributable to the difference in the energy band structure between Si and $Si_{0.7}Ge_{0.3}$, without extra current leakage.

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Achievement

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