# Photonic crystal for optoelectronic integrated circuits (OEICs)

-Technology and application of photonic crystal-

Anri Nakajima (Associate Professor, Research Center for Nanodevices and Systems, Graduate School of Advanced Sciences of Matter), Shin Yokoyama (Professor, Research Center for Nanodevices and Systems, Graduate School of Advanced Sciences of Matter), Masaru Wake (Graduate School of Advanced Sciences of Matter, M2)

## 1. Introduction

Photonic crystals are new optical materials having periodically changed refractive index and considered to act as a base medium for future ultra-small large-scale photonic integrated circuits (PICs).<sup>1)</sup> In order to realize high performance PICs, a three-dimensional photonic crystal with a perfect photonic bandgap is necessary.<sup>2)</sup> The functional devices such as nano-ampere laser arrays and optical waveguides with sharp bends can be integrated using the three-dimensional photonic crystals in the PICs.



Figure 1 The proposed realization method for three-dimensional photonic crystals.

Therefore, we need the fabrication technique for three-dimensional photonic crystal to control the structure easily.

At the Research Center for Nanodevices and Systems (RCNS), Hiroshima University, we are studying the technology of three-dimensional photonic crystals not only for the Si-based large-scale PICs but also for optoelectronic integrated circuits (OEICs). The research topics developed so far are demonstrated.

## 2. Research Results

There have been a few reports of such a fabrication technique of three-dimensional photonic crystal. However, the reported methods for fabricating three-dimensional photonic crystals are fairly complicated<sup>3,4)</sup> or have less flexibility of structure designing.<sup>5)</sup> Also, realization of optoelectronic integrated circuits (OEICs) with low cost is difficult when Si-based materials<sup>4,5)</sup> are not used for the fabrication. Recently, we have developed a direct patterning technique of interlayer dielectric films using the photosensitive film methylsilazane (MSZ) for multilevel interconnetions in ultra-large scale integrated circuits (ULSIs).6-8) The photosensitive MSZ film can be directly patterned (without using the resist) by the use of electron-beam (EB) or ultraviolet lithography. In this process, EB-resist or photo-resist coating and dry etching is not necessary for the patterning. We applied this direct patterning technique to the formation of three-dimensional photonic crystals. Owing to this technique, the number of process steps can be reduced by about half for the fabrication of three-deminsional photonic crystals.

Figure 1 shows the proposed method. A photosensitive MSZ precursor (refractive index of 1.55) is spin coated on a Si wafer to form a 150-nm-thick film [Fig. 1(a)]. After prebaking, to form a basic two-dimensional structure, EB lithography is carried out [Fig. 1(b)]. After the development and curing, the photosensitive MSZ film is changed to methylsilsesquioxane (MSQ) film (refractive index of 1.45).<sup>60</sup> In these processes, both EB-resist and dry-etching processes are eliminated for the pattern formation and the desired pattern of MSQ film is formed. Then, spin-on-glass (SOG, refractive index of 1.38) film is spin coated on the



Figure 2 A conventional method for the fabrication of three-dimensional photonic crystals.

patterned film (200-nm-thick film is formed for a plane film) [Fig. 1(c)]. After baking, SOG film with flat top surface is formed. Repeating above processes, we can easily fabricate a three-dimensional photonic crystal having the periodically changed refractive index [Fig. 1(d)].



Figure 3 Cross sectional SEM image of the fabricated structure having MSZ stripe patterns.

On the other hand, in the conventional fabrication method, resist coating [Fig. 2(b)] after the film formation of the photonic crystal material having the refractive index different from that of SOG [Fig. 2(a)], dry etching of the material with the resist mask [Fig. 2(d)], and the resist mask stripping [Fig. 2(e)] are added compared with the proposed processes (Fig. 1). Therefore, the number of process steps in the proposed method is reduced by about half.

Figure 3 shows a SEM image of the fabricated structure. As seen in Fig. 3(a), a basic two-dimensional structure of the MSZ film with the stripe pattern is indeed formed and covered by the SOG film having the flat top surface. The line and space of the stripe pattern is 300 nm, which is suitable to the photonic crystal in the optical wavelength region ( $500 \sim 1600$  nm). Owing to the flatness of the top SOG surface, the periodic two-dimensional structure of the MSZ can be stacked repeatedly [Fig. 3(b)].

Figure 4 shows the bird's-eye view SEM image of the woodpile structure fabricated using the proposed process. The stripe patterns of the stacked MSZ layer crosses over the underlying one.

Figure 5 shows a SEM image of a two-dimensional structure with a Y-branch wave guide fabricated using the proposed technique. Thus, we can easily incorporate such basic two-dimensional structures into three-dimensional photonic crystals for functional devices.



Figure 4 Bird's-eye view SEM image of the fabricated woodpile structure.

Our process proposed in this study is compatible with those of ULSIs because the direct patterning technique has been primarily developed for the dielectrics for interconnections in ULSIs. The compatibility leads to the capability of utilizing state-of-the-art nanostructure-fabrication technologies in ULSIs. Moreover, we can combine the fabricated photonic crystals with ULSIs easily. This is advantageous to the realization of OEICs with low cost.

### 3. Summary

In summary, we have successfully applied the





Figure 5 Top view SEM mage of the fabricated two-dimensional Y-branch waveguide structure (a) and the schematic of the cross section (b).

direct patterning technique to the formation of three-dimensional photonic crystals. The basic structures with stacked stripe pattern, woodpile structure, and two-dimensional Y shape waveguide have been realized. Utilizing this process, the number of process steps can be reduced by about half. The proposed process is promising for realizing low cost OEICs.

#### References

- 1) E. Yablonovitch, Phys. Rev. Lett. 58 (1987) 2059.
- E. Yablonovitch, T. Gmitter, and K. Leung, Phys. Rev. Lett. 67 (1991) 2295.
- S. Noda, N. Yamamoto, and A. Sasaki, Jpn J. Appl. Phys. 35 (1996) L909.
- 4) J. G. Fleming and S.-Y. Lin, Opt. Lett. 24 (1999) 49.
- 5) M. Notomi, T. Tamamura, T. Kawashima, and S. Kawakami, Appl. Phys. Lett. 77 (2000) 4256.
- S. Mukaigawa, T. Aoki, Y. Shimizu, and T. Kikkawa, Jpn. J. Appl. Phys. 39 (2000) 2189.
- 7) T. Kikkawa, T. Nagahara, and H. Matsuo, Appl. Phys. Lett. 78 (2001) 2557.
- T. Kikkawa, Tech. Dig. Int. Electron Devices Meet. 2000 p. 253.

## Achievements

Photonic Crystal

(Patent)

- Inventors: A. Nakajima, S. Yokoyama, M. Wake, and T. Kikkawa, "Fabrication method of stacked films with different refractive index and the patterned stack structures," Application number and filing date: 2003-081181 (H15.03.24).
- Inventor:A. Nakajima, "Organic laser and the fabrication method," Application number and filing date: 2004-099015 (H16.03.30).

Scaled Devices

(Journal)

- A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, "NH<sub>3</sub>-annealed atomic-layer-deposited silicon nitride as a high-k gate dielectric with high reliability," Appl. Phys. Lett. 80, pp.1252-1254 (2002).
- Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Low thermal-budget ultrathin NH<sub>3</sub>-annealed atomic-layer-deposited Si-nitride/SiO<sub>2</sub> stack gate dielectrics with excellent reliability," IEEE Electron Device Lett. 23, pp. 179-181 (2002).
- 3) K. Kawamura, T. Kidera, A. Nakajima, and S. Yokoyama, "Coulomb blockade effects and conduction mechanism in extremely thin polycrystalline-silicon wires," J. Appl. Phys. 91,pp. 5213-5220 (2002).
- 4). Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Reliable extraction of the energy distribution of Si/SiO<sub>2</sub> interface traps in ultrathin metal-oxide-semiconductor structures," Appl. Phys. Lett. 80, pp. 3952-3954 (2002).
- 5) Y. Ito, T. Hatano, A. Nakajima, and S. Yokoyama,

"Fabrication of Si single-electron transistors having double  $SiO_2$  barriers," Appl. Phys. Lett. 80, pp. 4617-4619 (2002).

- 6) A. Nakajima, Y. Ito, and S. Yokoyama, "Conduction mechanism of Si single-electron transistors having an one-dimensional regular array of multiple tunnel junctions," Appl. Phys. Lett. 81, pp. 733-735 (2002).
- 7) Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "High quality NH<sub>3</sub>-annealed atomic Layer Deposited Si-nitride/SiO<sub>2</sub> Stack Gate Dielectrics fo Sub-100nm Technology Generations," Solid State Electron. 46, pp. 1659-1664 (2002).
- A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kidera, and S. Yokoyama, "Low-temperature formation of highly-reliable silicon-nitride gate dielectrics with suppressed soft-breakdown phenomena for advanced complementary metal-oxide-semiconductor technology," J. Vac. Sci. & Technol. B 20, pp. 1406-1409 (2002).
- 9) A. Nakajima, T. Kidera, H.Ishii, and S. Yokoyama, "Atomic-layer deposition of ZrO<sub>2</sub> with a Si nitiride barrier layer," Appl. Phys. Lett. 81, pp. 2824-2826 (2002).
- 10) Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "Response to "Comment on 'Reliable extraction of the energy distribution of Si/SiO<sub>2</sub> interface traps in ultrathin metal-oxide-semiconductor structures" [Appl. Phys. Lett. 81, 3681 (2002)]", Appl. Phys. Lett. 81, pp. 3683-3684 (2002).
- 11) A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, and S. Yokoyama, "Atomic-layer-deposited silicon-nitride/SiO<sub>2</sub> stack ---- a highly potential gate dielectrics for advanced CMOS technology," Microelectronics Reliability 42, pp.1823-1835 (2002) (Introductory Invited).
- 12) A. Nakajima, Q.D.M. Khosru, T. Kasai, and S. Yokoyama, "Carrier Mobility in p-MOSFET with Atomic-Layer-Deposited Si-Nitride/SiO<sub>2</sub> Stack Gate Dielectrics," IEEE Electron Device Lett. 24, pp. 472-474 (2003).
- 13) A. Nakajima, Q.D.M. Khosru, T. Yoshimoto, T. Kasai, and S. Yokoyama, "High Quality Atomic-Layer-Deposited Ultrathin Silicon-Nitride Gate Dielectrics with Low Density of Interface and Bulk Traps," Appl. Phys. Lett. 83, pp. 335-337 (2003).
- 14) H. Ishii, A. Nakajima, and S. Yokoyama, "Growth and electrical properties of atomic-layer deposited ZrO<sub>2</sub>/Si-nitride stack gate dielectrics," J. Appl. Phys. 95, pp.536-542 (2004).
- 15) T. Kitade and A. Nakajima, "Application of highly doped Si single-electron transistors to an exclusive-NOR operation," Jpn. J. Appl. Phys. 43, pp. L418-L420 (2004).

(Proceedings)

16) A. Nakajima and S. Yokoyama, "Atomic-layer-deposition of Si nitride and ZrO<sub>2</sub> for gate dielectrics," Abst. AVS Topical Conference on Atomic Layer Deposition (ALD 2002) (Seoul, August 19-21, 2002) pp. 6-6 (**Invited**).

- 17) Q.D.M. Khosru, A. Nakajima, T. Yoshimoto, and S. Yokoyama, "A novel method for extracting the energy distribution of Si/SiO<sub>2</sub> interface traps in ultrathin oxide MOS structures," presented in the Second IEEE Conference on Nanotechnology (Washington, D.C., August 26-28, 2002).
- 18) Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "Time-dependent breakdown of ultrathin SiO<sub>2</sub> gate dielectrics under static and dynamic stress," Abst. 2nd ECS Int. Semiconductor Technology Conf. (Tokyo, September 11-14, 2002), Abstract No.71.
- 19) H. Ishii, T. Kidera, A. Nakajima, and S. Yokoyama, "Atomic-layer deposition of ZrO<sub>2</sub> with a Si nitiride barrier layer," 2002 Int. Conf. on Solid State Devices and Materials (Nagoya, September 17-19, 2002), pp. 452-453.
- 20) Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "A comparative study of bulk and interface trap generation in ultrathin SiO<sub>2</sub> and atomic-layer-deposited Si-nitride/SiO<sub>2</sub> stack gate dielectrics," Forth Int. Symposium on Control of Semiconductor Interface (ISCSI-IV) (Karuizawa, October 21-25, 2002) pp. A6-3-A6-3.
- 21) Q.D.M. Khosru, A. Nakajima, and S. Yokoyama, "An Effective Method for Obtaining Interface Trap Distribution in MOS capacitors with Tunneling Gate Oxides", Proceedings 2002 IEEE Int. Conf. on Semiconductor Electronics (ICSE 2002) (Penang, December 19-21, 2002) pp. 402-406.
- 22) T. Kitade, K. Ohkura, and A. Nakajima, "Periodic Coulomb oscillation in highly doped Si single-electron transistor," 2003 Int. Conf. on Solid State Devices and Materials (SSDM2003)(Tokyo, September 16-18, 2003) pp. 584-585.
- 23) A. Nakajima, H. Ishii, T. Kitade, and S. Yokoyama, "Atomic-Layer-Deposited Ultrathin Si-Nitride Gate Dielectrics ---A Better Choice for Sub-tunneling Gate Dielectrics---," Technical Digest of the 2003 IEEE International Electron Devices Meeting (Washington, D.C., Dec. 8-10, 2003) pp.657-660.
- 24) A. Nakajima and S. Yokoyama, "Atomic-layer-deposition of ultrathin Si Nitride for sub-tunneling gate dielectrics---," to be presented at ECS Symposium I1: First International Symposium on Dielectrics for Nanosystems (Honolulu, Hawaii, October 3-8, 2004) (Invited).
- 25) T. Kitade, K. Ohkura, and A. Nakajima, "Room temperature operation of an exclusive-OR cuircuit using highly doped Si single-electron transistors," submitted to 2004 Int. Conf. On Solid State Devices and Materials (SSDM2004).

(Book)

26) A. Nakajima,"Silicon Quantum Dots," Encyclopedia of Nanoscience and Nanotechnology," H.S. Nalwa (ED.), U.S.A., American Scientific Publishers, USA, 2004, ISBN:1-58883-001-2.