To Improve HiSIM-SOI for Real Application

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1. Research Target

SOI-MOSFET is a candidate for next generation integrated circuit technology due to its reduced junction capacitances and improved subthreshold swing. However, to utilize the technology for circuit application, a robust circuit model is needed. A complete surface-potential based fully depleted SOI-MOSFET model for circuit simulation has been developed by our group and is named HiSIM-SOI [1, 2]. This model considers device features explicitly as well as preserves the charge conservation. To improve HiSIM-SOI for real application is the purpose of this present work.

2. Research Results

One problem focusing now is the influence of bulk oxide thickness on the device performances. The bulk oxide thickness has the effect on body effect factor and in turn on threshold voltage. If the thickness of bulk oxide is very thin then the body effect factor increases. But this increased body effect factor increases the parasitic capacitance between the drain and substrate as well as drive current is degraded mainly due to vertical electric field.

The effect of the bulk oxide thickness and the bulk impurity concentration has been analyzed for fully depleted SOI-MOSFET. Besides, Drain Induced Barrier Lowering (DIBL) effect of SOI-MOSFET has also being investigated. The investigation is done with the 2D device simulator MEDICI. Results are shown in Figs. 1-3. Figs. 4-6 show simulation results characterizing the body effect factor.

3. Summary

The DIBL as well as the body effect factor are found to be very sensitive to device parameters, such as the bulk oxide thickness.

4. Future Plan

The simulation study will be analyzed to develop models describing the phenomena.

References

[1] D. Kitamaru, Y. Uetsuji, N. Sadachika, and M. Miura-Mattausch, “Complete Surface-Potential-Based Fully-Depleted Silicon-0n-Insulator Metal-Oxide-Semiconductor Field-Effect-Transistor Model for Circuit Simulation,” Jap, J. Appl. Phys., 43, pp. 2166-2169, 2004.

[2] N. Sadachika, Y. Uetsuji, D. Kitamaru, H. J. Mattausch, M. Miura-Mattausch, L. Weiss, U. Feldmann, and S. Baba, “Fully-Depleted SOI-MOSFET Model for Circuit Simulation and Its Applications to 1/f Noise Analysis,” Proc. Simulation on Semiconductor Processes and Devices, 2004.

Fig.1: Tsoi and Tbox dependence

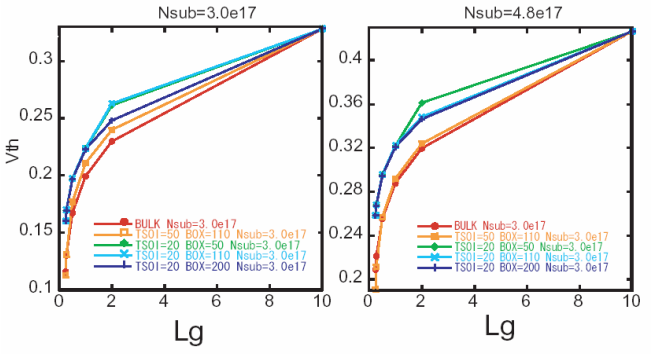

Fig.2: impurity-concentration dependence

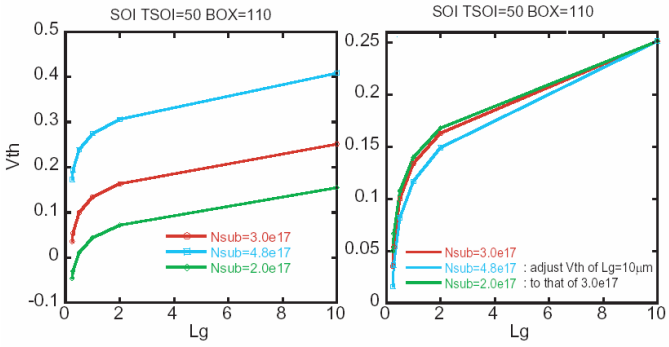

Fig.3: impurity-concentration dependence

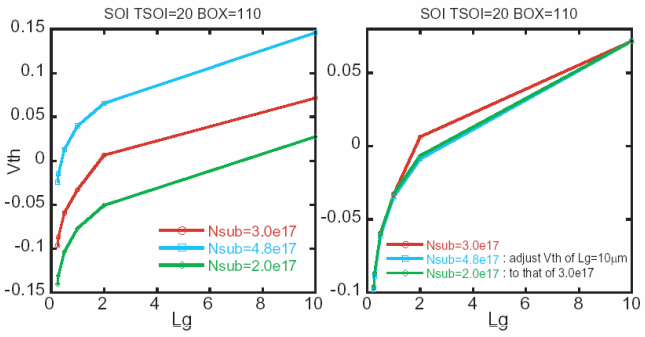

Fig.4: Vth-Vbs characteristics-1

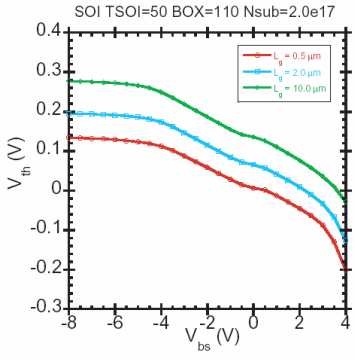

Fig.5: Vth-Vbs characteristics-2

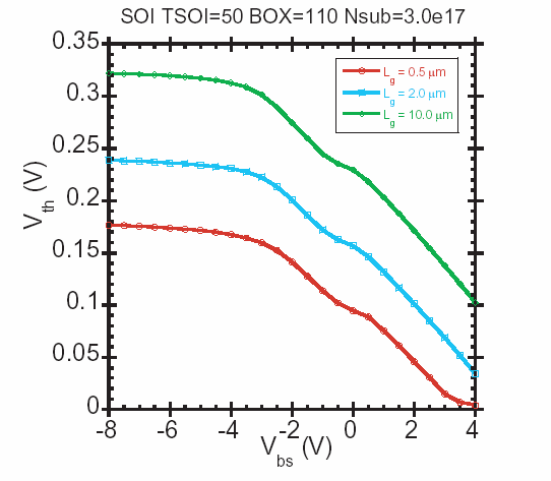

Fig.6: Vth-Vbs characteristics-3