Recent Progress of the COE

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Concept of the 21st Century COE

The concept and recent progress of the COE on **"Nano-electronics for tera-bit information Processing"** are described. The scientific staff of RCNS and the cooperating member of the Graduate School of Advanced sciences of Matter extend their world-class research position, and form the COE for innovative research and education on Nano-electronics. The features of the COE are to fuse the 3 research fields of (1) circuit design and system architecture, (2) device molding, and (3) nano-devices and processing. Fusing these research fields, a unique three dimensional integration technology (3DCSS: 3D custom stack system) utilizing wireless interconnects and optical interconnects has been proposed and its technology basis has been developed. By utilizing the 3DCSS, highly intelligent image recognition systems with learning capability and a robot brain with strategy learning are developed.

Progress of the COE

The research cooperation has started aiming at the fusion of the research fields. The researches for combining (1) high frequency MOS device modeling and RF circuit design, and (2) radio wave transmission system and antenna structure have progressed. The research on the system level such as the image processing using associative memory, bio-inspired visual processing architecture utilizing wireless interconnection has started. Furthermore, the research efforts on new devices and fabrication technologies for implementing 3 dimensional integration systems have also progressed.

For publicity of the concept of our COE, the 1st International Workshop on Nano-electronics was held in March , 2003.

In 2003, we have been awarded a large Grant in Aid for basic research (S) on "3 dimensional integration architecture using radio communication between chips for high recognition processing system", and many other grants. COE members have also accomplished cooperative research projects with public laboratories and companies.

Researchers and educational organization

An important aim of the COE is to bring-up a large number of young researchers, capable of doing self-defined and independent high-quality research, through the participation in leading-edge research programs of the COE. For this purpose, we will establish the new department of "**Semiconductor Electronics and Integration Sciences**", in April 2004, in the Graduate School of Advanced Sciences of Matter, Hiroshima University. We have already developed a new program for high-level education through advanced research and practical training.

The COE has advertised for postdoctoral COE researchers and employed 9 persons (3 foreigners) as additional core members of the COE in 2003. We also employ 6 doctoral course students as COE researchers. Our plan is to increase the COE researchers to 20 for postdoctoral researchers and to 16 for doctoral students in 2004.

Major Achievements

1. MOSFET Model: *HiSIM* for high frequency operation and the SOI structure has been developed. Its concept is to describe devices in accordance with basic physical principles. An 0.18um-CMOS testchip with RF-MOS devices and a voltage controlled oscillator (VCO) was designed and measured for evaluating the HiSIM model in the GHz frequency region.

2. Wireless Interconnection: Radio wave propagation through a silicon substrate was measured using integrated dipole antennas. A 20GHz radio wave propagates with low loss through a highly resistive Si substrate made by the proton implantation. This technology realizes the new 3 dimensional integration utilizing chip-to-chip wireless global interconnects for system clocks and buses for bi-directional data transfer and broadcasting.

Another complementary solution for wireless interconnects using resonant coupling of a spiral inductor pair was proposed. It realizes low power multi-giga bit/s wireless interconnects with highly parallel multi-channel communication suitable to transfer 2D data such as visions and neural information.

3. Associative memory based learning algorithm and integration of learning capability have been developed. They are applicable to detection and recognition of various objects after image segmentation.

4. Multi-chip vision system architecture is proposed using PWM signals and wireless interconnection. Image recognition based on the Principal Component Analysis was also studied, and its applicability to multi-object recognition systems has been confirmed.

5. New MOS devices using new structures and materials, three dimensional MOS devices on SOI as well as, single metal-gate CMOS devices using the metal work function control are under investigation.

6. Opto-electronic merged technology:

Optical waveguides using EO materials were proposed for implementing an optical switch using resonance. Floating gate devices with multi-layer quantum dot structure have been successively fabricated, and single electron charging behavior has been studied. Its application to a direct-optical-writing memory device is also proposed.

Summary

Fusing the research fields, new interdisciplinary fields are formed, and innovative knowledge is obtained in Nano-electronics. Young researchers are grown up into people of acute vision and executive ability.

Concept of the COE

Research:

1. Merging and Unification of R&Ds on silicon-based system, circuit,device-modeling and device-fabrication
2. Solution for the 3-dimensional-integration problem by **wireless interconnect technology**
3. Realization of integration systems with high-level recognition and learning capabilities

Education:

We are intending to bring up highly-capable human resources: PhD researchers who are capable of advanced, visionary and well reflecting research, in a broad range of fields, by the cooperative research.

Three Core Research Fields

I. Circuit and System Architecture

1. RF analog circuits (Prof. Iwata and Prof. Sasaki)
2. Associative-memory based systems with recognition and learning capability (Prof. Mattausch and Prof. Koide)
3. Processing system with highly cognitive level (Prof. Iwata)

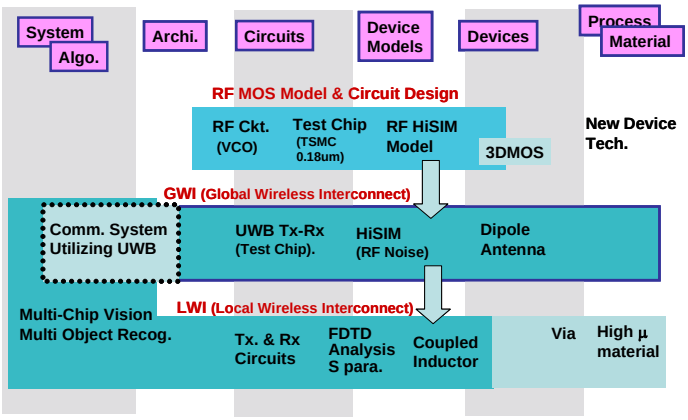
II. Device Modeling

1. Integration of electron and optical devices
2. Three Dimensional SOI-MOS device (Prof. Miura and Dr. Ueno)

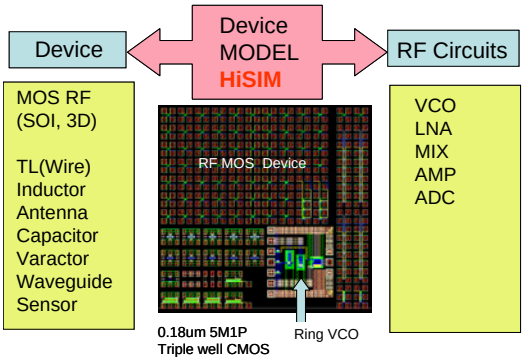
III. Nanodevice and Process

1. Fundamental device scaling techniques (Prof. Shibahara and Prof. Miyazaki)
2. Ultra-small SOI-MOS devices (Prof. Sunami and Prof. Miura)
3. Functional nano-devices (Prof. Miyazaki Prof, Higashi and Mr. Murakami)
4. Wireless interconnection (Prof. Kikkawa and Prof. Sasaki)
5. Optical interconnection (Prof. Yokoyama and Prof. Nakajima)

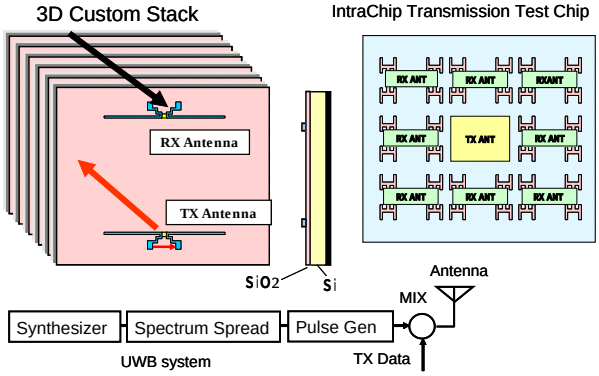
Research Collaboration for fusing Tech. Area



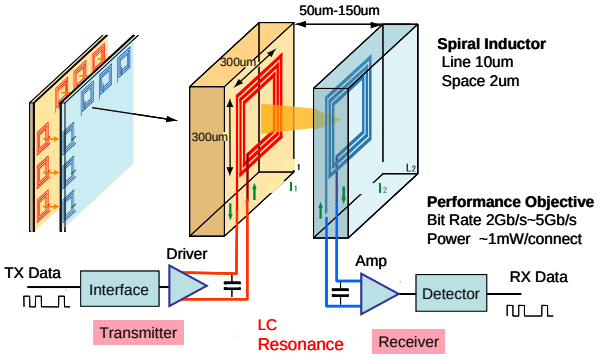
1st Test Chip for modeling RF MOS and RF Circuits



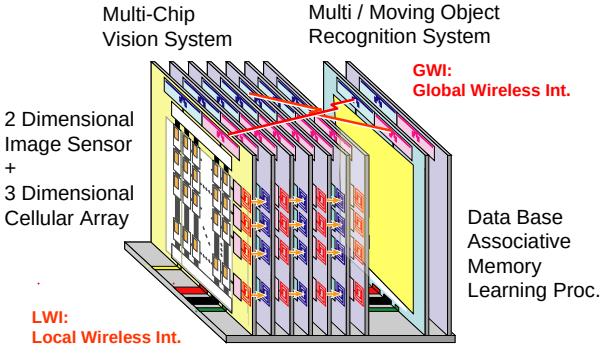
Global Wireless Interconnect using Si Integrated Antenna and UWB Communication



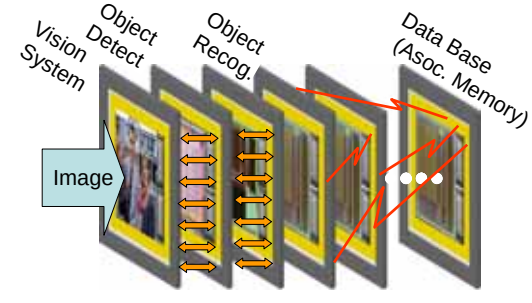
Local Wireless Interconnect using Resonant Coupling



3DCSS Structure utilizing GWI and LWI



Multi Object Recognition System Conf. and Data Flow



LWI : 2D Image Data, Detected Features, Object Data

GWL: System Ctr. Memory,Learning Matching