LOW POWER SOC TECHNOLOGY DEVELOPMENT AT STARC

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ABSTRACT

Low power SoC technology, which realizes ubiquitous computing era, is investigated. Low voltage operation of 0.5V for logic and memory IPs and 1.0V operation for analog IP are target techniques. Such low voltage logic, memory and analog IPs are to be implemented in a single chip to realize super low power SoC.

INTRODUCTION

Low power technology group of STARC [1] started in 2001 as the group that conducts R and D of low power technology of SoC using 90nm CMOS technology. The group is supported by project ASUKA[2] which is founded Japanese 11 semiconductor companies. This paper describes a scope of our research project and introduces some of our low power technologies. We are focusing on low voltage operation of CMOS circuits. A block diagram of SoC using 90nm CMOS technology is shown in Figure 1.

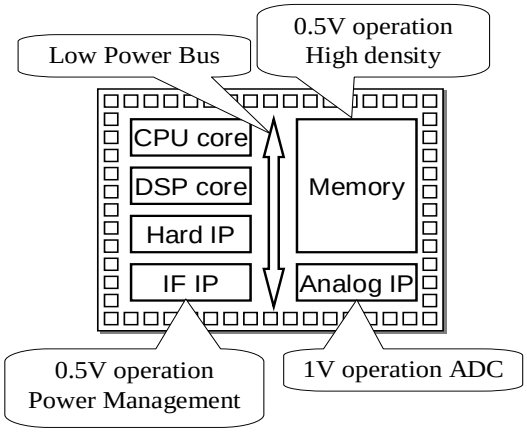

FIGURE 1 STRUCTURE OF SOC IN 90NM TECHNOLOGY

There are various blocks such as a CPU core, a DSP core and hard IPs for digital IPs. Except for the digital IPs, high density memory and analog IP are put on the SoC. The IPs are tied through on chip bus. Our strategy is to reduce the operating voltage down to 0.5V for digital and memory IPs. The operating voltage of analog IP is also reduced to 1V. This low voltage operation of an analog IP block enables not only low power operation but high performance of the IP block. The concept of the low voltage operation for each IP blocks is described in the following chapters.

DIGITAL IPS

Power of digital circuit is described in the following equation as

$$P = NaCV^2f + Nt\, I_L V \qquad (1)$$

where, P is power of SoC, Na is number of active node, C is capacitance of the active node, V is supply voltage, f is frequency, Nt is number of total node, I_L is leakage current. The first term is power for active node, and the second term is that for leakage currents. It is well known that low supply voltage is effective to reduce the power of digital circuits because the active power is proportional to V squared. However, the leakage currents increase as technology is advanced and supply voltage is reduced. Therefore, the second term of Eq.(1) increases. There are three leakage-current paths in 90nm node device as shown in Fig. 2.

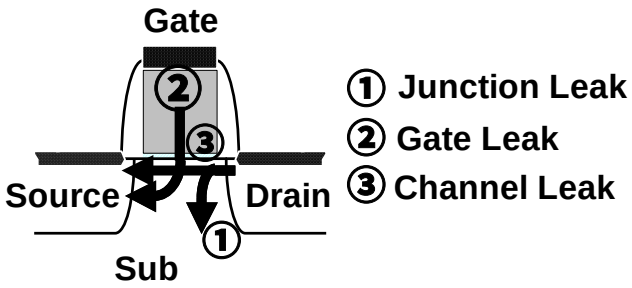

FIGURE 2 LEAKAGE-CURRENT PATHS OF A MOS TRANSISTOR

The first one is leakage current from drain to substrate due to junction leakage current as well as gate induced drain leakage(GIDL), the second leakage current flows from gate to source due to tunneling phenomena through gate oxide. The third path is from drain to source due to low threshold voltage. The leakage current through the third path is enhanced by drain voltage, this phenomena is called as drain induced barrier lowering (DIBL). As for the junction leakage and gate leakage currents, the leakage currents can be drastically decreased when the supply voltage is reduced from 1.2V to 0.5V by one to two orders of magnitude, because the electric field in the drain region and gate dielectrics is reduced. As for the channel leakage current, the DIBL effect is also relaxed by the reduced electric field. Therefore, only the leakage current we must care for is subthreshold current.

Body bias controlling method is known as technique to control the subthreshold current, because the threshold voltage is changed by the body voltage[3,4]. As shown in Figure 3, when the frequency must be high, the body voltage is controlled to be high value, while the body voltage stays at low level at low frequencies. Such controlling method has a potential to reduce the subthreshold leakage current. We have estimated the effect of this technique based on the data of the test chip using 0.13um CMOS technology. The power could be reduced to 1/5 by using this substrate bias control technique[5].

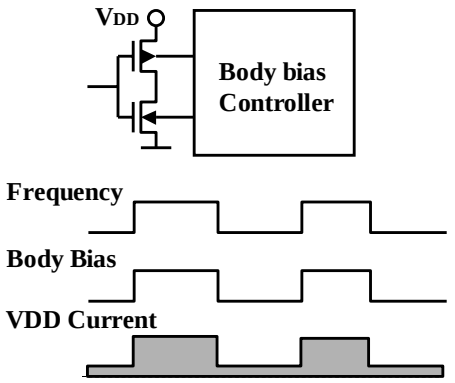

FIGURE 3 CONCEPT OF BODY BIAS CONTROL METHOD

ANALOG IPS

Since it is hard to achieve low voltage operation for analog circuit, the supply voltage stays constant value of 2.5 or 1.8V, even that for logic circuits is reduced to 1V at 90nm CMOS technology. Therefore, analog IPs cannot receive benefit from high performance transistors which are used in logic circuits. We are targeting low voltage operation of analog circuit, thereby analog circuit attains high performance.

We have investigated high speed ADCs for a driver of analog IPs. We have developed a 1.2-V calibration comparator array for a Flash-type ADC using 0.13-um generic CMOS technology. The developed offset calibration technique corrects the offset mismatch better than 6-bit resolution. By employing an offset calibration circuit in the com-parator array, the comparator array can operate at low supply voltages. To evaluate the comparator array, a 4-bit Flash-type ADC was fabricated that occupies 0.198 mm.2 With a 1.2-V power supply, it achieves 4.0 GSam-ple/s and consumes 182 mW[6].

The calibration comparator array is composed of a variable reference array (VRA), trigger comparator arrays (TCA), counter/operation circuit, and SW controller, is shown in Figure 2. The VRA generates the variable reference voltage by selecting the switches connected to the resistor array. The TCAs, TCA1 and TCA2, located at the end of the regular comparator array are composed of four comparators which reference terminal is connected to Vref_top or Vref_btm directly. The counter/operation circuit operates which switch should be selected by using the data from regular comparator array and TCAs. The resolution is defined by choosing the number of resistor. In the case of n-bit Flash-type ADC, the resistor array is composed of 2^n resistors, generally. Accordingly, to get m times resolution, $m2^n$ resistors are needed. The adjustable range is defined by choosing the number of switches connected to reference terminal of each comparator.

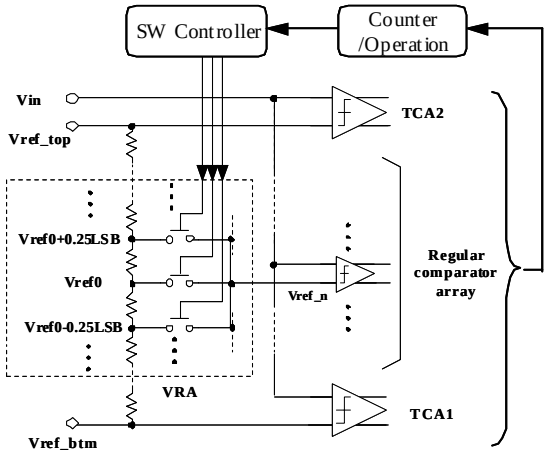

FIGURE 4 ARCHITECTURE OF OFFSET CANCEL CIRCUIT
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CONCLUSION

Low power SoC technology is investigated in low power technology of STARC founded by project ASUKA. Low voltage operation of 0.5V for logic and memory is investigated to achieve low power operation down to 1/200 of current level. Low voltage operation of 1.0V for analog circuit will enable high speed ADC. Such low voltage logic, memory and analog IPs are to be implemented in a single chip to obtain low power SoCs which will realize ubiquitous computing era.

REFERENCES

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