CDMA Communication Chips for Highly Flexible Robot Brain

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1. Introduction

Various serial interface standards, e.g., USB, IEEE-1394, etc have been established for multimedia applications. However, they do not have sufficient feature for robot control systems, in which various sensors, imagers, actuators and processors are connected as network. The robot control network requires real-time communication so as satisfy the restriction on the sampling time. Furthermore, it has communicate various amount of data, e.g., commands to the actuators being little amount and huge image data from the imagers, etc. In addition, the network should be implemented with a few wiring lines, so that the actuators can smoothly move.

We propose a communication scheme suitable for the robot control system. A key idea is CDMA serial communication [1][2]. The CDMA technique is used for data multiplexing and it realizes many virtual paths on the single wiring.

2. TDMA vs. CDMA

In CDMA communication, bit data are encoded by a spread code and the encoded signal is sent from the transmitter, as shown Figure.1. In the receiver, the data can be obtained by decoding the received signal. The decoding is a correlation operation between the received signal and the same code as used in the transmitter.

In order to show that CDMA is suitable for robot control system, the performance of CDMA is compared with two types of TDMA. The packet sizes of two TDMAs are 200bit and 10kbit, respectively. Conditions of the comparison are shown in Table 1. The event data mean hard real-time data, such as system interrupt. When a needed bandwidth is reserved for the typical real-time data, the bandwidth for the event data will be restricted as shown in Figure.2. The reserved bandwidth also affects the delay time of the event data. Figure.3 shows the relationship between the maximum delay time of the event data and the reserved bandwidth. As shown in Figs.2 and 3, CDMA gives the wider bandwidth to the event data, and the event data can be sent within shorter delay time by CDMA.

3. CDMA Receiver Chip and Measurement

Figure.4 shows a block diagram of the CDMA receiver chip. The received differential-signal is de-interleaved by wave samplers. The number of the wave samplers is equal to the length of the spread codes. The MUX and the voltage- controlled delay circuits are needed for the synchronization.

The receiver chip was fabricated in a 0.25um standard digital CMOS technology to demonstrate a 2.0Gbps, 7 multiplexing CDMA serial link. The 2.4mm X 4.0mm die photo is shown in Figure.5. The chip is packaged in a 160-pin QFP plastic package. The size the I/O bond pads is 70um X 70um. The amplitude of the transmitted differential signal for one code is set to 100mVp-p and the multiplexed wave has 800mVp-p swing because the number of multiplex codes is 8. The multiplexed transmitter signal has been generated by an arbitrary waveform generator AWG710, in measurement. Because the 2Gbps signal is de-interleaved into the 8 wave samplers, the decoders operate at the 250MHz system clock. The ring oscillator consists of 8 stages. The 8 clocks, which control the 8 wave samplers, are supplied from the 8 stages of the ring oscillator. The first one of the 8 clocks works also as the system clock. In order to adjust the phases of data in the 8 wave samplers to the phase of the system clock, 3 stages of S/H circuits working as master-slave are prepared. The system clock and the above S/H circuits are not described in Fig.4 to avoid the complication.

Figure 6 shows the measurement results of the first one of the sampler clocks after MUX, in order to confirm the operation of the synchronization. The left and the right are the sampler clock during the code (bit) synchronization and during the chip synchronization, respectively. Because the clock is always shifted by MUX during the code (bit) synchronization, the 8 phases of the clock overlap each other. On the other hand, the phase is fixed during the chip synchronization. The measurement results of the differential control voltages Cnt+ and Cnt- for the voltage-controlled delay circuits are also shown in Fig.6. They are fixed at 1.9V and 0.7V during the phase of the code (bit) synchronization. The cntSW controlling the switches is also shown in Fig.6, and it indicates the point at which the phase moves from the code (bit) synchronization into the chip synchronization. Cnt+ and Cnt- are adjusted and locked in the DLL, during the phase of the chip synchronization. The receiver chip consumes 264mW at 2.5V supply.

4. Conclusions

A 2Gbps and 7 multiplexing CDMA serial interface and the receiver circuit are proposed. The key techniques of the receiver chip are the two-step synchronization and its circuit implementation. The receiver chip fabricated in a 0.25um digital CMOS technology achieves a 2Gb/s data-transfer rate and synchronization of 7 multiplex communications.

Now, we are designing a transmitter chip based on the proposed serial CDMA scheme in order to demonstrate the CDMA serial link in the completed form.

References

[1] R.Yoshimura et al. “DS-CDMA Wired Bus with Simple Interconnection Topology for Parallel Processing System LSIs,” ISSCC Digest of Tech. Papers, pp.370-371, Feb. 2000

[2] Zhiwei Xu et al. “A 2.7 Gb/s CDMA-Interconnect Transceiver Chip Set with Multi-Level Signal Data Recovery for Re-configurable VLSI Systems,” ISSCC Digest of Technical Papers, pp.82-83, Feb. 2003

Table. 1 Conditions to compare TDMA with CDMA.

Bit rate	1 Gbps
Size of event data	32 bit
Overhead of event data	8 bit
Overhead of typical real-time data	32 bit

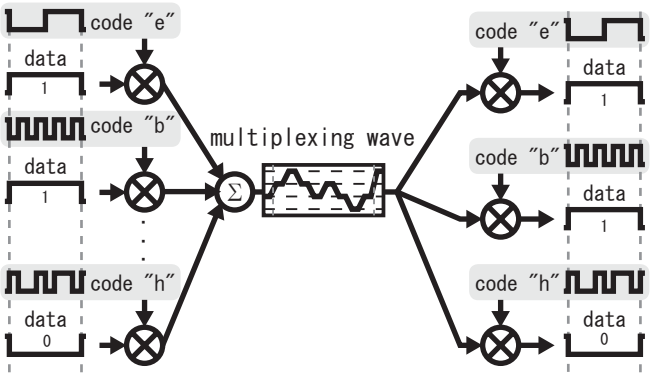

Fig. 1 CDMA technique.

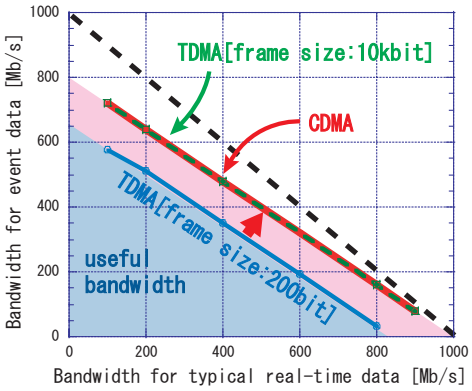

Fig. 2 Bandwidth for event data vs. Bandwidth for typical real-time data.

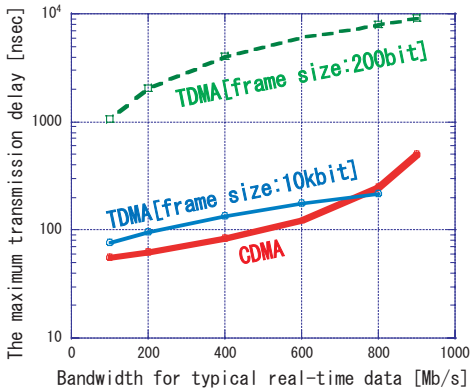

Fig. 3 The maximum transmission delay vs. Bandwidth for typical real-time data.

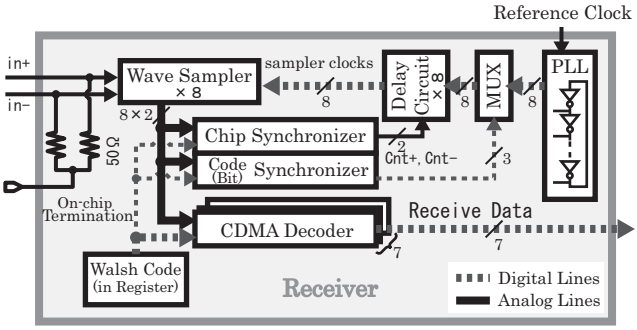

Fig. 4 A block diagram of the CDMA serial receiver chip.

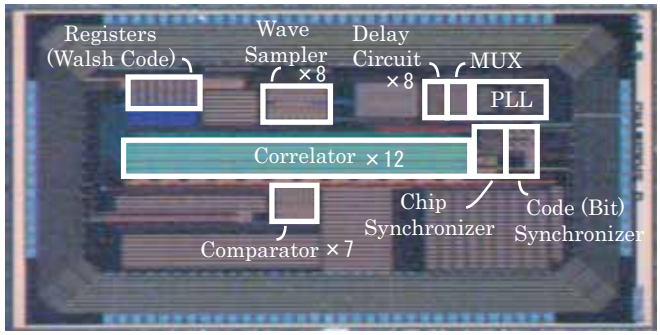

Fig. 5 Chip micrograph.

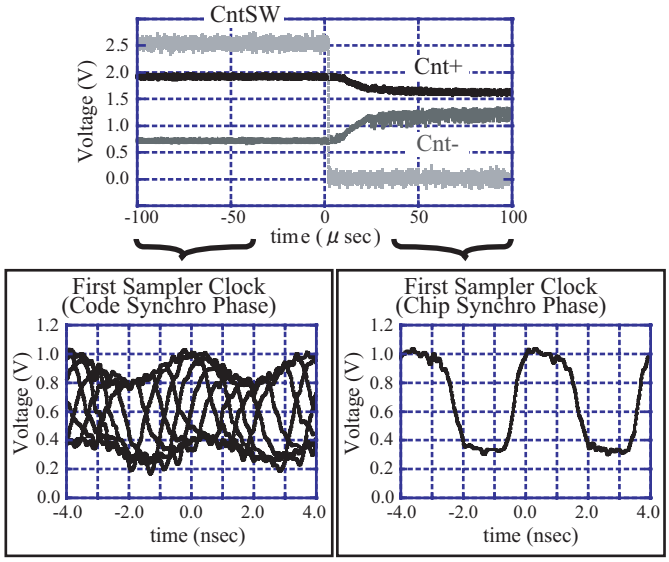

Fig. 6 Measurement results.