A Single Chip UWB Transmitter Based on 0.18 μm CMOS Technology for Wireless Interconnection

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1. Introduction

Steady downscaling of semiconductor device dimensions and the demand for System On a Chip (SOC) have led to the concept for wireless interconnection as shown in Fig. 1 within the chip and among the chips to avoid transmission delay due to parasitic resistance, capacitance and inductance of conventional wiring [1-3]. Ultra Wide Band (UWB) radio technique, which had been confined to radar and remote sensing applications for many years can be applied for efficient implementation of re-configurable interconnect for high frequency clock and data transmission among different sub-circuits within a chip or among the different chips [4]. This paper presents a single chip ultra wideband transmitter which transmits ultra wide band Gaussian monocycle. The well known time hopping spread spectrum technique with pulse position modulation is employed in UWB transmitter for multiple access capability. The time hopped pulse which contains information is then converted into monocycle for transmission. A new technique based on current CMOS technology is developed to generate monocycle. The proposed transmitter based on 0.18 μm CMOS technology is simulated by using HSPICE and results are presented in this paper.

2. UWB Transmitter

A functional block diagram of a UWB transmitter is shown in Fig. 2. In figure 2(a) $w_{tr}(t)$ represents the transmitted gaussian monocycle that nominally begins at a time of zero on the transmitter's clock. The jth monocycle generally begins at $jT_f+c_j^{(k)}T_c+\Delta d^{(k)}$. Here T_f is the pulse repetition time which is typically be a hundred to thousand times of the monocycle width [4]. In the present work the pulse width is considered to be as 0.5ns and pulse repetition time or frame clock is 20ns which is 40 times of the pulse width. These values are taken to avoid the complexity of the circuit design for initial investigation. A frame consists of a number of compartments which is occupied by one of the k^{th} users (i.e. k^{th} chip). In order to avoid the catastrophic collision in multiple accessing due to the possible occupancy of the same compartment at the same instance by the users and to spread the spectrum, each chip is assigned a distinct pulse shift pattern (c_j^k) known as time hopping code. These time hopping code is periodic with a period N_p. The time hopping code provides an additional time shift of $c_j^kT_c$ seconds to each jth pulse of the kth user. Here Tc, the controllable unit time also known as hopping period should satisfy $N_hT_c \le T_f$ to avoid any collision from next pulse N_h denotes the maximum decimal value of the hopping code. In this work three bit hopping is considered which limits decimal value of N_h from 0 to 7 and thus the number of compartment or slot in a frame is 8. An additional time shifting $\Delta d^k_{j/Ns}$ is provided to encode the data sequence corresponding to the j^{th} pulse of the k^{th} user where $d^k_{j/Ns} \varepsilon \{0\ 1\}$. Here Δ represents the modulation factor (i.e. the time interval between bit "1 " and "0") whose optimum value is a fraction of the monocycle duration. N_s represents the number of pulse repetitions per data bit yielding the actual data transmission rate $R_s= 1/N_sT_f$ bit per second.

3. Circuit Simulation Results and Discussion

The UWB transmitter is implemented using the current 0.18μm CMOS technology. The circuit schematic of UWB transmitter and chip layout is shown in Fig. 3. The VCO produces a signal of 800 MHz which is divided by 16 (by using four divide by 2 circuit) to produce a frame clock of 50 MHz. The simulated VCO output before and after divider is shown in Fig. 4. The frequency stability of the frame clock is an important factor in UWB system. Here the simulation shows that the frequency stability with change of v_{dd} and temperature is about 5% in the worst case. The seven time shifted frame is generated from frame by the precise delay lines. The delay generation circuit is based on the delay line which consists a number of buffer stages connected in series . The circuit is tapped at seven points so that a delay of 2.5ns interval with reference to frame clock can be achieved. The simulated output is shown in Fig. 5. Four Linear feedback shift registers along with an XOR logic is used to generate pseudorandom sequence. The initial shift in data is taken as [1 0 0 0]. This will repeat after the every 15^{th} cycle of the clock frequency of 400 MHz. The simulated result is shown in Fig. 6. It is observed that the generated PN sequence satisfies all its randomness properties such as balance , run and co-relation property. An eight to 1 multiplexer circuit is designed using conventional CMOS NAND and NOR gate. Multiplexer selects the time shifted frame clock according to PN sequence with three hopping bit. The HSPICE simulated multiplexer output is shown in Fig .7 . The figure shows the time shifted pulse is positioned in each slot of the frame according to the PN sequence. The time hopped signal is then shifted according to the data symbol (0 or 1). The time shifting due to PPM is done by fine delay line which gate delay is approximately the modulation time of 0.05ns. The time shifted pulse is then selected according to symbol 0 or 1 by using the 2 to 1 multiplexer. The two to 1 multiplexer output is shown in Fig. 8. For the present investigation return to zero (RZ) data signal with a width of 1.25ns is considered. The simulated time shifted pulse which contains data is shown in fig. 8. It shows that the data is placed in the desired compartment at desired position of the frame according to PN sequence and data symbol. The pulse generator circuit shown in fig. 3 produces damped sinusoidal like wave from the time shifted signal. The frequency of oscillation of the generating signal can be controlled by varying L and C values. This signal is then passed through transmission gate which is controlled by the pulse of desired width to pass the first cycle of the generated signal at the output. The proposed circuit is simulated using HSPICE. The FFT of the monocycle is shown in Fig. 10. The FFT shows that the generated monocycle has wide half power bandwidth (BW) of approximately the monocycle center frequency (.i.e 2GHz).

4. Future plan

To achieve target frequency of 20GHz, we have to modify the proposed monocycle generator by proper designing of the spiral inductor. Synchronization circuit has to be designed for clock and PN synchronization between transmitter and receiver to recover data at the receiver end. We have also plan to evaluate the bit error rate and signal to noise ratio for estimating the signal quality of the proposed wireless interconnect system.

5. Conclusion

In the proposed UWB transmitter all circuit blocks are almost digital architecture except monocycle generation circuit. However

monocycle can be generated using the current CMOS technology which has led us to implement the UWB transmitter in a single chip. Since the monocycle is generated from the time shifted pulse, it is only necessary to keep constant gate delay with any variation of vdd and substrate voltage.

Reference.

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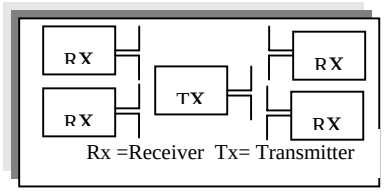
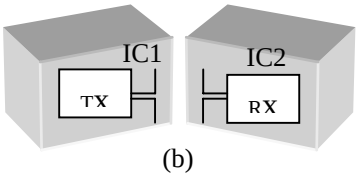
2. A B M H Rashid, S Watanabe and T. Kikkawa, JJAP, vol. 42 (2003).
3. Brian A. Floyd, Chih-Ming Hung and Kenneth K.O. IEEE Journal of Solid State Circuits, vol 37, No. 5, May 2002, PP. 543-552.
4. Moe Z Win and Robert A. Scholtz, IEEE Transactions on communications, vol 48, No. 4, April 2000, pp. 679-691.



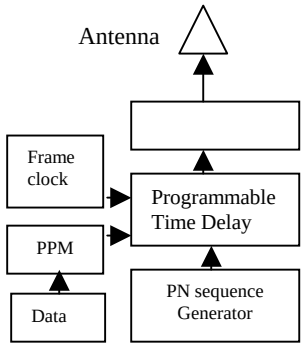
(a)



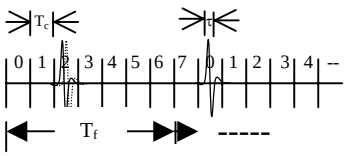
(b)

Fig. 1 Wireless Interconnection (a) Intra chip and (b) Interchip.

$$s^k(t) = \sum w_{tr}(t - jT_f - c_j^{(k)}T_c - \Delta d_{[j/N_s]}^{(k)})$$

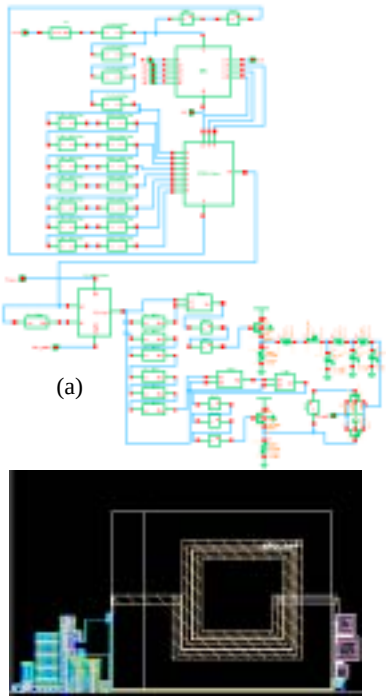


(a)



(b)

Fig.2 (a) Functional block of UWB transmitter and (b) UWB pulse train.



(a)

(b)

Fig. 3 (a) UWB Tx circuit schematic and (b) chip layout (size: 600μm x 310 μm).

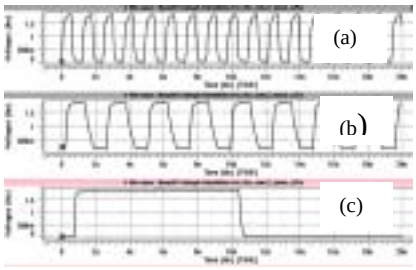


Fig. 4 VCO output (a) 800 MHz VCO output; (b) 400 MHz and (c) 50 MHz Frame clock.

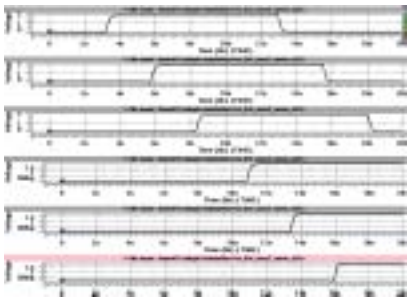


Fig. 5 Time shifted frame clock.

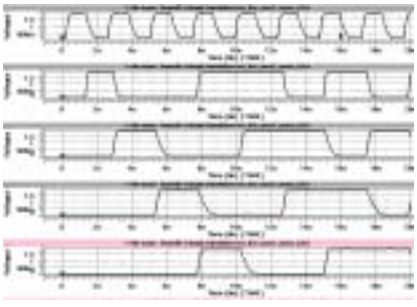
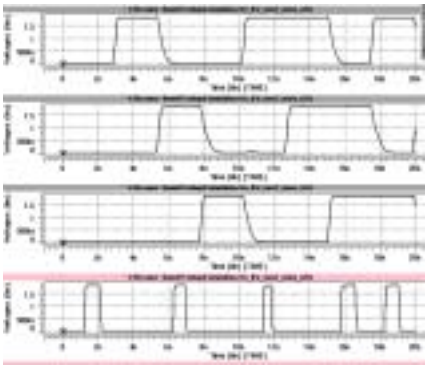
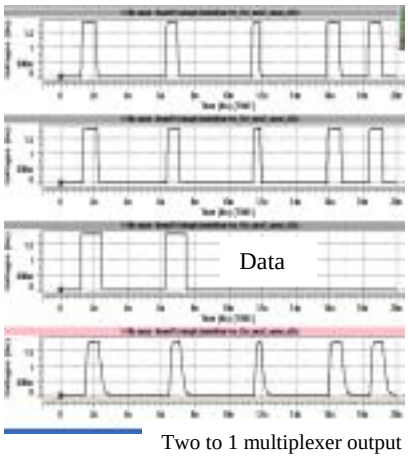


Fig. 6 PN sequence output for initial loading of [1000] and chip rate is 400 MHz.



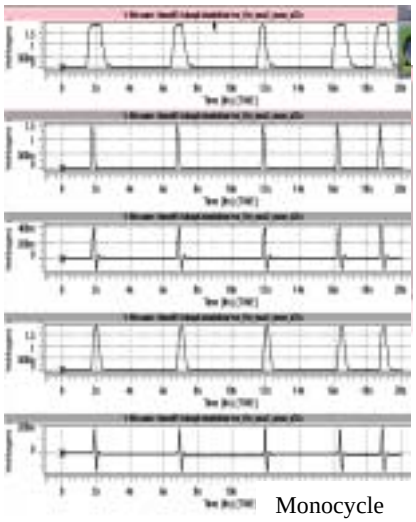
Multiplexer output

Fig. 7. Eight to 1 multiplexer output according to PN sequence with 3 hopping bit.



Two to 1 multiplexer output

Fig. 8 Time shifted pulse containing data from 2 to 1 multiplexer output.



Monocycle

Fig. 9 Monocycle containing information from UWB transmitter output.

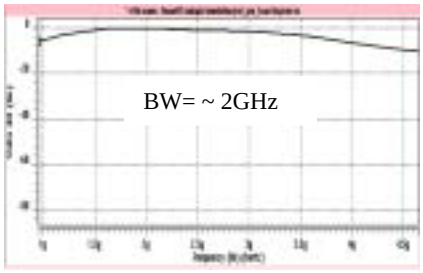


Fig. 10 FFT of transmitted Monocycle.