Three Dimensional Integration Architecture for Tera-bit Information processing

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1. Research Target

[3D integration systems]

As a promising solution for breaking Moore's law, we have proposed three dimensional integration technologies utilizing nano-devices and advanced interconnects. To realize tera-bit processing systems, inter-chip connection capability with tera-bit/s bandwidth is needed, as well as multi-chip parallel processing capability with tera-operations/s. (Fig. 1)

[Interconnection for 3D integration]

Electrical interconnections using multi-layer wirings, are extended to use transmission lines and via holes. In addition, wireless and optical interconnections are investigated. We have to consider many levels of interconnection. Table 1 shows an application map of interconnection.

We intended to realize 3D integration of multi-chips with different kinds of functions, circuits and devices. The most important technology is flexible chip-to-chip interconnections between stacked various chips. For that purpose, we have proposed two types of wireless interconnections for global clock/data transfer (GWI) and parallel interconnections between adjacent chips (LWI) as well as optical interconnection with high-speed and wideband.

[System architecture]

The target is highly sophisticated recognition system with high speed real-time image analysis capability and flexible data matching and learning functions. As new architectures to realize the system, parallel processing units with over 10GHz clock and flexible network integrating a huge amount of distributed multi-dimensional data, are required.

2. Research achievements

2.1 RF and low noise circuit design

An 0.18um-CMOS test chip with RF-MOS devices and a VCO was for the *HiSIM* model in the GHz frequency region. (In Corporation with Prof. Miura's Group)

Future artificial brain should have communication capability with living things. To realize the bio-interface, low noise analog circuits for neural signal sensing were investigated. Low noise CMOS chopper stabilization technique was established for uV level signal amplification.

2.2 Wireless Interconnection

For realizing LWI with low power dissipation, we have proposed an interconnect scheme based on resonant coupling of integrated spiral inductors. A test chip was developed with 0.25μm CMOS technology. Measured performance of 800Mb/s/ch at 9mW/ch was obtained. If we use a 90 nm device technology, 2-5Gbps data transfer with 1mW/ch. By compromising inductor size, chip thickness and power dissipation, distributed data are transferred in highly parallel between neighboring chips. (Table 2)

2.3 Three dimensional integration using GWI and LWI

We call the proposed 3D integration system, 3D custom stack system (*3DCSS).* In the *3DCSS,* GWI is used for distribution of over 10GHz system clocks, bi-directional data transfer and broadcasting of data to each chip, and LWI provides highly parallel multi-channel communication.

In order to realize wide bandwidth UWB

For flexible global network for robot control, CDMA system was investigated. A CDMA serial transceiver chip with 7-multiplexed 2-Gcps and an interface board for multi-DSP was developed. (Fig. 2)

2.4 Algorithm and Architecture for 3DCSS

[Vision system based on biological processing]

In multi-chip systems, a high resolution and advanced functions are integrated by dividing circuits into separate chips. Due to the wireless connections, the 3DCSS is well-suited for realizing the multi-chip vision mimicked the vertebrate visual system. A prototype vision chip was developed with a PWM-based line parallel interconnection and confirmed it operation.

[Multi-object recognition system using 3DCSS]

For realizing real-time/high-level recognition system, a multi-object recognition system using 3DCSS was proposed. The Principal Component Analysis and eigen face method are extended to applicable to multi-object recognition. We developed a software human face recognition system. This system can operate at 10-30 frame/s and recognize one or more human faces between each frame.

Recognition block diagram of multi-object recognition system is shown in Fig.3. 3DCSS structure composed of image sensor, image normalizer, objects detector, objects recognizer and multi-object database chips are shown in Fig. 4.

[Robot Brain with multi-processor network]

The first target is to propose a strategy learning model for the Robot Brain. By extending LVQ learning algorithm, the model to create strategy of attack adaptively changing environment have been obtained. The model will be applied to architecture of brain chip for 3DCSS.

3. conclusions and future plan

A prototype 3DCSS multi-chip vision system with GWI and LWI will be demonstrated in 2005.

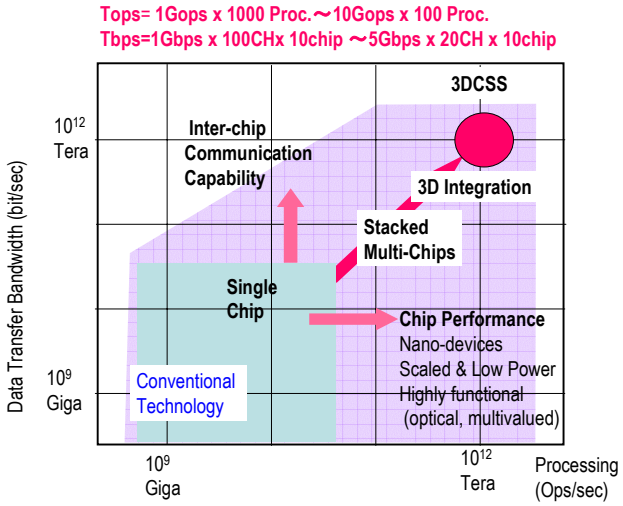

Fig.1 Target of Tera-bit Information Processing

Table 1 Interconnection Technogies for 3D Integration

	Intra-chip	Inter-chip	Assembly, chip-chip
Electrical	Multi-layer On-chip TL	Via hole	TL on PCB Coaxial Cable
Wireless		L Coupling: Short range C Couple: Short rang Rdio Wave[Antenna]: Long range	
Optical	Intergated Optical Components	Optical waveguide substrate Optical fiber	

Table 2 Comparison of chip-to-chip Local Interconnections

Connection Method	Research organization	Feature Technology	Bit rate	Power	Size
L coupling	Hiroshima Univ.	LC Resonator 0.25um CMOS	800Mbps	T: 6mW R: 3mW	L :200um D:200um
		Futer target 90nm CMOS	1.0Gbps	T: 0.8mW R: 0.2mW	L :100um D :200um
	Keio Univ. (3)	Trans Coupling 0.35um CMOS	1.2Gbps	T: 43mW R: 2.5mW	L :100um D :300um
C coupling	Univ.of Tokyo (2)	Capacitor between pads 0.35um CMOS	1.27Gbps	T+R:3mW	L : 20um D :1-2um
Via hole	Several Company (1)	Inter-layer via	～1Gbps	T+R:10mW	

(1) Burnss et al. ISSCC2001, pp.268-269, Konayagi et al.ISSCC2001,pp.270-271
(2) Kanda et al. ISSCC2003, pp.186-187
(3) Mizoguchi et al. ISSCC2004, pp142-143

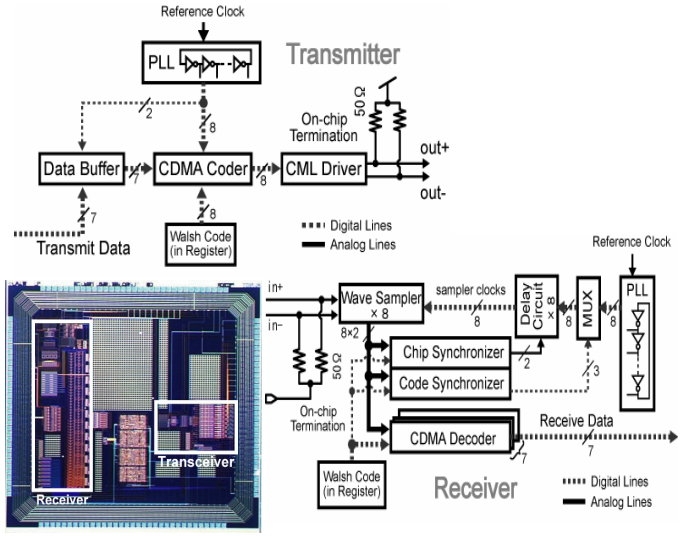

Fig. 2 CDMA Serial Communication Chip for Robot Brain Network

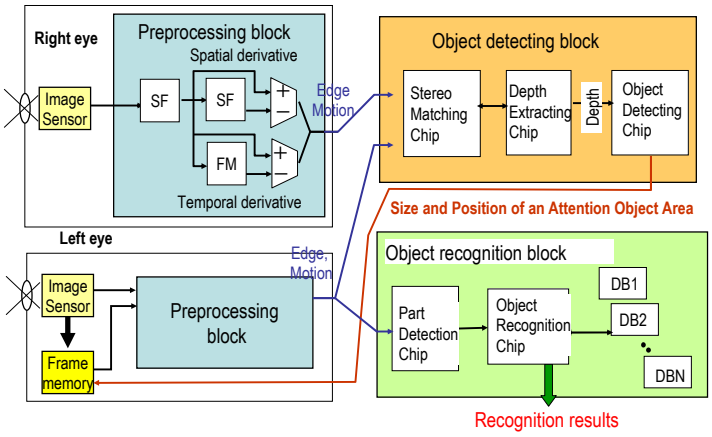

Fig. 3 Architecture of multi-object Recognition System

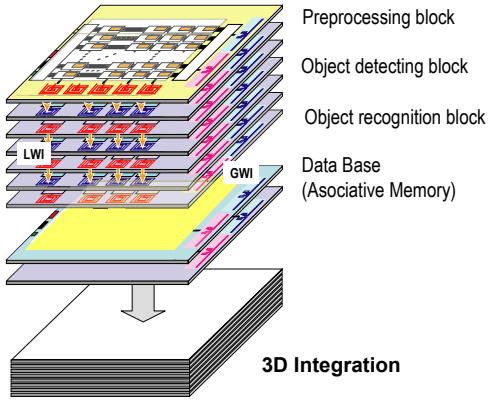

Fig. 4 Multi-Object Recognition System using 3DCSS

3D Integration Architecture for Tera-bit Information processing

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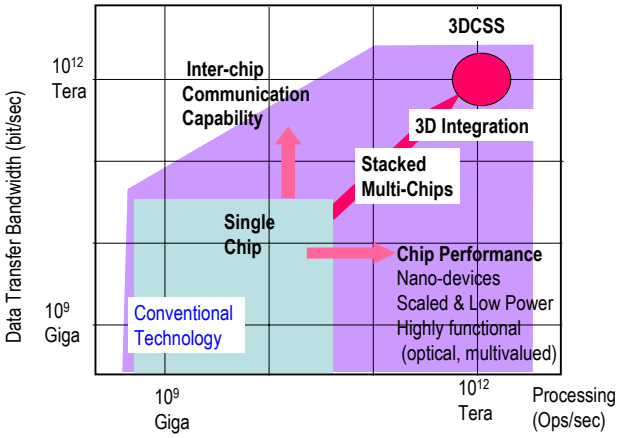
Research Target

Architecture and 3D Integration for Tera bit Information processing system



Interconnections for 3D Integration

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Comparison of chip-to-chip Interconnects

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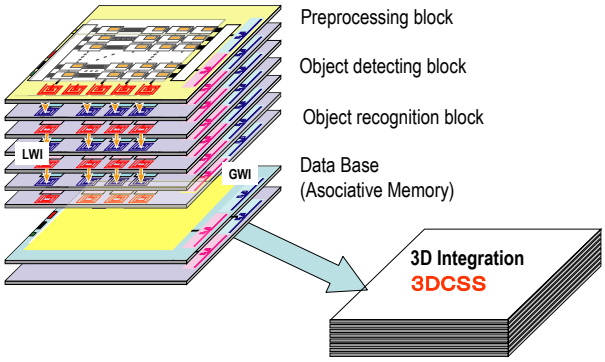
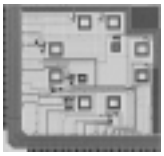
3D integration Structure of Multi-Object Recognition System

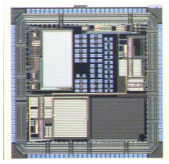


Members and Research Subjects

[Group Leader] **Atsushi Iwata,** [Sub Leader] **Mamoru Sasaki**
[Circuits for Communications] Joint Research Group

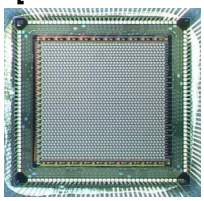


Mamoru Sasaki
Wireless Interconnect ⟺ Kikkawa Group
using Inductors



Takeshi Yoshida
Analog Circuits ⟺ STARC Project
for bio- and RF Interface
& Circuit design using HiSIM ⟺ Miura Group

[Vision and Recognition System]

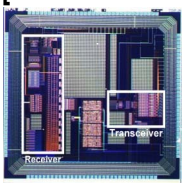


Seiji Kameda
Multi-chip Vision ⟺ Kikkawa Group
with wireless Interconnect

Hiroshi Ando
Multi-Object recognition ⟺ Mattaushe Group

Kan'ya Sasaki
Object Detection
by Stereo Visions

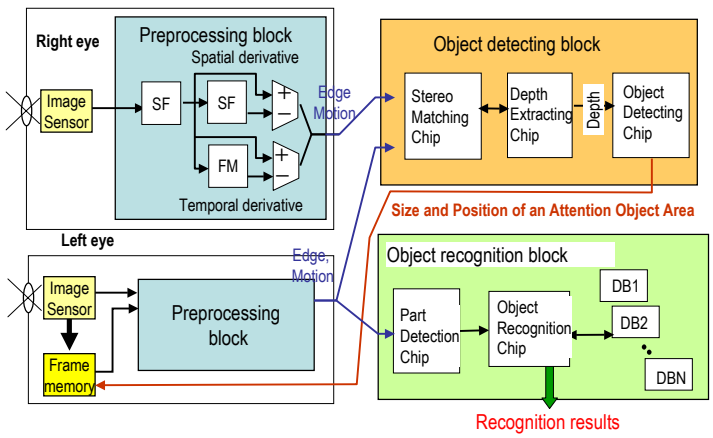
[Robot Control System] ⟺ CREST project



Mitsuru Shiozaki
CDMA Serial Interface ⟺ Kaneko Group
for Robot Control Hyper Human COE

Masahiro Ono
Learning algorithm
for Robot brain

Application Target Multi-object Recognition System



Future Plan

A prototype 3DCSS multi-chip vision system
with wireless interconnections will be demonstrated in 2005.