

A Brain-type Multi-chip Vision System with a PWM-based Line Parallel Interconnection

Seiji Kameda, Masaki Odahara and Atsushi Iwata

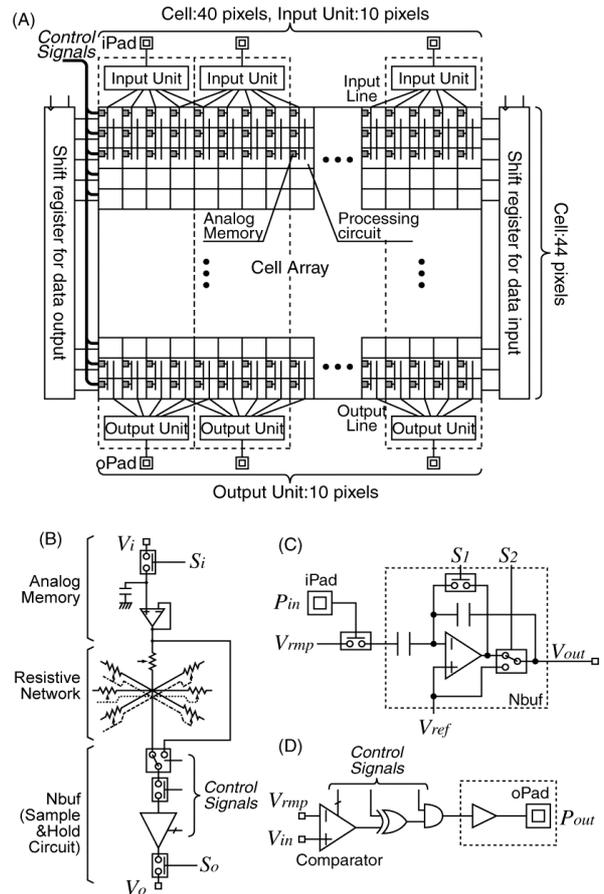
Hiroshima University, 1-3-1 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8530, Japan
Phone and Fax: +81-824-22-7358, E-mail: {kameda, msk, iwa}@dsl.hiroshima-u.ac.jp

1. Research Target

The vertebrate visual system processes huge visual information in real-time by massively parallel neural networks arranged hierarchically and adapts to a rapidly changing visual environment by an adaptive mechanism. Inspired by the unique architecture and algorithm of the vertebrate visual system, the neuromorphic vision chips or brain-type vision device, which are novel analog Very Large Scale Integrated (VLSI) circuits, have been fabricated ([1] for outlines). These neuromorphic chips, however, encounter a serious problem, namely, the trade-off between the resolution and the computational complexity of the chip. To solve the problem, multi-chip vision systems have been developed previously [2-3]. In these multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. In our 21st Century COE, a visual processing system using a 3 Dimensional Custom Stack System (3DCSS) has been proposed [4]. In the system, multiple chips fabricated by various technologies and arranged hierarchically are connected by two types of wireless connections, which are a local connection [5] and a global connection [6]. Due to the wireless connections, the 3DCSS overcomes a wiring complexity that is the demerit of the multi-chip system generally. Each of the chips has massively parallel pixel array and is able to carry out real-time image processing. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system. In the present study, we developed a prototype multi-chip vision system with a wired line parallel interconnection.

2. Prototype visual processing chip with a PWM-based line parallel interconnection

A prototype visual processing chip, that is a smoothing chip, was developed as a preliminary step toward fabrication of the visual processing system using the 3DCSS configuration [5]. Fig.1 (A) shows a block diagram of the smoothing chip. The chip consists of a cell array, a line parallel input and output units and two ramp generators. In the cell array, pixel circuits are arranged in a 44 x 40 matrix. Fig.1 (B) shows a circuit design of the single pixel. The pixel circuit consists of an analog memory, a resistive network and a sample/hold buffer, Nbuf. An input image is smoothed by the resistive network and the extent of the smoothing is controllable by external bias voltages [6]. The Nbuf is embedded to compensate for circuit offsets, which are an amplifier offset and fixed pattern noises due to statistic mismatch of transistor characteristics [6]. And the output of the Nbuf varies proportionally to the time-varying input signal; therefore, the Nbuf can serve as a subtractor circuit. Fig.1 (C) and (D) show circuit designs of the input



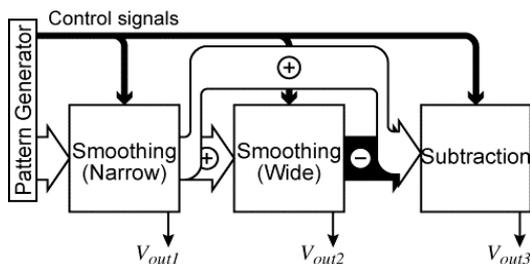
and output units respectively. The input and output units are arranged every 4 column of the cell array in a line (1 x 10) respectively, as shown in Fig.1 (A). Note that an analog output data must be converted into a digital data in order to use the wireless interconnection modules. Therefore, a pulse width modulation (PWM) method was adopted to the data transfer between adjacent chips [7]. The PWD (pulse width demodulation) input unit consists of the sample/hold circuit, Nbuf. A ramp signal is fed into the sample/hold circuit while the input pulse signal is high. And then, a ramp voltage is held into the sample/hold circuit when the input pulse signal becomes low. Accordingly, the output voltage is proportional to the input pulse width and is not influenced by the offset of the circuit feeding in nor of the sample/hold circuit itself due to using the Nbuf. The PWM output unit consists of a clocked CMOS comparator [7]. The output unit generates a pulse signal until a ramp volt-

age is equal to the input analog voltage, which is an output of the pixel. Thus, the output pulse width is proportional to the pixel output voltage. Conversion gains of the PWM and PWD are controllable by a gradient of the ramp voltage signals. The ramp signals for the input and output units are generated by the ramp generators incorporated in the smoothing chip and the gradient can be modulated by external bias voltages. The smoothing chip was implemented with a 0.35 μm , double-poly, three metals, standard CMOS technology and the die size was 4.5 x 4.5 mm^2 .

3. Multi-chip vision system for contrast enhancement filtering

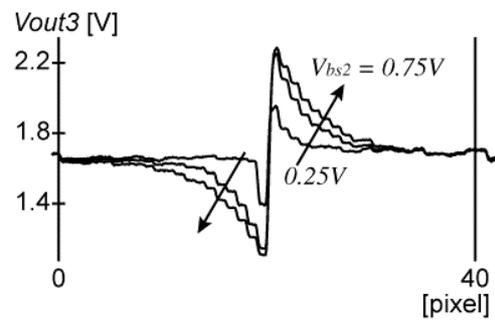
We developed a multi-chip vision system for contrast enhancement filtering using the smoothing chip. Fig.2 shows a system design of the vision system. The vision system consists of the three smoothing chips. These chips were connected by transfer bus consisting of 10 parallel lines, which was made by a wire harness. A pattern generator, Agilent 16702B, generated control signals of every chips and an input signal to the first chip. The system configuration was inspired by the outer retinal circuit in the vertebrate retina [7].

The contrast enhancement filter is obtained as follows. Firstly, an image data is fed into the first smoothing chip through the line parallel input unit. The image is smoothed weakly by the resistive network of the first chip. And the weakly smoothed image is memorized into the Nbuf array. Secondly, the weakly smoothed image is transferred to the second and third chips simultaneously through the line parallel pathway. In the second chip, the weakly smoothed image is smoothed strongly by the resistive network and the strongly smoothed image is memorized into the Nbuf array. In the third chip, the weakly smoothed image from the first chip is memorized as a reference signal of the Nbuf array without processing by the resistive network. Finally, the strongly smoothed image of the second chip is fed into the third chip through the line parallel pathway. The strongly smoothed image is input into the Nbuf array without processing by the resistive network. Here, the Nbuf takes a difference between a voltage memorized as a reference signal and a delayed input voltage. Accordingly, the Nbuf array of the third chip takes a difference between the weakly smoothed image from the first chip and the strongly smoothed image from the second chip. The receptive field of the system is approximated by the Laplacian-Gaussian filter: the filter carries out the contrast enhancement and



smoothing.

Fig.3 shows responses obtained from the multi-chip vision system. As an input signal, wide pulse width signals, 0.9 μs , were fed into the right side of the first chip and narrow pulse width signals, 0.1 μs , were fed into the left side; therefore, a pseudo black-white edge was input into the first chip. The bias voltage applied to the resistive network of the first chip, V_{bs1} , was 0.0V. The bias voltage applied to the resistive network of the second chip, V_{bs2} , was varied from 0.25V to 0.75V. The gradient of the ramp signal is 1.65V/ μs . In these figures, the horizontal axis measures the pixel position and the vertical axis measures the output voltage of 23-th row of the third chip. As shown in Fig.3, the output of the third chip shows a Mach band-like effect near the pseudo black-white edge. The receptive field size becomes wider and the response amplitude becomes larger when the bias voltage, V_{bs2} , is increased. The fluctuation is suppressed within 10 mV.



4. Conclusion and future

As a preliminary step toward development of the visual processing system, we have developed the prototype multi-chip vision system for contrast enhancement filtering using the smoothing chips with a PWM-based line parallel interconnection. In the next step, we are going to design the multi-chip system with wireless interconnection and consider visual processing algorithms.

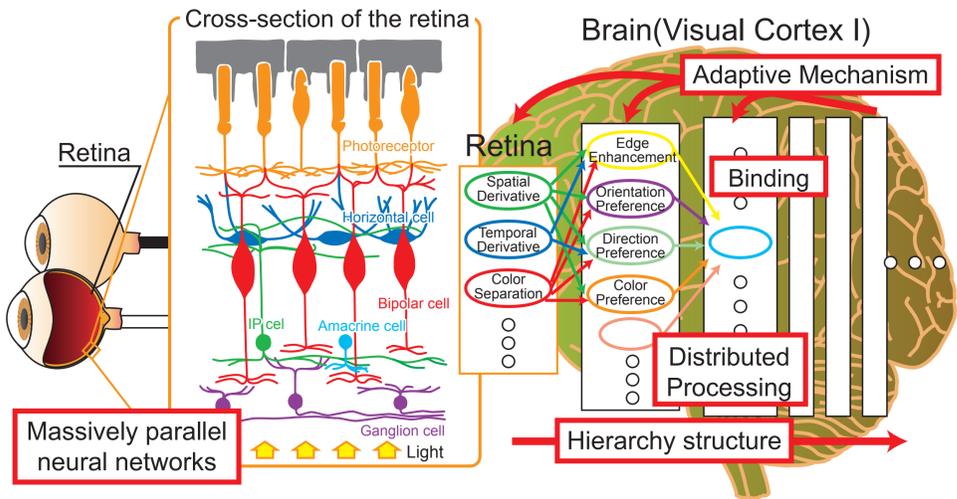
References-

- [1] A. Moini, *Vision Chips* (2000).
- [2] C.M. Higgins, *et al.*, *Analog Integrated Circuits and Signal Processing*, **24** (2000) pp.195-211.
- [3] S.-C. Liu, *et al.*, *Neural Networks*, **14** (2001) pp.629-643.
- [4] S.Kameda, *et al.*, *Proc. 2nd Hiroshima Int. Workshop on Nanoelectronics for Terra-Bit Information*, (2004) pp.74-75.
- [5] M. Sasaki, *et al.*, *Proc. 2nd Hiroshima Int. Workshop on Nanoelectronics for Terra-Bit Information*, (2004) pp.104-105.
- [6] A.B.M.H. Rashid, *et al.*, *IEEE Electron Device Letters*, **23(12)** (2002) pp.731-733.
- [7] S. Kameda, *et al.*, *IEEE Trans. Neural Networks*, **14(5)** (2003) pp.1405-1412.
- [8] A. Iwata, *et al.*, *IEICE Trans. Fundamentals*, **E84-A(2)** (2001) pp.486-496.

A Brain-type Multi-chip Vision System with a PWM-based Line Parallel Interconnection

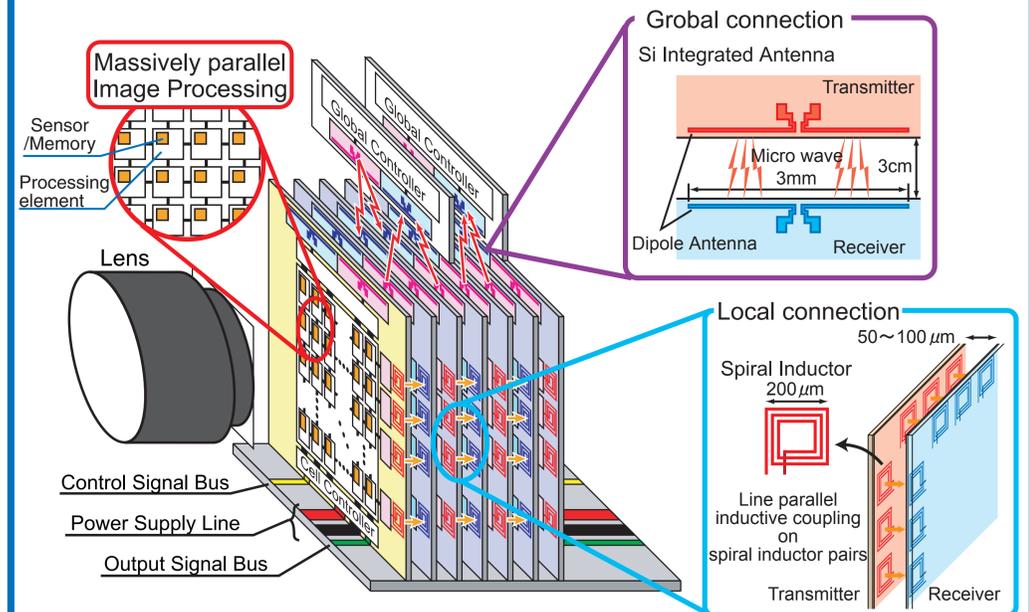
Seiji Kameda, Masaki Odahara and Atsushi Iwata Hiroshima University

Vertebrate visual system



The vertebrate visual system processes visual information **extraction** and its **binding** by **massively parallel** neural network arranged **hierarchically** in **real-time** and **adapts** to a rapidly changing visual environment by an **adaptive mechanism**.

Visual processing system using 3-Dimensional Custom-Stack System



Power of the **3-D integration** is demonstrated by **engineering realization** of the **architecture and algorithm** of the vertebrate visual system

Smoothing Chip with a PWM-based Line Parallel I/O

A prototype visual processing chip, a **smoothing chip**, was developed as a **preliminary step** toward fabrication of the visual processing system using the **3DCSS** configuration

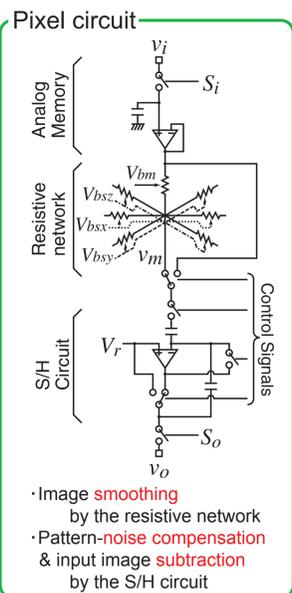
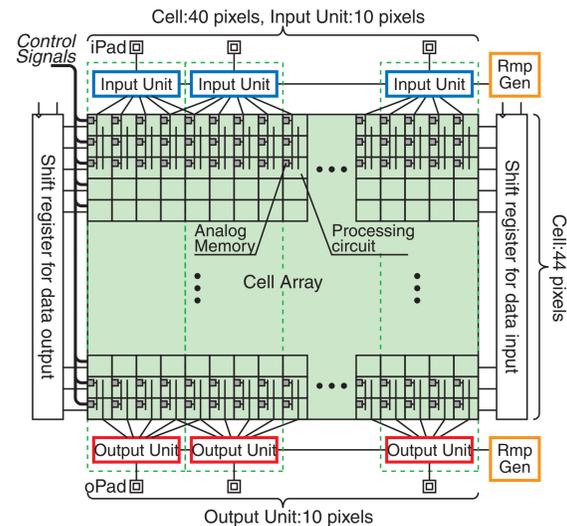
Main characteristics

- **Massively-parallel** image processing
- Line parallel **PWM/PWD** data transfer

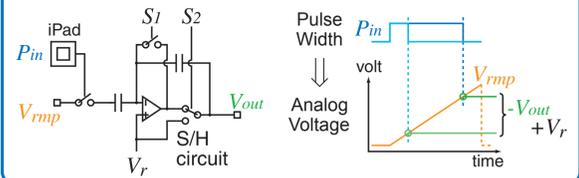
Functions

- Smoothing
- Subtraction
- Gain control

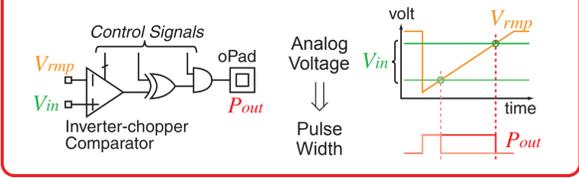
Chip design



PWD (pulse width demodulation) Input Unit

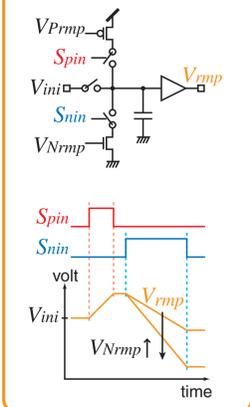


PWM (pulse width modulation) Output Unit

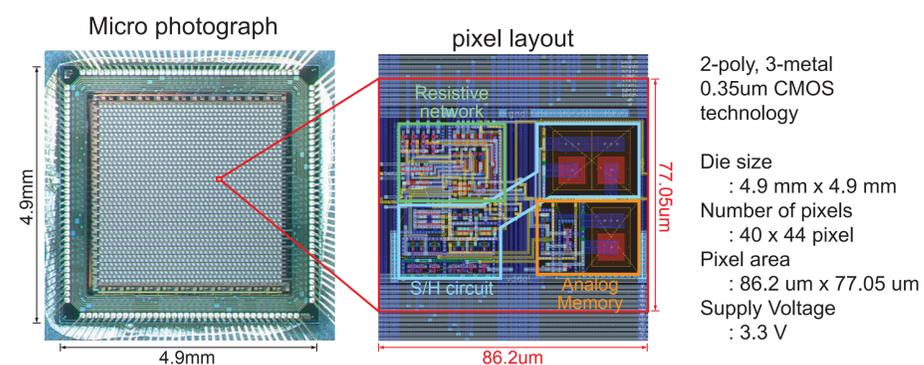


Conversion **gains** of the **PWM & PWD** are controlled by a gradient of the **ramp voltage** signal, which is generated by the **ramp generator**.

Ramp Generator (Rmp Gen)

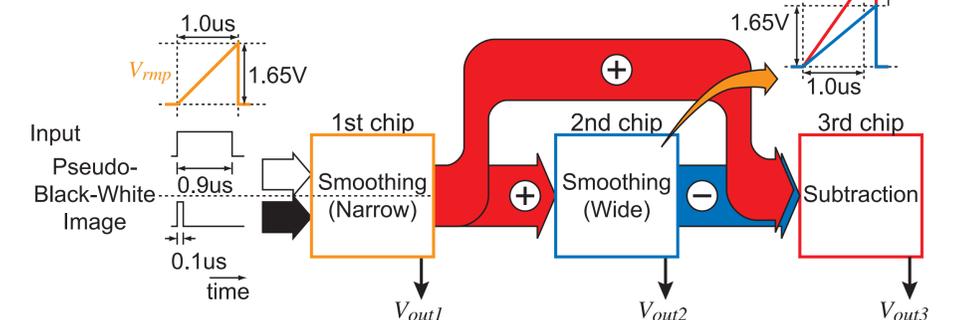


Chip Layout



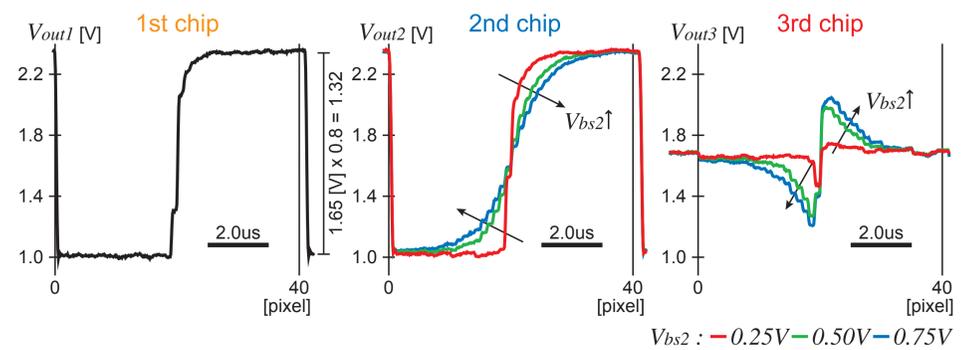
Laplacian-Gaussian Filtering by a Multi-chip system configured by the smoothing chip

System design

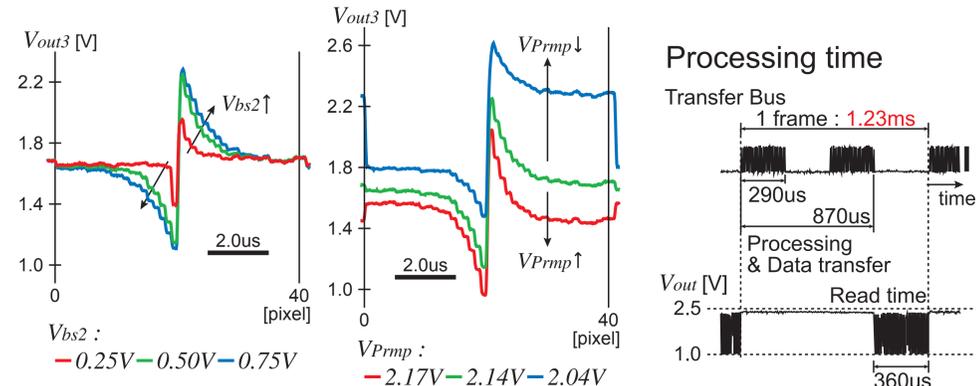


The system configuration was inspired by the **outer retinal circuit** in the vertebrate retina.

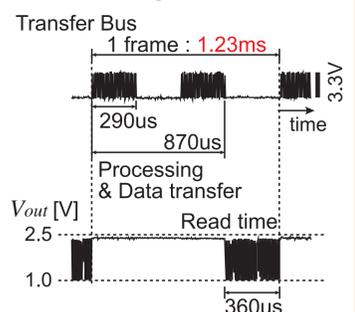
Responses obtained from the Multi-chip system (23th line): $V_{bs1} = 0.25 V$



Responses obtained from the 3rd chip : $V_{bs1} = 0.0 V$



Processing time



Next step

- Development of the **3DCSS** with local wireless interconnection for Image Processing
- Consideration of visual processing algorithms for the vision system

Prototype design of the 3DCSS

