# Design and Measurement of On-Chip CMOS UWB Receiver

Nobuo Sasaki, Pran Kanai Saha and Takamaro Kikkawa
Research Center for Nanodevices and Systems, Hiroshima University
Phone: +81-824-24-6265, Fax: +81-824-22-7185, E-mail: kikkawa@sxsys.hiroshima-u.ac.jp

## 1. Introduction

Although metal wiring has been used for signal transmission of conventional integrated circuit, signal delay due to parasitic RC will become a serious problem for future ULSI. RF wireless technology, which enables re-configurable interconnection, can provide a better solution for this problem [1-3]. A conceptual figure of inter-chip wireless interconnections using integrated dipole antennas is shown in Fig. 1. In this paper, a single-chip CMOS UWB receiver is presented [4,5]. The goal of this research is the development of 1Gbps transceiver using Gaussian monocycle pulse of 5GHz center frequency as a transmitted waveform. This time, the measurements results of UWB receiver are presented, and demodulation of the data is confirmed.

## 2. Circuit Design

Figure 2 shows a block diagram of proposed UWB receiver, and the chip photograph of the UWB receiver, which is based on 0.18μm CMOS technology, is given in Fig. 3. HSPICE simulation shows that the impedance matching circuit has an input impedance of 200Ω~107Ω at 1~10 GHz. Amplification phase has a voltage gain of 15.6dB, where a series connection of two differential amplifiers is used. Although the frequency response of LNA gives rise to the extension of the pulse width, the shape of Gaussian monocycle pulse is not changed so much by LNA (Figs. 4,5). Mixer and integration circuit give a cross correlation between received signals and template signals. Therefore, the demodulation is performed when a proper waveform of the template is given from the internal Gaussian Monocycle Pulse Generator [4]. This time, an input signal itself is used as the template, because the synchronization between the signal and template is a difficult problem. Demodulated data is held by S/H circuit, and is converted to digital signal by comparator. The receiver circuit design is performed using TSMC 0.18μm mixed signal design rule ($V_{dd}$=1.8V).

## 3. Measurement

To avoid the disturbance from a large inductance of bonding wires, a bare chip is directly mounted on the testing board, and SS (GSG) probe is used for the measurement (Fig. 6). Here, each pad size is 50μm x 50μm, and the distance between G and S (S and S) is 150μm. Pulse Pattern Generator (Agilent, 81134A) can generate a rectangular pulse of 80ps rise time. Impulse Forming Network (PSPL, 5214-104) gives the differentiated waveform of the rectangular pulse. A waveform of the generated Gaussian monocycle pulse is shown in Fig. 7, and the relation between the input voltage of the rectangular pulse and output voltage of Gaussian monocycle pulse is given in Fig. 8. Power spectrum of Gaussian monocycle pulse is also given in Fig. 9. The figure shows that the center frequency of the power spectrum is 3.4GHz.

Here OOK (On-Off Keying) modulation method is adopted as shown in Fig. 10. Figure 11 shows a comparator output signal of the receiver without input signal. In this case, 'data=0' phase and 'clear' phase are repeated per internal clock cycle. Figure 12 shows a final output signal when the 1010 Gaussian monocycle pulse is entered into the receiver. The figure shows that the receiver is succeeding to recovering 1010 data from the OOK modulated Gaussian monocycle pulse. It also shows that the minimum voltage of the input Gaussian monocycle pulse necessary to recover data is at least 62mV (from peak to peak). This voltage is comparatively larger than the expected value (20mV). Therefore, the further improvement of the circuit is necessary.

## 4. Summary

A single chip UWB receiver based on TSMC 0.18μm CMOS technology is studied and measurements results are shown. It is confirmed that the receiver could recover digital data formed by OOK modulated Gaussian monocycle pulse, and the minimum voltage of the input Gaussian monocycle pulse necessary to recover data is 62mV (from peak to peak).

## References

[1] A. B. M. H. Rashid, S. Watanabe and T. Kikkawa, IEEE Electron Device Letters, 23 (2003) pp.731-733.

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[4] Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa, Proceedings of ISSSTA 2004, (2003) pp. 962-966

[5] M. Z. Win and R. Scholtz, IEEE Trans. on Communication. 48 (2000) pp679-691.

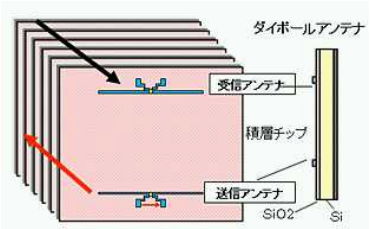


Fig. 1. Conceptual figure of inter-chip wireless interconnections using integrated dipole antennas.

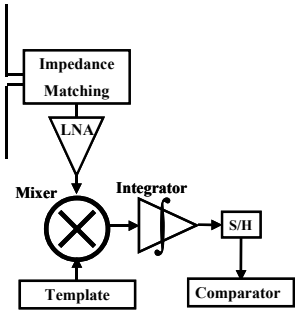


Fig. 2. Block diagram of UWB receiver.

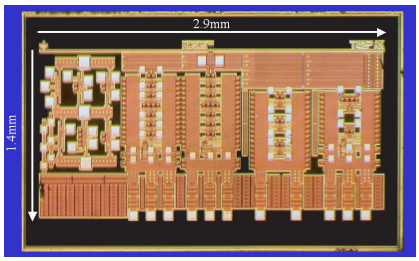


Fig. 3. Chip photograph of the UWB receiver.

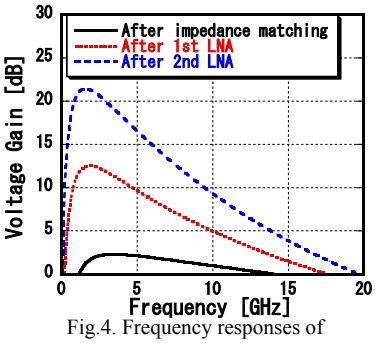


Fig.4. Frequency responses of impedance matching circuit and LNA (HSPICE results).

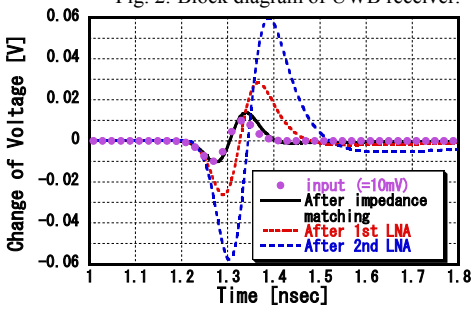


Fig. 5 Output signals of impedance matching circuit and LNA (HSPICE results).

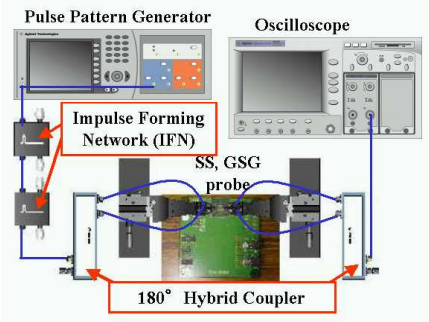


Fig. 6. Setup for the measurement of the UWB receiver.

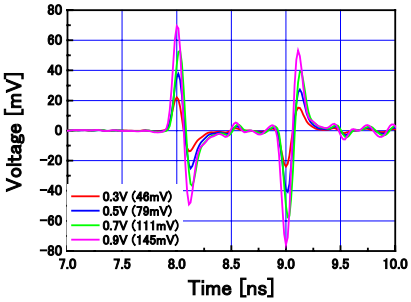


Fig. 7. Waveforms of the generated Gaussian monocycle pulses.

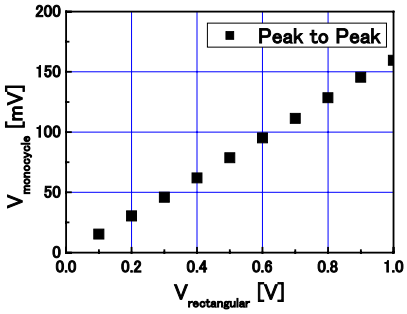


Fig. 8. The relation between the input voltage and output voltage of Gaussian monocycle pulse.

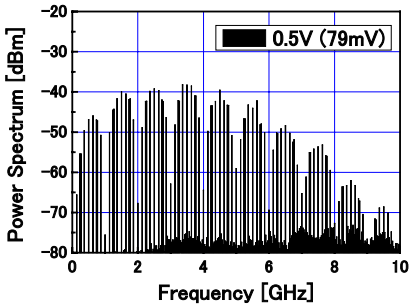


Fig.9. Power spectrum of Gaussian monocycle pulse.

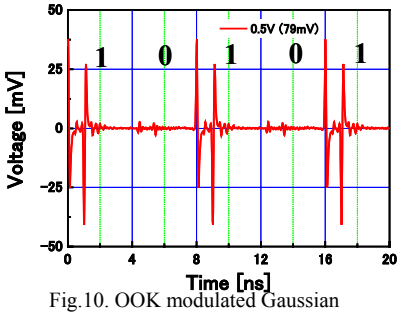


Fig.10. OOK modulated Gaussian monocycle pulses.

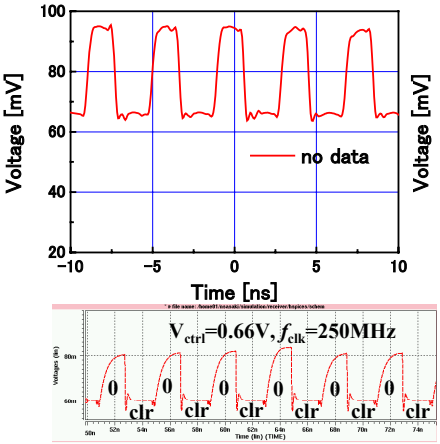


Fig.11. Experimental result and simulation of output signal without input data.

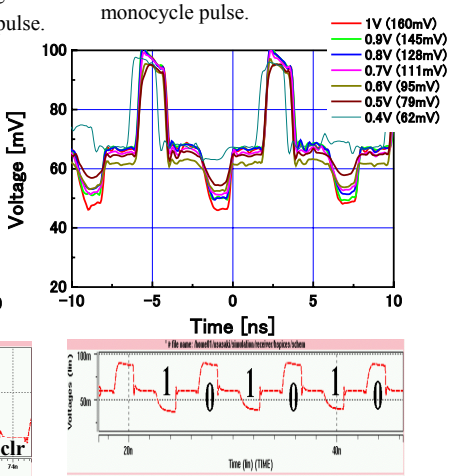


Fig.12. Experimental results and simulation of output signals with input data.

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Research Center for Nanodevices and Systems, Hiroshima University

1-4-2 Kagamiyama, Higashi-Hiroshima, 739-8527 Japan

E-mail: kikkawa@sxsys.hiroshima-u.ac.jp


RCNS Hiroshima University

## Wireless Inter-chip Interconnection

**Signal Delay Due to RC → Serious Problem for Future ULSI**

**Solutions:**

- Copper/low-k Interconnection → Limitation from Materials
- RF Wireless Technology → Re-configurable Interconnection

**Goal:**

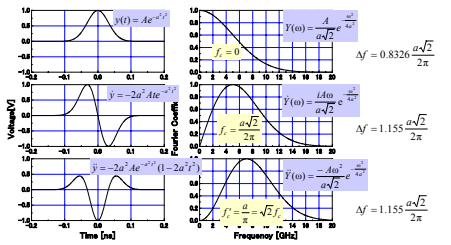
- Development of On-Chip Wireless Interconnections for High Speed Clock/Data Transmission.
- Time Hopping (TH) UWB → Re-configurable Inter-Chip Interconnections

**Target Performance:**

- Single Chip
- 1Gbps Data Rate (Single Channel)
- Target Distance : 1mm ~ 1cm

## Impulse-Based UWB

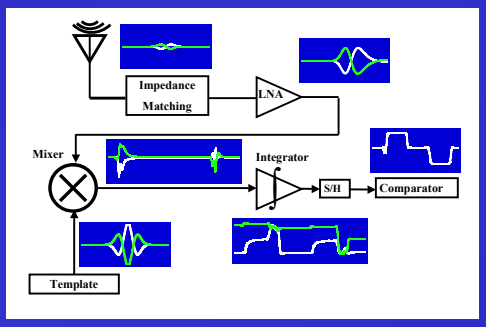
- Transmission Wave → Gaussian Monocycle Pulse
- Ultra-Wide Band Width → High Immunity for Noise
- Base-band Communication → Simple Circuitry




Gaussian, 1st Derivative and 2nd Derivative of Gaussian Pulse and Fourier Transform of Them

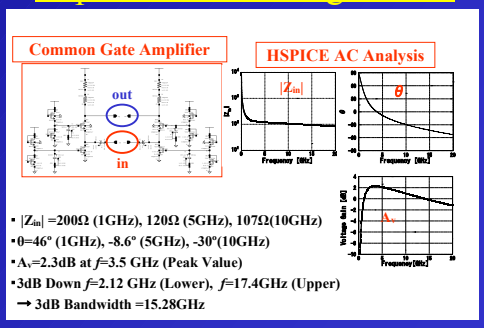
## Single-chip UWB Receiver

- Demodulation : Cross Correlation between Received Signal and Template Signal
- Differential Circuitry



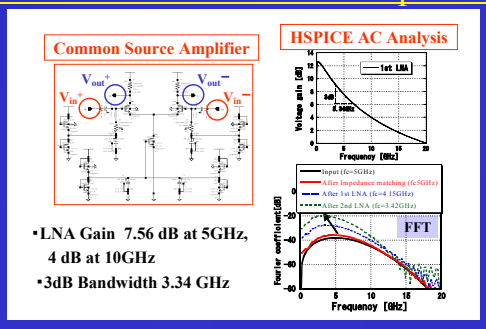

# Circuit Design and Results of HSPICE Simulation

## Impedance Matching Circuit



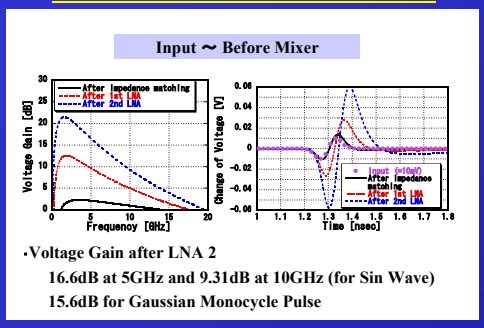

- $|Z_{in}|$ =200Ω (1GHz), 120Ω (5GHz), 107Ω(10GHz)
- θ=46° (1GHz), -8.6° (5GHz), -30°(10GHz)
- $A_v$=2.3dB at $f$=3.5 GHz (Peak Value)
- 3dB Down $f$=2.12 GHz (Lower), $f$=17.4GHz (Upper)
  → 3dB Bandwidth =15.28GHz

## Differential Low Noise Amplifier




- LNA Gain 7.56 dB at 5GHz, 4 dB at 10GHz
- 3dB Bandwidth 3.34 GHz

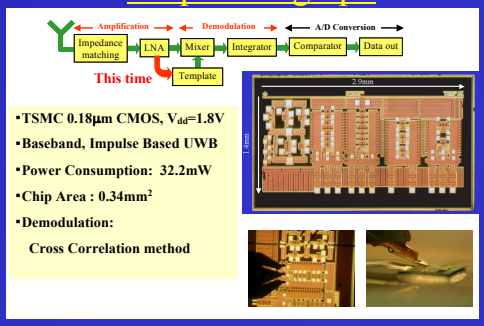
## Total Gain and Waveform




- Voltage Gain after LNA 2
  16.6dB at 5GHz and 9.31dB at 10GHz (for Sin Wave)
  15.6dB for Gaussian Monocycle Pulse

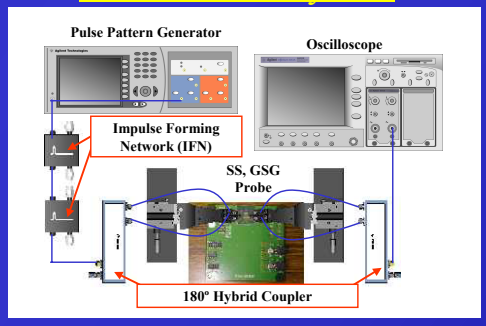
# Measurement Results of UWB Receiver

## Chip Photograph

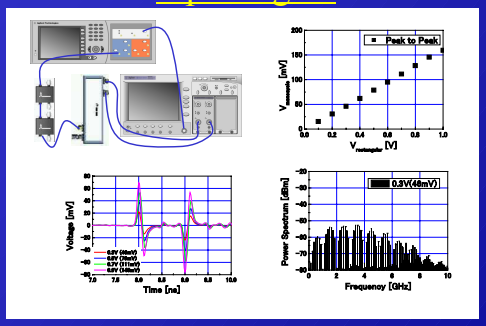



- TSMC 0.18μm CMOS, $V_{dd}$=1.8V
- Baseband, Impulse Based UWB
- Power Consumption: 32.2mW
- Chip Area : 0.34mm²
- Demodulation:
  Cross Correlation method

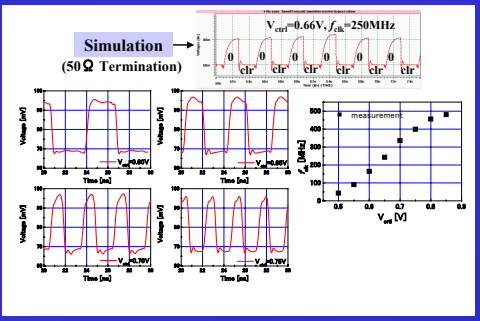
## Measurement System




## Input Signal

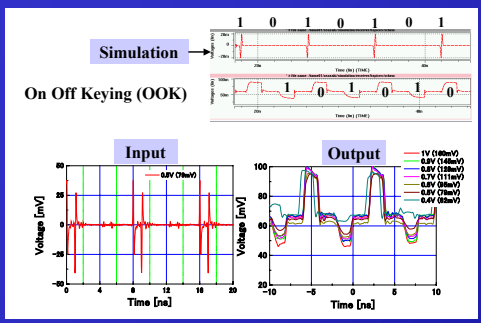



## Output Signal Without Data




- 'Data=0' Phase and 'Clear' Phase are Repeated

## Output Signal With Data




- The UWB Receiver could Recover Digital Data
- Minimum Input Voltage = 62mV

## Summary

- A Single-Chip CMOS UWB Receiver Based on 0.18μm CMOS Technology is Presented
- The UWB Receiver could Recover Digital Data Formed by OOK Modulated Gaussian Monocycle Pulse
- Minimum Voltage of the Input Gaussian Monocycle Pulse Necessary to Recover Data is 62mV (from Peak to Peak)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