Transmission characteristics of Gaussian monocycle pulse for inter-chip wireless interconnection using integrated antenna

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1. Introduction

According to the scaling rule, the reduction in device feature sizes improves the performance of ultra-large-scale-integrated circuits (ULSI) in terms of operation frequency and power consumption. However, conventional metal interconnects will have limitation in global clock frequency of ULSI for high speed operation at 3-4 GHz due to parasitic resistance-capacitance (RC) delay.

In order to overcome this problem, a new concept of wireless interconnection using Si integrated antennas has been proposed to send signals by electromagnetic wave so that both parasitic capacitance and resistance can be eliminated.[1,2] The conceptual diagram of inter-chip wireless interconnection for stacked multi-chip packaging using integrated antenna is shown in Figure 1. Si integrated antennas are fabricated on Si-ULSI so that the global clock signals can be sent from a transmitting antenna of one chip and received by a receiving antenna of another chip by electromagnetic wave propagation. Most of the radiated electromagnetic wave from the antenna on the Si substrate penetrates into the Si due to the difference in dielectric constants between Si (ε_{Si}=12) and air (ε_{Air}=1).[3]

In this study, the feasibility of inter-chip wireless interconnection using Si integrated antennas is investigated.

2. Fabrication and Measurement

P-type (100) Si substrates with 10 Ω·cm resistivity were prepared. A 0.3 μm-thick SiO_2 was formed by pyrogenic oxidation at 1050˚C on the 260 μm-thick Si substrate surface. A 1.0 μm-thick aluminum layer was deposited on the SiO_2 by direct current magnetron sputtering. 10 μm-wide and 4 mm long dipole antennas were fabricated by use of HL-700 electron-beam lithography and subsequent wet etching. Figure 2 shows the schematic diagram of inter-chip measurement sample structure. The Si wafers were stacked vertically and the horizontal distance between antennas (d=3 mm) and antenna length (L=4 mm) were fixed. The Si substrates thickness (h) was varied from 0.26 mm to 2.86 mm.

A wafer level measurement set-up for S-parameter measurements in frequency domain is shown in Figure 3. It consists of HP8510C Vector Network Analyzer, 180° Hybrid Couplers (6-26.5 GHz), probe station and Signal-Signal (SS) probes. Wafers were measured on a wood (2.6 mm-thick) on the metal chuck of the probe station. The relative dielectric constant of the wood was 2.15 at 1 GHz.[3] From measured S-parameters: reflection coefficient (S_{11}) and transmission coefficient (S_{21}), [4] antenna transmission gain (G_a) through Si substrates can be calculated.

Figure 4 shows the measurement set-up for inter-chip antenna transmission characteristics in time domain. It is composed of Agilent N4902A Serial BERT, impulse forming networks and Agilent 86100B sampling oscilloscope.

3. Results and Discussion

Effects of the inserted Si substrates thickness on S_{11} and S_{21} of the dipole antenna (L=4 mm) in the stacked structure were shown in Figures 5, 6 and 7. Neither S_{11} nor S_{21} were affected by the inserted Si substrates thickness having ρ=2.29k Ω·cm very much as shown in Figs. 5 and 6. On the other hand, S_{21} decreased with increasing the inserted Si substrates thickness having ρ=10 Ω·cm as shown in Fig. 7. This is due to the loss of electromagnetic wave in Si substrates. Figure 8 shows G_a at 20 GHz versus the Si substrates thickness for different Si substrates resistivities: ρ=10 Ω·cm and ρ=2.29k Ω·cm. The attenuation rates were -0.4 dB/mm and -4.9 dB/mm per unit vertical distance for ρ=2.29k Ω·cm and ρ=10 Ω·cm, respectively.

Figure 9 shows the transmitting Gaussian monocycle pulse, which was formed by inserting two cascade impulse forming networks at the output of the Serial BERT. Fast Fourier transform of the transmitting signal is shown in Figure 10. The center frequency was approximately 15 GHz and the bandwidth was 20 GHz.

The transmitting antenna with antenna length of 4 mm was radiated Gaussian monocycle pulses and the received signal at the receiver dipole antenna which was located at the horizontal distance of 3 mm and vertical distance of 2.86 mm with 2.29k Ω·cm resistivity Si substrates is shown in Figures 11(a) and 11(b). Moreover, Figure 12 shows received signal at the receiver in the case of inserted Si substrate resistivity was 10 Ω·cm and thickness was 2.86 mm. Compared Fig. 11 to Fig. 12, peak to peak voltages were 1.9 mV and 0.7 mV for Si substrates resistivities of 2.29k Ω·cm and 10 Ω·cm, respectively.

4. Conclusion

We have demonstrated signal transmission through the inter-chip wireless interconnection in the stacked structure by using Si integrated antenna.

Acknowledgements

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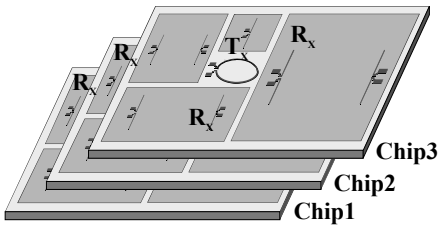
References

[1] Kihong Kim, et al, IEDM Tech. Dig., pp.485-488, December 2000.
[2] A.B.M. H. Rashid, et al, IEEE Electron Device Letters, Vol. 23, No.12, December 2002, pp.731-733.
[3] S. Watanabe, et al, Extended Abstract of SSDM 2003
[4] S. Watanabe, et al, Advanced Metallization Conference 2002 Asian Session, pp. 94-95



T_x : Transmitting antenna, R_x : Receiving antenna

Fig.1. Concept of inter-chip wireless interconnect using dipole antennas integrated in multiple Si ULSI chips.

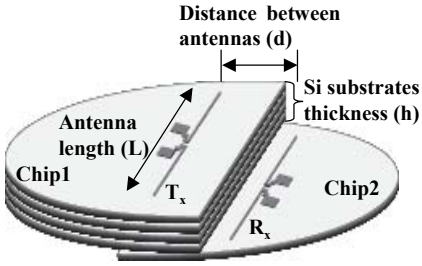


Fig. 2. Schematic diagram of inter-chip measurement sample structure.

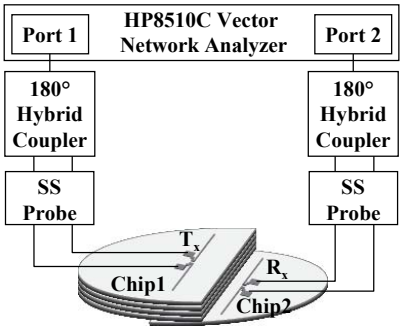
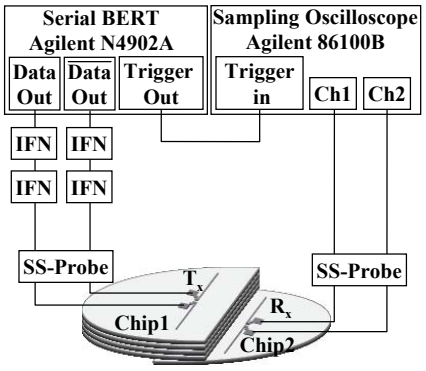


Fig. 3. Measurement setup for inter-chip antenna transmission characteristics in frequency domain.



IFN : Impulse Forming Network

Fig. 4. Measurement setup for inter-chip signal transmission characteristics in time domain.

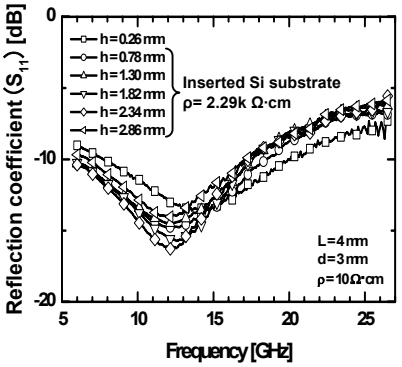


Fig.5. Effect of the inserted Si substrates thickness with ρ = 2.29k Ω·cm on the reflection coefficient (S_{11}) versus frequency. (Antenna L=4mm, d=3mm)

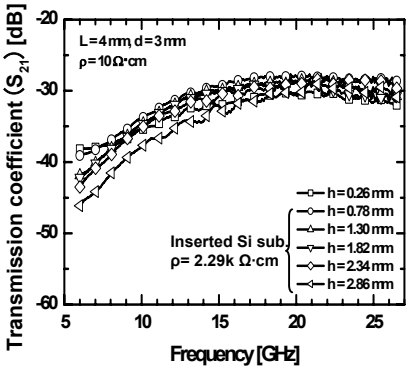


Fig.6. Effect of the inserted Si substrates thickness with ρ = 2.29k Ω·cm on the transmission coefficient (S_{21}) versus frequency. (Antenna L=4mm, d=3mm)

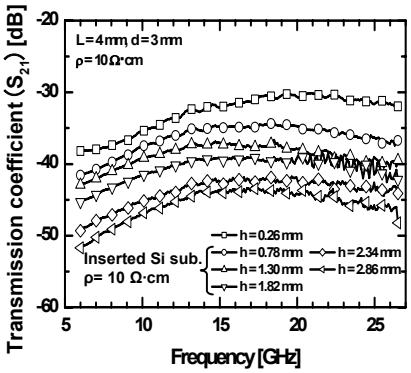


Fig.7. Effect of the inserted Si substrates thickness with ρ = 10 Ω·cm on the transmission coefficient (S_{21}) versus frequency. (Antenna L=4mm, d=3mm).

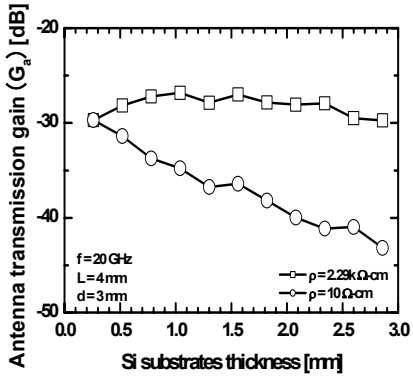


Fig.8. Antenna transmission gain (G_a) versus the inserted Si substrates thickness. (Antenna L=4mm, d=3mm)

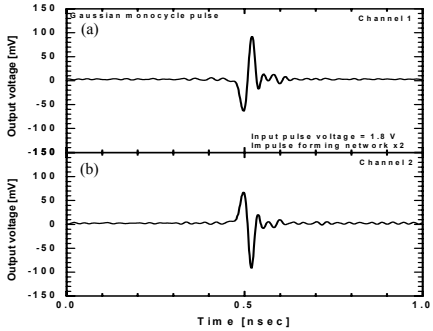


Fig.9. Transmitting Gaussian monocycle pulse for a transmitter dipole antenna. (a) Channel 1. (b) Channel 2.

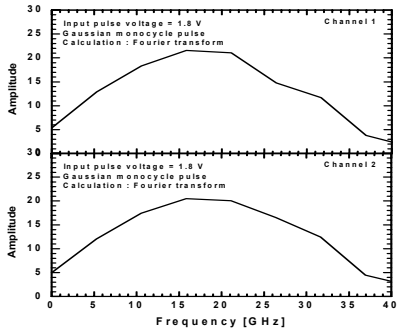


Fig.10. Fast Fourier transform of the transmitting Gaussian monocycle pulse signal.

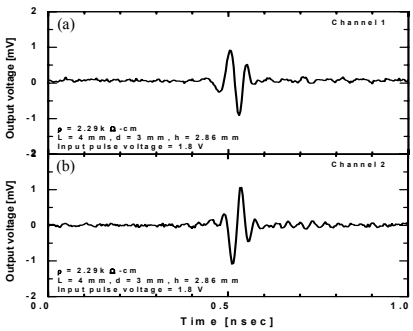


Fig.11. Received signal at the receiver dipole antenna. (a) Channel 1. (b) Channel 2. (Antenna L=4mm, d=3mm, h=2.86mm (ρ=2.29k Ω·cm))

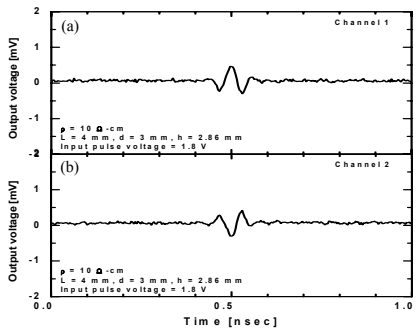


Fig.12. Received signal at the receiver dipole antenna. (a) Channel 1. (b) Channel 2. (Antenna L=4mm, d=3mm, h=2.86mm (ρ=10 Ω·cm))

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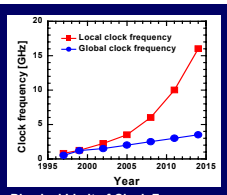
Motivation

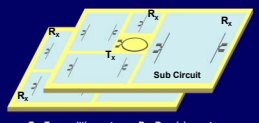
According to the scaling rule of LSI, conventional metal interconnects will limit high-speed operation of ULSI due to RC delay.

ULSI global clock frequency will be limited below 4 GHz due to RC time constants of interconnects.

Wireless interconnection could be a breakthrough technology for higher-speed operation of ULSI using Si integrated antennas.



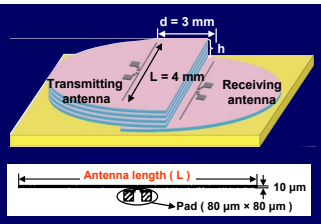
Physical Limit of Clock Frequency



T_x :Transmitting antenna, R_x :Receiving antenna

Concept of Wireless Interconnects on ULSI - Chip

Inter-chip Si Dipole Antenna Structure and Fabrication Process



: SiO_2 = 0.3 μm
: Si = 260 μm
: Wood = 2.6 ± 0.1 mm

L : Antenna length
d : Horizontal distance between antennas
h : Vertical distance between antennas
ρ : Si substrate resistivity

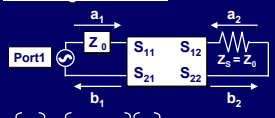
■ Inter-chip sample structure

■ Fabrication Process

1. Oxidation	Thermal oxide (thickness : 0.3 μm)
2. Aluminum sputtering	DC magnetron sputtering (thickness : 1.0 μm)
3. Lithography	Electron beam lithography (HL700)
4. Patterning	Wet etching
5. Photoresist stripping	Remover

Measurement Set-up (Frequency Domain)

Scattering – Parameter



$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

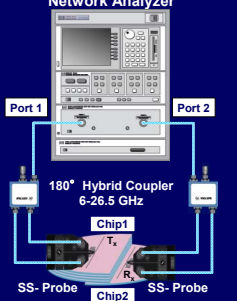
a_i - Incident wave
b_i - Reflected wave

$$S_{ii} = \left.\frac{b_i}{a_i}\right|_{a_j=0} \qquad S_{ij} = \left.\frac{b_i}{a_j}\right|_{a_i=0}$$

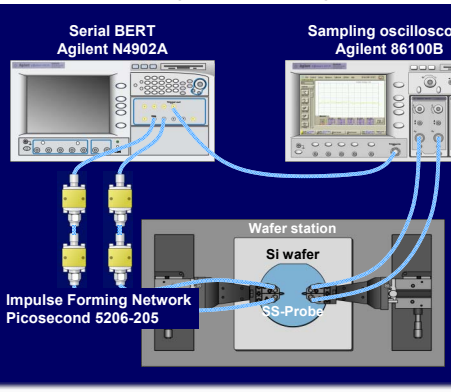
Antenna Transmission Gain (G_a)

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

HP8510C Vector Network Analyzer

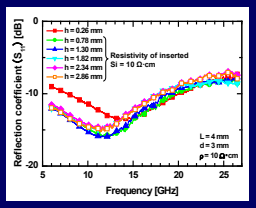


Measurement Set-up (Time Domain)

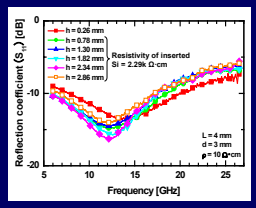


Effect of Si Substrates Thickness on Return Loss

Resistivity of inserted Si = 10 Ω·cm



Resistivity of inserted Si = 2.29k Ω·cm

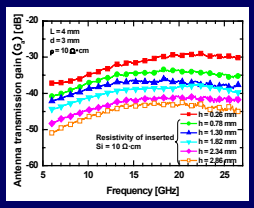


■ The thickness of the Si substrates was increased from 0.26 mm to 2.86 mm by increasing the number of inserted Si substrates.

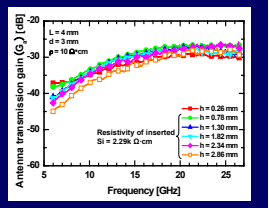
■ Return loss was not affected very much by either thickness or resistivity of Si substrates.

Effect of Si Substrates Thickness on Antenna Transmission Gain

Resistivity of inserted Si = 10 Ω·cm



Resistivity of inserted Si = 2.29k Ω·cm

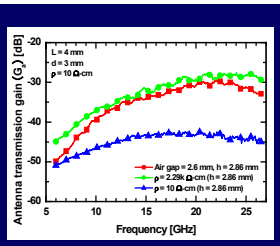


■ Antenna gain decreases with increasing the vertical distance between antennas, or increasing Si substrate thickness.

■ Antenna gain increases with increasing Si substrate resistivity.

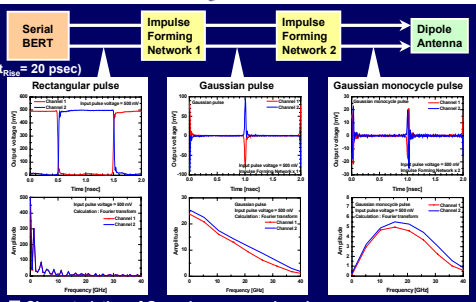
■ Antenna gain of -27 dB was obtained for the inserted Si thickness of 2.86 mm between transmitting and receiving antennas.

Effect of Inserted Materials between Antennas on Antenna Gain



■ Maximum antenna transmission gain was obtained by inserting high resistivity Si substrates between antennas.

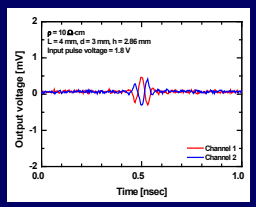
Characteristics of Gaussian Monocycle Pulse



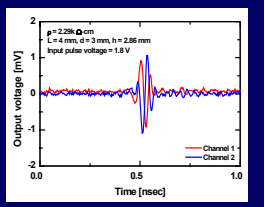
■ Characteristics of Gaussian monocycle pulse
Pulse width = 70 psec
Center frequency = 15 GHz
Bandwidth = 20 GHz

Effect of Si Substrate Resistivity on Gaussian Monocycle Pulse Amplitude

Resistivity of inserted Si = 10 Ω·cm



Resistivity of inserted Si = 2.29k Ω·cm

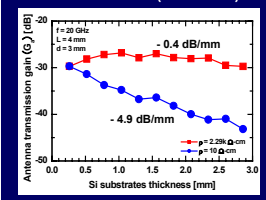


■ Gaussian monocycle pulse amplitude increased with increasing Si substrate resistivity.

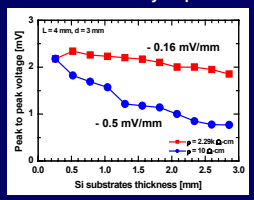
■ Peak to peak voltages were 1.9 mV and 0.7 mV for Si substrates resistivities of 2.29k Ω·cm and 10 Ω·cm, respectively.

Effects of Si Substrate Thickness on Transmission Signal

Sinusoidal wave (f = 20 GHz)



Gaussian monocycle pulse



■ Antenna transmission gain of -30 dB was obtained for vertical distance of 2.86 mm with 2.29k Ω·cm Si substrates.

■ Attenuation rates of antenna gain per unit vertical distance in the Si substrates were improved by increasing Si substrates resistivity.

■ Antenna gain and peak to peak voltage were decreased with increasing Si substrate thickness.

Summary

1. Performances of integrated antennas on Si substrates were investigated for inter-chip signal transmission in Si ULSI.
2. Antenna transmission gain between Si chips was improved by using high resistivity Si substrate.
3. Inter-chip antenna transmission gain of -27 dB was obtained for vertical distance of 2.86 mm with 2.29k Ω·cm Si substrates and horizontal distance of 3 mm by use of 4 mm long dipole antenna.

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