Study in 3-D MOS Transistor Formation

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1. Introduction

It is becoming difficult to control the short channel effect and to integrate conventional bulk devices up to date. To overcome this problem, three-dimensional (3-D) device structures have been proposed [1]. A FinFET of which gate electrode is 10 nm in length was already reported [2]. From now on, not only the scaling of these devices, but also the progress of new structure and/or new operation of 3-D devices becomes important. In this study, a new vertical structure transistor is proposed.

2. Proposed device and its fabrication processes

The structure of proposed device is shown in Fig. 1. In this structure, three transistors that are formed on a SOI beam can operate independently. This can apply to parallel part of a logic circuit, for example a part of NAND gate. Since transistors are integrated vertically, this structure has an advantage from the viewpoint of area efficiency.

In the fabrication of this device, it is important to form three gate electrodes using self-aligned process to realize normal operation of the device. The fabrication process is devised in consideration of this point. The process sequence is shown in Fig. 2. To realize the proposed device, isolation of gate electrode, and leveling of poly-Si are key techniques.

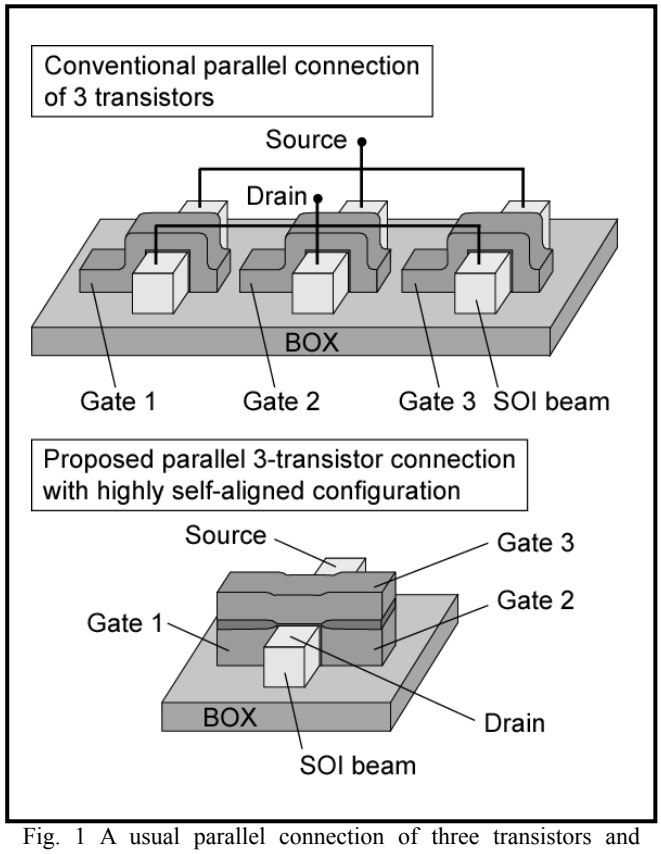


Fig. 1 A usual parallel connection of three transistors and the structure of the proposed device.

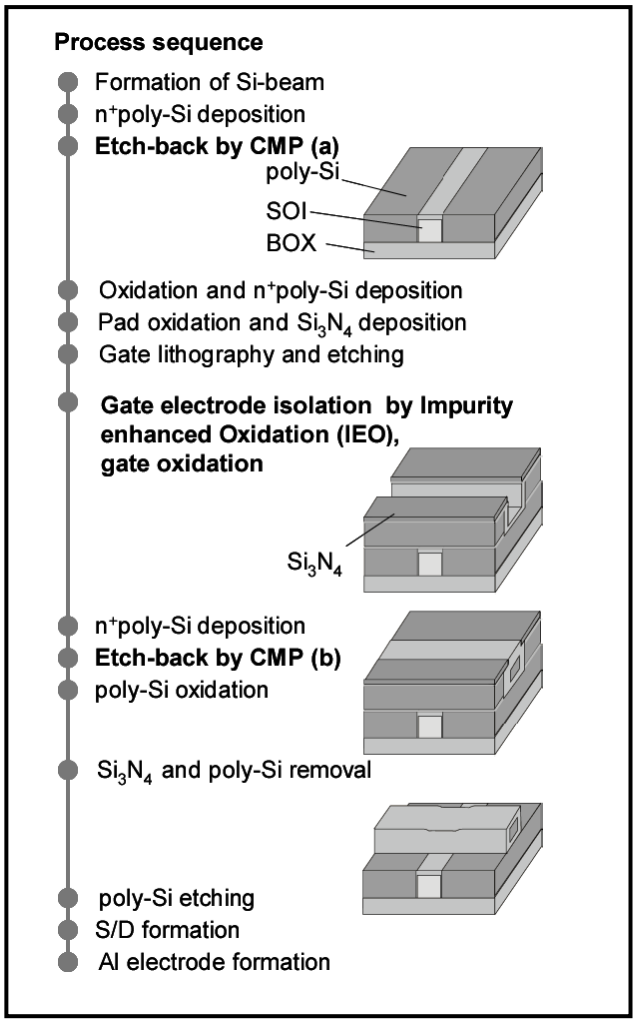


Fig. 2 The process sequence of the proposed device.

3. Experimental results and Discussion

3.1 Gate electrode isolation by impurity enhanced oxidation (IEO[3])

Since the isolation layer of gate electrodes and gate oxide film of the third gate are formed simultaneously, enlargement of the ratio of oxide thickness of Si substrate and poly-Si is needed. From this reason, the impurity enhanced oxidation (IEO[3]) is introduced in this process. Oxide thickness of phosphorous doped n^+poly-Si and boron doped Si substrate at 850 ^oC and 1000 ^oC are shown in Fig. 3. Although the ratio of oxide thickness of n^+poly-Si and p(100) Si substrate exceeds almost 4.4 times at 850 ^oC, oxide film thinning at edge of poly-Si gate occurs (Fig. 4). This phenomenon is suppressed by the relaxation of the stress by viscous flow at high-temperature oxidation (Fig. 5). Since the ratio of oxide thickness at 1000 ^oC is almost 2.7 times, oxide film

on p(100) Si substrate becomes thick as compared with oxide grown at 850 °C. To control thickness and configuration of isolation layer and gate oxide, suitable oxidation condition has to be chosen. For example, it is thought that combination of low-temperature oxidation and high-temperature oxidation with diluted oxygen is useful.

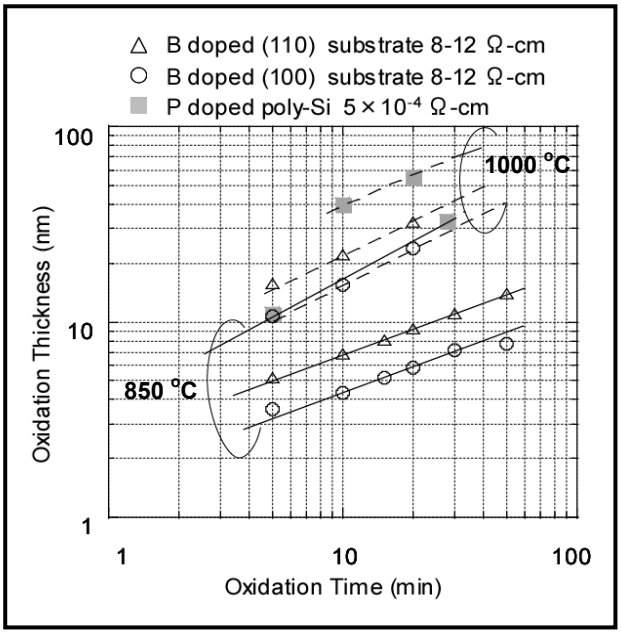


Fig. 3 Impurity enhanced oxidation at 850 °C and 1000 °C (O_2=2 slm).

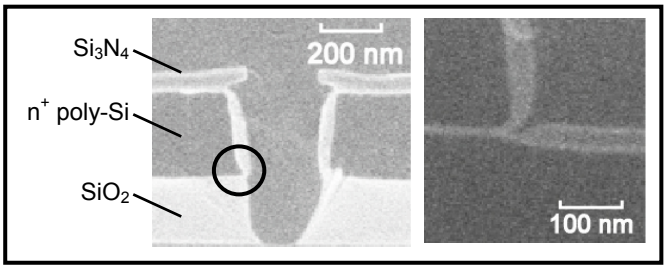


Fig. 4 SEM images showing SiO_2 film thinning formed by dry oxidation at 850 °C.

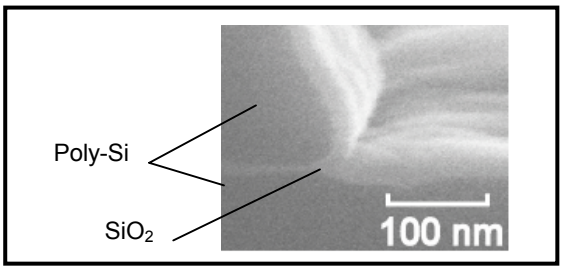
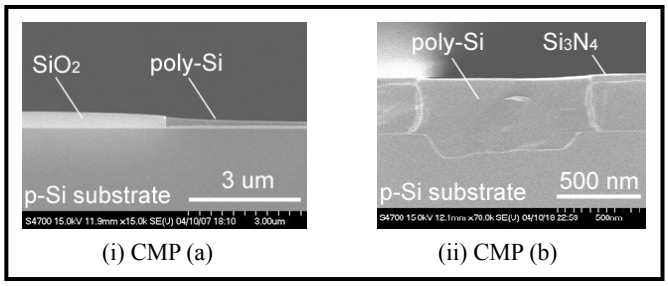


Fig. 5 An SEM image showing conformability of SiO_2 film formed by dry oxidation at 1000 °C.

3.2 Leveling process

Leveling of poly-Si is needed twice in the process (CMP (a) and (b) in Fig. 2). One is required for separation of side gate electrodes and the other is to form the third one. Cross-sectional SEM images of samples after CMP (a) and (b) are shown in Fig. 6. In this experiment, dishing and erosion are observed in the former case. It may be because the area of SOI-beams is narrow in the CMP (a). To prevent these phenomena, introducing of dummy patterns is needed (Fig. 7). In the latter case, a good configuration was obtained.



(i) CMP (a) (ii) CMP (b)

Fig. 6 Cross-sectional SEM images of obtained poly-Si stripes by CMP etch-back.

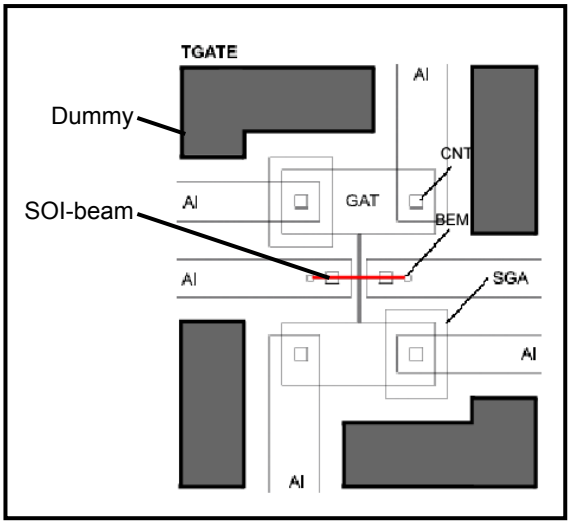


Fig. 7 Layout patterns of proposed device with dummy patterns.

4. Summary

A novel 3-D transistor structure and its fabrication process are proposed. With respect to the IEO which applies to the formation of the gate oxide film of the third gate and the isolation layer of gate electrodes it becomes clear that suitable oxidation condition has to be chosen to avoid the oxide film thinning at edge of patterns. In leveling processes, to cope with the problem of dishing and erosion in CMP, introducing of dummy patterns is planned to realize the desirable device structure.

5. References

[1] Y-K. Cho, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Andersen, T-J. King, J. Bokor, and C. Hu, *IEDM Tech. Dig.,* pp. 421-424, 2001.

[2] Bin Yu, Leland Chang et al, *IEDM Tech. Dig.,* pp. 251-254, 2002.

[3] H. Sunami, *J. Electrochem. Soc.,* **125,** pp. 892-897, 1978.

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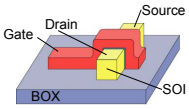
1. Introduction

Difficulty of suppression of short channel effect and integration of conventional bulk devices

Three-dimensional (3-D) device structures on SOI, such as FinFET have been proposed in this circumstances [1,2].



There is another possibility in 3-D device application.

Objectives : Development of transistor structure and its formation process for another application of 3-D transistor

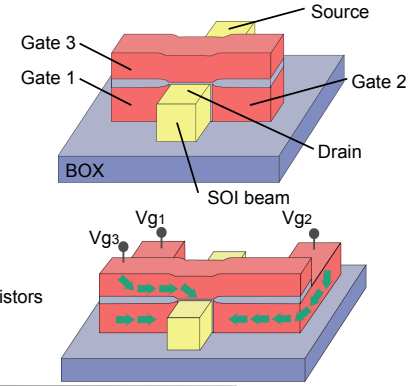
In this study, a new vertical structure transistor and its formation process are proposed.

2. Proposed device and its fabrication processes

Device structure

Independent three gate electrodes on SOI-beam

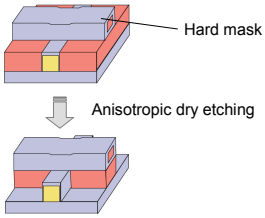
Gate voltage can be applied three channels independently



- Parallel connection of three transistors
  - ⇨ Area efficiency
- Control of device characteristic of side transistors by Vg_3

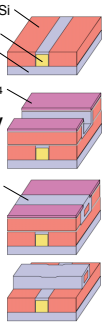
Fabrication Process

Self aligned formation of three gate electrodes



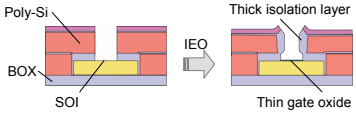
Process sequence

- Formation of SOI-beam
- Poly-Si deposition
- **Etch-back by CMP (a)**
- Poly-Si and Si_3N_4 deposition
- Gate lithography and etching
- **Gate electrode isolation by impurity enhanced oxidation (IEO [3])**
- Poly-Si deposition
- **Etch-back by CMP (b)**
- poly-Si oxidation
- Si_3N_4 and poly-Si removal
- Side poly-Si etching
- S/D formation
- Al electrode formation



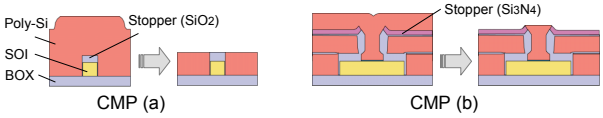
Key techniques

Gate electrode isolation by IEO



Enhancement of the ratio of oxide thickness of SOI and poly-Si is needed.

Leveling of poly-Si by CMP etch-back



3. Experimental result and Discussion

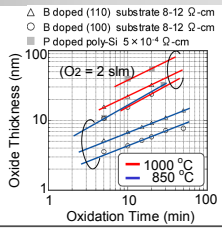
3.1 Gate electrode isolation by IEO

Ratio of oxide thickness

p(100) substrate : P doped poly-Si

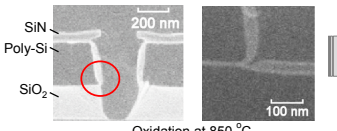
850 °C	1 : 4.4
1000 °C	1 : 2.7

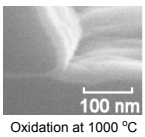
the ratio is large enough at 850 °C.



Oxide film thinning at edge of poly-Si

Film thinning was suppressed at 1000 °C



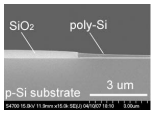


Optimization of oxidation condition is needed.

3.2 Leveling process

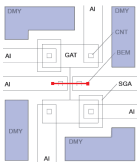
CMP is needed twice in this process

- **CMP (a) : separation of side gate electrode**



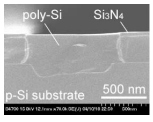
Dishing and errosion are observed.

Area of SOI-beams is narrow in this process ⇨ Introducing of dummy is needed



Layout patterns with dummy

- **CMP (b) : formation of third gate electrodes**



Good configuration was obtained.

4. Summary

A new 3-D structure transistor with novel fabrication process is proposed.

- **Gate electrode isolation by IEO**

850 °C	1000 °C
● Ratio of oxide thickness is large.	● Ratio of oxide thickness is small.
● Oxide film thinning at edge of poly-Si	● Good configuration

To control thickness and configuration, suitable oxidation condition has to be chosen.

- **Leveling process**

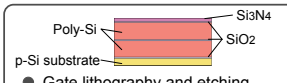
  Dishing and errosion are observed in CMP (a) ⇨ Introducing of dummy is needed

- **Formation of two-layer poly-Si wiring**

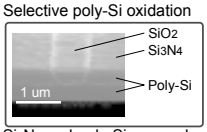
  Fabricated by combination of **gate electrode isolation by IEO** and **CMP (b)**

⇨ Two-layer poly-Si wiring was successfully fabricated

3.3 Formation of two-layer poly-Si wiring

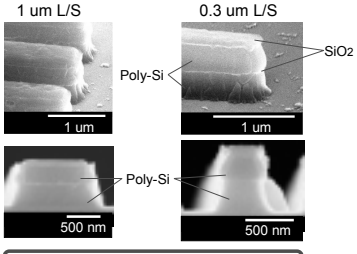


- Gate lithography and etching
- **Gate electrode isolation by IEO**
- Poly-Si deposition
- **Etch-back by CMP (b)**
- Selective poly-Si oxidation



- Si_3N_4 and poly-Si removal
- Side poly-Si etching

● Obtained poly-Si wiring



Two-layer poly-Si wiring was successfully fabricated

References :
[1] Y-K. Cho, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Andersen, T-J. King, J. Bokor, and C. Hu, *IEDM Tech. Dig.*, pp. 421-424,2001.
[2] Bin Yu, Leland Chang et al, *IEDM Tech. Dig.*, pp. 251-254, 2002.
[3] H. Sunami, *J. Electrochem. Soc.*, **125,** pp. 892-897, 1978.