Characterization of Charged States of Silicon-Based Quantum Dots and Its Application to Floating Gate MOS Memories

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1. Research Background

Serious limitations in down-sizing conventional MOS devices motivate us to develop novel functional devices with well-defined Si nanostructures. Especially, implementation of silicon-quantum-dots (Si-QDs) as a floating gate in MOSFETs has received increasing attention because of its potential advantage for multivalued memories with a reliable operation even at room temperature and above [1,2]. To realize discrete charged states in the Si-QDs floating gate with respect to the gate voltage, the size uniformity of Si-QDs with an areal density comparable to the channel electron density is a crucial factor because both charging energy and quantization energy in each of Si-QDs is strongly size dependent. In that regard, the self-assembling process is thought to be adequate for controlling the formation of high density Si-QDs on SiO_2. So far, we have demonstrated spontaneous formation of Si-QDs on thermally-grown SiO_2 with a fairly uniform size distribution and a high areal density ($>10^{11}cm^{-2}$) by controlling the early stage of low-pressure chemical-vapor deposition (LPCVD) from SiH_4 [3], and demonstrated unique multiple-step electron charging in the Si-QDs floating gate [4, 5].

2. Research Results

2.1 Fabrication of Multiple Stacked Si-QDs Embedded in Gate Oxide

In preparing Si dots with a areal density as high as $10^{11}cm^{-2}$ on thermally-grown SiO_2, the surface termination with OH bonds was made previously by dipping in a dilute HF solution just before the Si dot formation [3]. To fabricate multiply-stacked structures consisting of Si-QDs and ultrathin SiO_2, we have combined the Si dot formation by SiH_4-LPCVD with the surface modification by remote plasma treatments in which surface oxidation and subsequent OH termination are preformed by exposing to remote O_2 plasma and remote Ar/H_2 plasma, respectively [6]. From cross-sectional TEM observations of the samples so prepared, we have demonstrated that this method is very feasible to fabricate densely stacked Si-QDs embedded in SiO_2. Also, we have confirmed that plasma-induced damages and/or contaminations are negligible in this fabrication process from the charging and discharging characteristics of Si-QDs stacked structure as a floating gate in MOS capacitors.

2.2 Fabrication of Si-QDs with a Ge Core and Their Electrical Characterization

After Si dot formation on ultrathin SiO_2, we controlled the selective growth conditions in LPCVD using alternately 5% GeH_4 and pure SiH_4. As a result, the spherical dots with an ellipsoidal Ge core were formed on the SiO_2 layer, being in contrast to the hemispherical pure Si dots pregrown on the SiO_2 layer [7]. The distinct change in the dot shape is attributable to the structural relaxation at highly strained interface between Si and Ge. From the change in the surface potential of Si dots with a Ge core caused by electron injection or emission as measured with an AMF/Kelvin probe technique [8], we found that electrons and holes are retained in the Si clad and the Ge core, respectively as predicted in the type II band discontinuity between the Si clad and the Ge core [9]. In addition, we have evaluated the electron transport through Si-QDs with a Ge core by conductive AFM measurements and demonstrated the presence of the Ge core is clearly detected from the current image contrast being dependent on the positive bias applied to the AFM tip. The enhanced current thought the Ge core is thought to be related to the accumulation of holes into the Ge core caused by the extraction of valence electrons from both the Si clad and the Ge core.

2.3 Impact of Cold light Irradiation on Characteristics of Al-gate MOS Capacitors with Si-QDs as a Floating Gate

Electron Charging and discharging characteristics of a Si-QDs floating gate has been studied so far in dark at room temperature from unique hysteresis characteristics observed in high frequency capacitance-voltage (C-V) and displacement current-voltage (I-V) curves of Al-gate MOS capacitors with a Si-QDs floating gate on p-type and n-type Si(100) [4]. From the facts that the hysteresis characteristics are observed with a symmetrical pattern reflecting the Fermi energy of the substrate and both the capacitance and displacement current peaks appear around the flat-band condition, the contribution of traps to the measured hysterisis characteristics can be ruled out.

When the high frequency C-V measurements were carried out under white light irradiation in the wavelength region of 400-800nm through a fiber-optics equipped with an infrared filter from a 100W halogen lamp, a distinct capacitance peak due to the charge injection to the Si-QDs floating gate in the inversion condition becomes observable as shown in Fig. 1 [10]. This is because photo-generated carriers in the vicinity of the area masked with the Al gate flow into beneath the gate oxide and respond to the gate voltage modulation even at a high frequency. For nMOS on p-Si(100) seen in Fig.1, the observed capacitance peak in the inversion condition indicates that the injection of electrons to the electrically-neutral Si-QDs occurs in unison at a certain gate voltage as in the case of electron emission from the charged Si-QDs near the flat-band condition. Under a depletion condition at -0.3V, the transition from the C-V curve of dot neutral state to that of the charged state occurs due to the electron injection and correspondingly the displacement current peak due to the electron injection

appears at the same voltage. Obviously, the voltage required for electron injection to the neutral state is markedly reduced under light illumination but in contrast, the voltages for electron emission from the charged state and neutral state and for the neutralization of the dots almost remain unchanged. In addition, the displacement current in the strong inversion condition is hardly observed under light illumination because the electron concentration of the Si surface can be changed within the delay time by the action of virtual source. In the depletion condition, because of little carrier flow from the peripheral region, the displacement current due to electron emission from the charged dots becomes observable.

2.4 Influence of light Irradiation of Poly-Si Gate nMOSFETs with a Si-QDs Floating Gate

Based on the characteristics of MOS capacitors with the Si-QDs floating gate, we have designed and fabricated n-MOSFETs with a doubly-stacked Si-QDs floating gate [5]. The multi-step electron charging to the Si-QDs floating gate caused by the Coulomb blockade effect has been confirmed from distinct bumps in drain current-gate voltage characteristics observed in ramping up the gate voltage after complete discharging and also from the temporal change in the drain current (I_d-t) at constant gate biases. In addition, in the I_d-t characteristics there is a metastable state with a fairly long incubation period to the next charging and injected electrons are redistributed during the metastable state to further electron charging. From the temperature dependence of Id-t characteristics, we found that the electron charging in dark proceeds with an activation energy corresponding to the 1st and 2nd energy states in neighboring dots. As shown in Fig. 2 [11], I_d-t characteristics measured under visible light illumination show that electron injection to the Si-QDs is markedly pronounced in compared with the results in dark and the period of the metastable charged state is reduced significantly. An increase in the current level under visible light irradiation is due to the photogenerated electron contribution. Since the current level in dark after light-induced charging coincides with the current level of the stable state obtained in dark, no excess electrons over a thermally equivalent level in dark is not injected to the dots under this light irradiation. Considering the facts that the time to the final stable state becomes shorter with higher photon flux and/or higher photon energy but the transition from the metastable charged state to the finally stable charged state is almost unchanged, the light irradiation mainly accelerates the temporal change in the charging during the metastable charged states to trigger the transition to the final stable state.

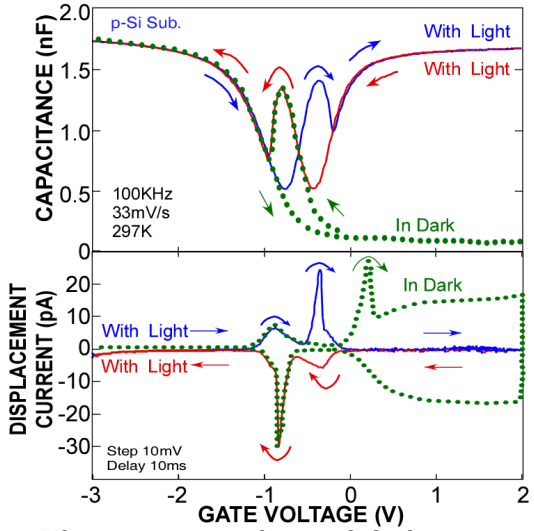

Fig. 1 100kHz capacitance-voltage and displacement current-voltage characteristics of an Al-gate MOS capacitor with a Si-QDs floating gate measured at room temperature in dark and under illumination of cold light in the wavelength region of 400-800nm.

3. Future Research Issues in the COE Program

To develop photosensitive functional devices, the gate stack structures consisting of a semitransparent metal gate, a gate dielectric with a high dielectric constant (high-k), a QDs-floating gate and the bottom tunneling oxide will be investigated, especially from the viewpoint of operations critical to the input of a few photons.

Acknowledgements

The author wishes to thank Dr. H. Murakami and Assoc. Prof. S. Higashi for their assistance and M. Ikeda, T. Shibaguchi, T. Nagai and K. Makihara for their valuable contribution. This work was supported in part by Grant-in Aids for the 21st Century COE Program "Nanoelectronics for Tera-bit Information Processing" and for scientific research of priority area (A) from the Ministry of Education, Science, Sports and Culture of Japan.

References

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2. A. Kohno, et al., Jpn. J. Appl. Phys. 40 (2001) L721.
3. S. Miyazaki, et al., Thin Solid Films 369 (2000) 55.
4. T. Shibaguchi, et al., *Proc. of Asia-Pasific Workshop on Fund. & Appl. of Adv. Semicond. Devices (Busan, 2003) p. 151.*
5. M. Ikeda, et al., Jpn. J. Appl. Phys. 42 (2003) 4131.
6. K. Makihara, et al., *Dig. of Papers on 2004 Int. Conf. on Micorprocess and Nanotechnology (Osaka, 2004) p.216.*
7. Y. Darma, et al., Jpn. J. Appl. Phys. 42, 6B (2003) 4129.
8. K. Takeuchi, et al., *Proc. of ECS Int. Semicond. Technol. Conf. (Tokyo, 2003) p.1.*
9. Y. Darma, et al., *Ext. Abst. of Int. Conf. on Solid State Devices and Materials (Tokyo, 2003) p. 300*
10. S. Miyazaki, et al., *Abst. of Int. Symp on Nanoscale Devices and Materials in ECS Meeting (Hawaii, 2004) 1013; Proc. of IU-MRS (Hsinchu, 2004) Invited*
11. T. Nagai et al., *Ext. Abst. of Int. Conf. on Solid State Devices and Materials (Tokyo, 2004) p.126.*

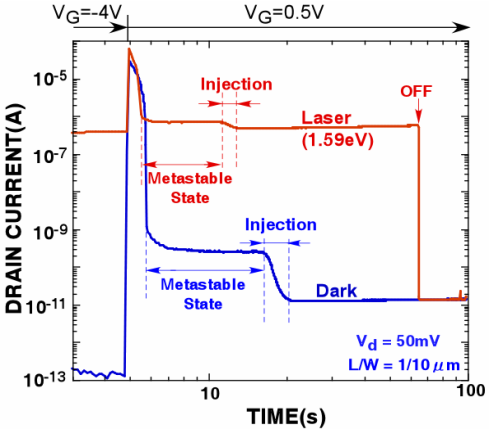

Fig. 2 Temporal changes in the drain current measured at V_g = 0.5V under irradiation of 780nm (1.59eV) light and dark condition after complete discharging of the Si-QDs floating gate at V_g = -4V.

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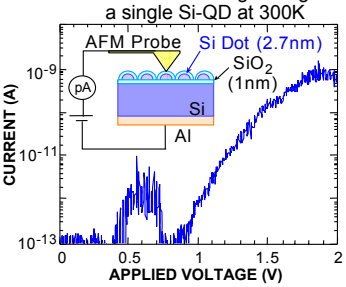
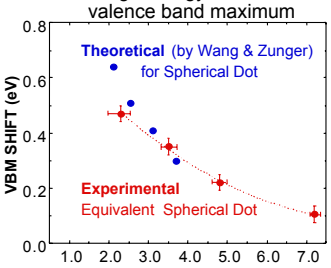
Silicon Quantum Dots for New Functionality

Resonant tunneling through a single Si-QD at 300K



M. Fukuda et al. APL (1997)

High energy shifts in valence band maximum



S.A.Ding et al. APL (1998)

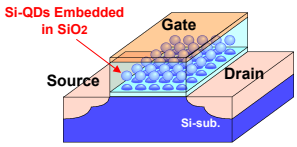
- Quantum Size Effect
- Coulomb Blockade

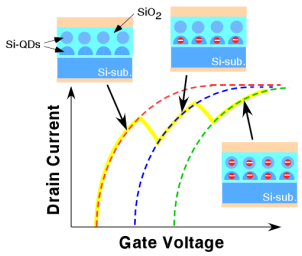
⇨ Novel Functional Devices

- **QDs Floating Gate Memory** — A. Kohno et al. JJAP (2001); S. Tiwari et al. APL (1996)
- **Single Electron Transistor** — Y. Takahashi et al. IEDM (1994, 1998)

Si-QDs Floating-Gate MOS Memories
Multivalued & Low-Voltage Operations at Room Temp.

Floating Gate Application of Si Quantum Dots





☆ **Control of Discrete Charged States in Si-QDs**

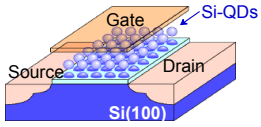
⇩

Electrical Interaction & Coupling among Electronic States in Neighboring QDs

Key Issues on Si-QDs Formation for Floating Gate Application

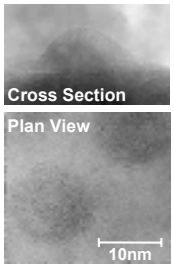
- The areal dot density comparable to the electron concentration in channel (higher than ~10^{11}cm^{-2})

☆ Uniformity in Size & Spatial Distribution

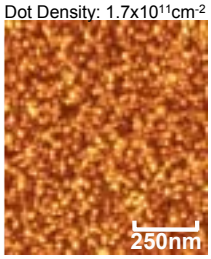


Spontaneous Formation of nc-Si on SiO_2 by LPCVD

HR-TEM Images



AFM Image
Dot Density: 1.7x10^{11}cm^{-2}

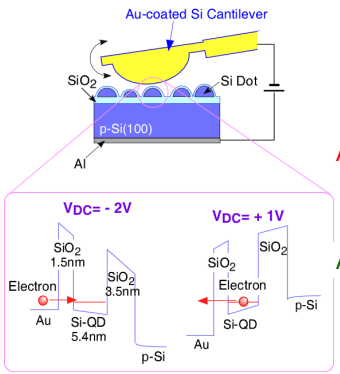


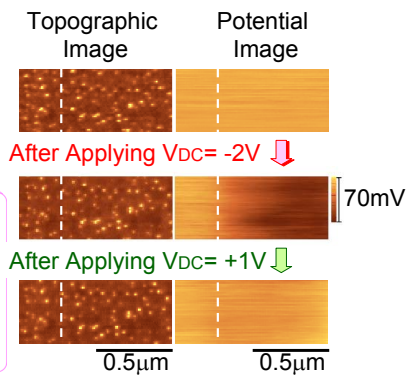
on as-grown SiO_2 600℃, 0.2Torr, 36s

on HF-treated SiO_2 560℃, 0.2Torr, 90s

S.Miyazaki et al. TSF (2000)

Surface Potential Changes due to Electron Charging & Discharging of Si-QDs as Detected by a AFM/Kelvin Probe Method

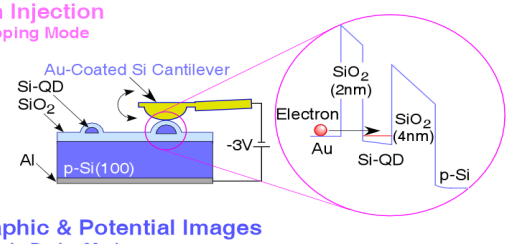




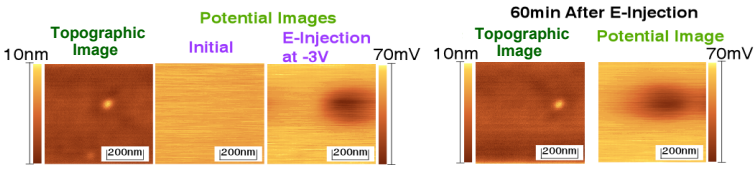
N. Shimizu et al, JJAP 39 (2000)2318

Electron Injection to Single Si-QD

- **Electron Injection** in AFM/Tapping Mode

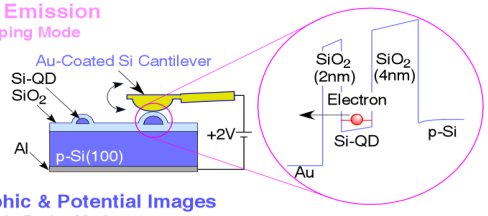


- **Topographic & Potential Images** in AFM/Kelvin Probe Mode



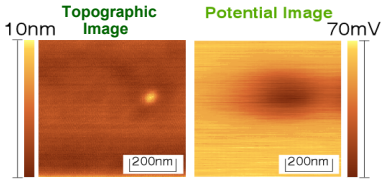
Electron Emission from Charged Single Si-QD

- **Electron Emission** in AFM/Tapping Mode

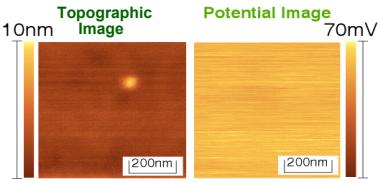


- **Topographic & Potential Images** in AFM/Kelvin Probe Mode

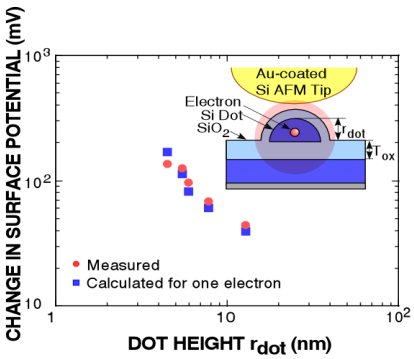
60min After E-Injection in CR Air at RT



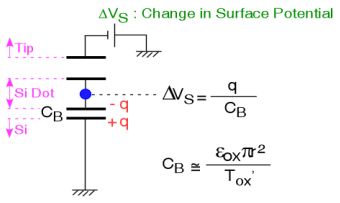
E-Emission at +2V



Dot Size Dependence of Surface Potential Changed by Electron Injection



An Equivalent Circuit Under KFM

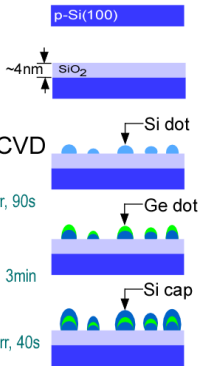


$r = r_{dot} + \Delta r$: Spread of Electric Lines of Force

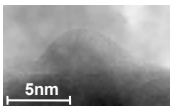
$T_{ox}' = T_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{r_{dot}}{2}$ εDielectric Const.

Formation of Si Dots with a Ge Core

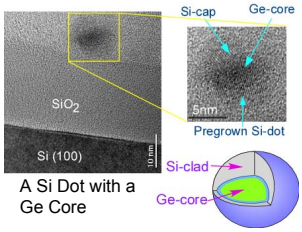
- **Precleaned HF-last:** $NH_4OH:H_2O_2:H_2O$=0.15:3:7; 80°C,10min and 4.5% HF 2min
- **Oxidation:** 2% O_2, 1000°C, 10min
- **Dot Formation by LPCVD**
  - Si-Dot: 100% SiH_4, 560°C, 0.1Torr, 90s
  - Ge-Core: 5% GeH_4, 400°C, 0.2Torr, 3min
  - Si-Cap: 100% SiH_4, 540°C, 0.02Torr, 40s



Cross-sectional TEM Images



A Si Dot pre-grown on SiO_2



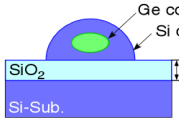
A Si Dot with a Ge Core

Y. Darma et al. JJAP (2003)

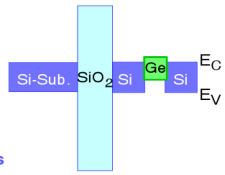
Characterization of Electron Charging into an Isolated Si Dot with Ge core

- **Dry Oxidation** 1000℃, 2% O_2, 10min
- **LPCVD**
  - SiH_4: 560℃, 0.1Torr, 90sec
  - GeH_4: 400℃, 0.2Torr, 180sec
  - SiH_4: 560℃, 0.02Torr, 40sec
  - Dot Density: ~2X10^8cm^{-2}

Si Dot with Ge core

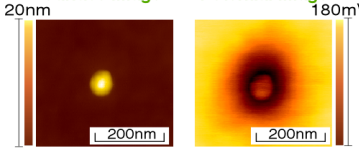


Energy Band Structure of Si Dot with Ge core

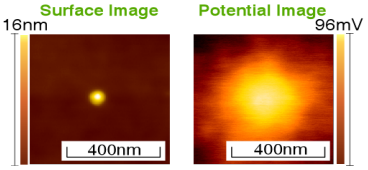


Topographic & Potential Images in AFM/Kelvin Probe Mode

E-Injection at -3V

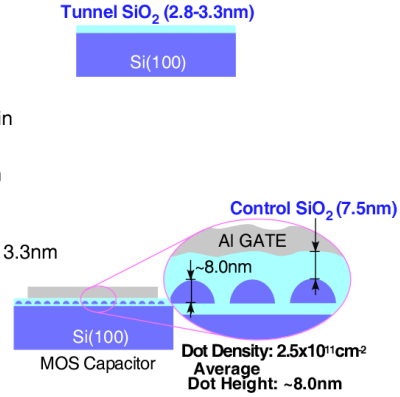


E-Extraction at +3V

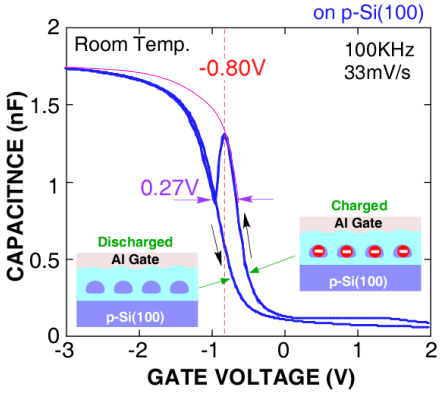


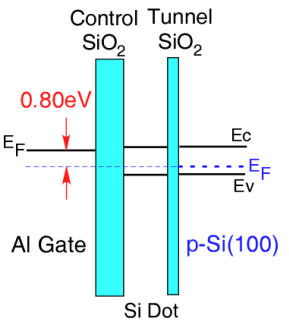
Fabrication of Si-QDs Floating Gate MOS Capacitors

- p-Si(100) (8-12 Ωcm)
  n-Si(100) (0.19 Ωcm)
- **Oxidation** 2%O_2 in N_2: 1000°C
- **0.1% HF Treatment**
- **Si-QDs Fabrication by LPCVD** SiH_4: 570°C, 0.2Torr, 1min
- **Oxidation of Si-QDs Surface** 2%O_2 in N_2: 850°C, 1min
- **a-Si Deposition & Oxidation**
  - a-Si Deposition Si_2H_6: 440°C, 0.2Torr, 3.3nm
  - a-Si Oxidation 2%O_2 in N_2: 1000°C
- **Gate Fabrication** Al Gate 1mmϕ

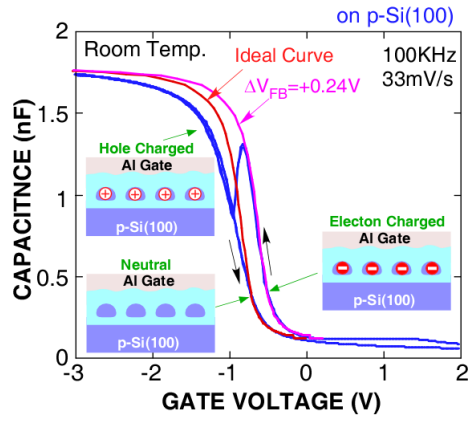


C-V Characteristics of a MOS Capacitor with Si-QDs Floating Gate

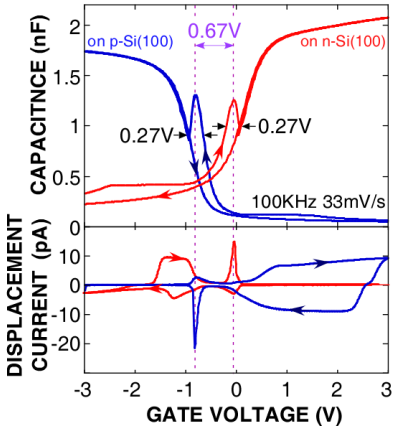




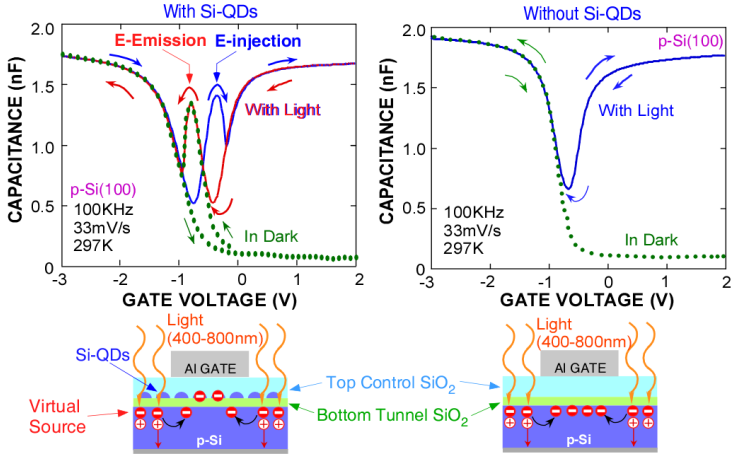
Comparison between Measured and Simulated C-V Curves for Si-QDs Floating Gate MOS Capacitor



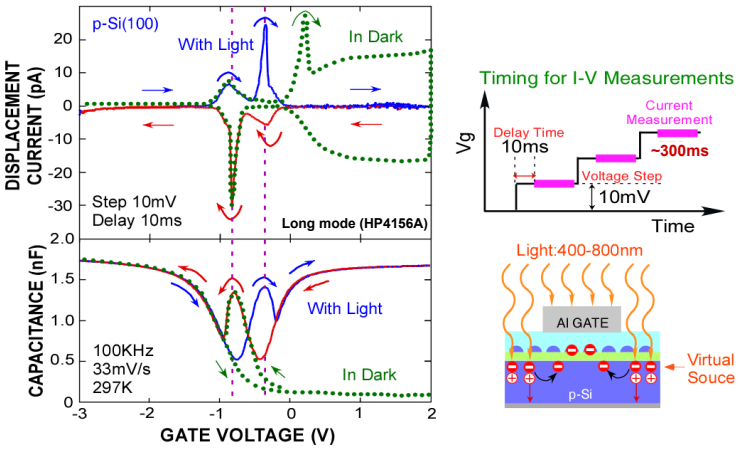
C-V & I-V Characteristics of Si-QDs Floating Gate MOS Capacitors Fabricated on p-Si(100) & n-Si(100)



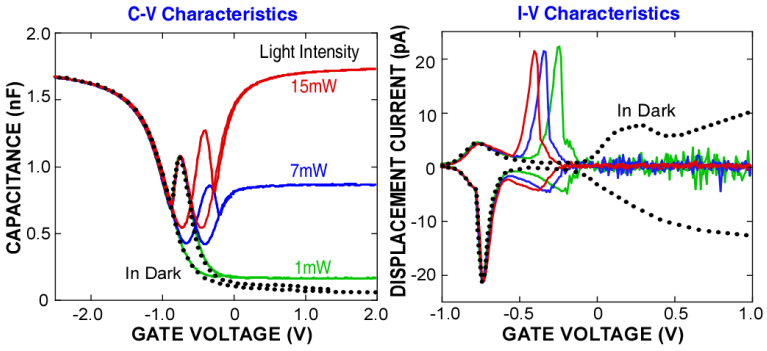
C-V Characteristics of MOS Capacitors with & w/o Si-QDs Floating Gate Measured in Dark and under Cold Light Irradiation



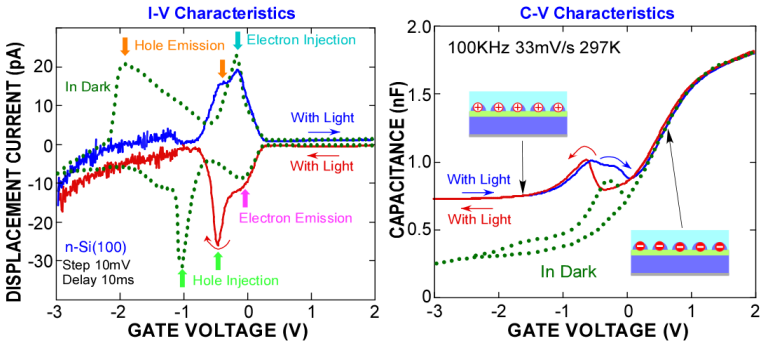
I-V & C-V Characteristics of Si-QDs Floating Gate MOS Capacitor Measured in Dark & under Cold Light Irradiation



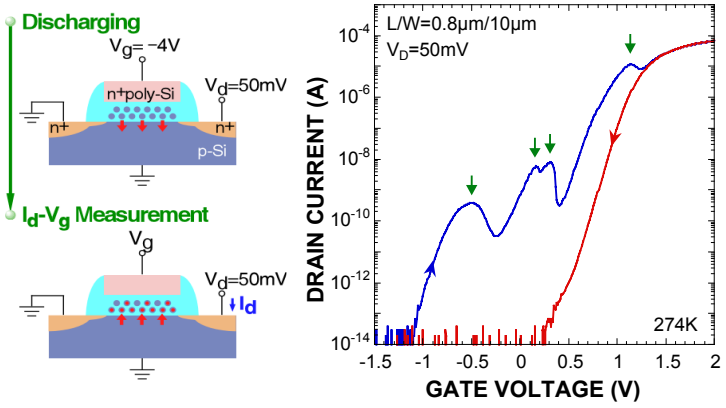
I-V & C-V Characteristics of Si-QDs Floating Gate MOS Capacitor Measured in Dark & under Cold Light Irradiation — Light Intensity Dependence —



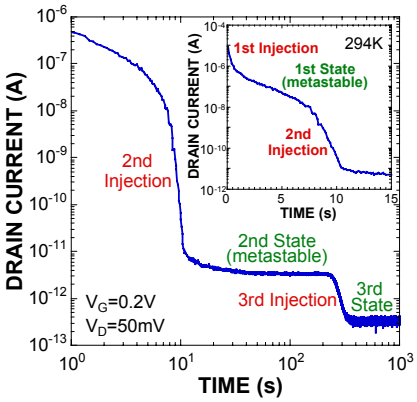
I-V & C-V Characteristics of Si-QDs Floating Gate MOS Capacitor Measured in Dark & under Cold Light Irradiation



I_d-V_g Characteristics for MOSFET with Doubly-Stacked Si-QDs Floating Gate

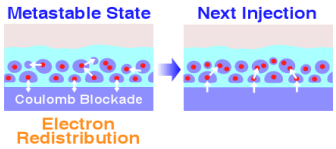


Transient I_d Characteristics by Electron Charging to Doubly-Stacked Si-QDs Floating Gate

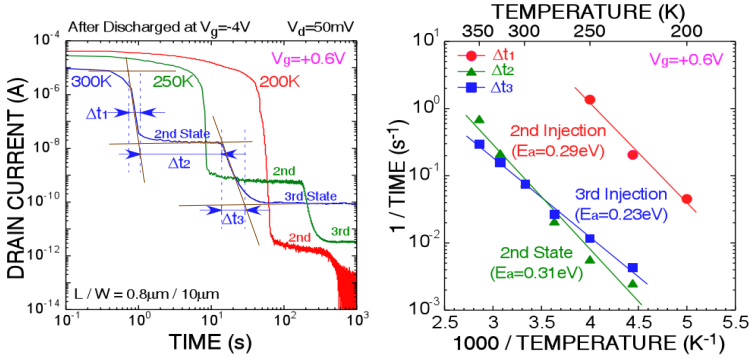


- ☆ Multiple-Step Electron Injection
- ☆ Incubation period between electron injections

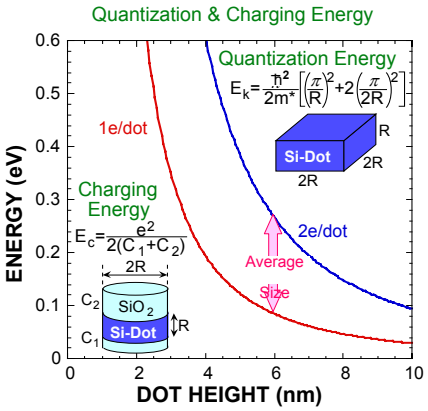
During each metastable state, electrons injected in Si-QDs floating gate are likely to be redistributed for the next electron injection.

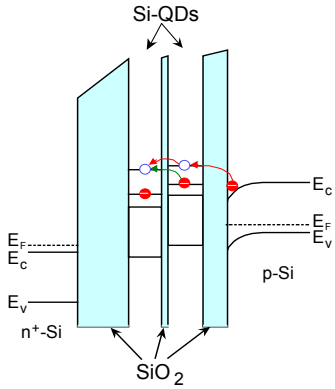


Temperature Dependence of I_d-t Characteristics



Model for Electron Charging in Si-QDs Floating Gate





SUMMARY

Self-Assembling Formation of Si-QDs on SiO_2 by LPCVD

Electron Injection to & Extraction from Isolated Si-QD

- Pure Si-QD: Single Electron Storage at RT
- Si-QD with a Ge Core :
  Storage of Electrons in the Si Clad & Holes in the Ge Core

MOS Cap. and n-MOSFETs with Si-QDs Floating Gate

- Room Temperature Memory Operation
- ☆ Multistep Electron Charging

Well-defined & Multivalued Memory Operation

➡ Optimization of Dot Size & Oxide Thickness
Control of Dot Arrangement

Acknowledgement

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