Fabrication of Multiply-Stacked Structures of Si Quantum-Dots Embedded in SiO_2 by Combination of Low-Pressure CVD with Remote Plasma Treatments

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Introduction

Silicon nanocrystals embedded in SiO_2 network have attracted a great deal of interest as quantum dots with discrete charged states and their application to the floating gate of MOS memories [1]. For the multivalued capability of the Si dots floating gate MOS devices, the growth control of Si quantum dots (Si-QDs) with an areal density as high as ~ 10^{12} cm^{-2} on an ultrathin SiO_2 layer is a crucial factor. In our previous work, we demonstrated the self-assembling formation of Si-QDs on ultrathin SiO_2 layers by controlling the early stages of low-pressure chemical vapor deposition (LPCVD) using a SiH_4 gas [2]. Also, we reported that the SiO_2 surface treatment with a dilute HF solution is quite efficient to form dots with high areal density and high size uniformity because Si-OH bonds created on the SiO_2 surface act as reactive sites to precursors such as SiH_2 during LPCVD. In addition, by spatially controlling OH termination of the SiO_2 surface before LPCVD, the selective growth of Si dots has been demonstrated [3]. More recently, we have also reported that, by exposing as-grown SiO_2 surface to a remote Ar plasma and subsequently to a remote H_2 plasma, OH bonds are efficiently created on the SiO_2 surface and results in the Si dot formation with fairly uniform size distribtution and high areal dot density as in the case of wet-chemical treatment using a dilute HF solution [2].

In this work, we extended our research work to fabricate multiply-stacked structures consisting of Si-QDs and ultrathin SiO_2 by alternately repeating the Si dot formation by SiH_4-LPCVD and the dot surface modification by remote plasma treatments in which surface oxidation and subsequent OH termination are preformed by exposing to remote O_2 plasma and remote Ar/H_2 plasma, respectively. And electron charging and discharging characteristics of Si-QDs stacked structure as a floating gate in MOS capacitors has been studied.

Experimental

For the first formation of Si-QDs, a 4 nm-thick SiO_2 layer was grown on n^+-Si(100) at 1000ºC in dry O_2 and the SiO_2 surface was exposed to pure Ar remote plasma and subsequently to pure H_2 remote plasma at 560 ºC for 1min in each plasma treatment. The remote plasma was generated in a quartz tube with a size of 10 cm in diameter by inductively-coupling with an external single-turn antenna connected to a 60 MHz generator through a matching box. The sample was placed on the susceptor at a distance of 32 cm away from the position of the antenna to eliminate ion damage. The VHF power and the gas pressure for the remote Ar plasma pretreatment were maintained at 100 W and 0.1 Torr, respectively, and for the remote H_2 plasma treatment at 200 W and 0.2 Torr, respectively. After remote plasma treatments, the formation of Si dots was carried out on plasma-treated SiO_2 in the same reaction chamber at 560ºC by LPCVD using pure monosilane under 0.5 Torr. And subsequently the surface oxidation of Si dots was performed at the same temperature by a remote VHF plasma of 1% O_2 diluted with He generated at 50 W and 0.1Torr. When HF-last n^+-Si(100) was exposed to the remote O_2 plasma, 2.4nm-thick SiO_2 was formed uniformly by 10 min exposure. For the fabrication of the stacked structures of Si-QDs, the above-mentioned process steps of remote Ar/H_2 plasma treatments, LPCVD and remote plasma oxidation were repeated at 560ºC. In the floating gate application, to form a 7.5nm-thick control oxide conformally on the dot layer, amorphous Si layer was grown on formed Si dots by LPCVD of 10% Si_2H_6 diluted with He at 440 ºC, then the a-Si layer was fully oxidized in dry O_2 at 1000 ºC. Finally, Al gates were evaporated to form MOS capacitors.

Results and Discussion

From the analysis of the Si2p spectra for the thermally-grown SiO_2 layer before and after remote Ar plasma and subsequent H_2 plasma treatments, the formation of surface OH bonds is suggested with no etching or sputtering. After the first formation of Si-QDs, AFM observations using a Rh-coated Si_3N_4 cantilever confirm the formation of the Si dots with an areal dot density as high as $\sim 6\times 10^{11}$ cm^{-2} and a dot height of ~4.5 nm on the plasma-treated SiO_2 surface. Also, no change in the surface morphology was detected after exposing to remote O_2 plasma, indicating uniform oxidation of Si-QDs surface. After 10 cycles of Si dot formation and remote plasma treatments, the fabrication of the stacked structure as expected was confirmed by cross-sectional TEM observations as shown in Fig. 1. In the high-resolution images as seen in Fig. 1 (b) and (c), we found that Si nanocrystallites with a size of ~ 4 nm are stacked with ~2 nm-thick SiO_2 interlayers.

The capacitance-voltage (C-V) and current-voltage (I-V) characteristics of MOS capacitors with a floating gate consisting of 6 stacked Si-QDs show unique hystereses as shown in Fig. 2. When the gate voltage is swept over ~0.7 V and backward from the accumulation, a flat-band voltage shift of ~0.24 V from the corresponding ideal curve is observed. The capacitance peak measured around the flat-band voltage can be attributed to the electron injection to the Si-QDs floating gate from the substrate as seen in the I-V curve. The discharging current was also measured in the voltage scan backward from the accumulation state.

In conclusion, the combination of LPCVD and remote plasma treatments demonstrated in this work is a practically promising way to fabricate multiply-stacked structures consisting of Si-QDs and ultrathin SiO_2 interlayers and will lead us to new device application as well as to the floating gate application.

References

[1] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. 40 (2001) 721.

[2] S. Miyazaki, Y. Hamamoto, E. Yoshida, M. Ikeda and M. Hirose, Thin Solid Films 369 (2000) 55.

[3] S. Miyazaki, M. Ikeda, E. Yoshida, N. Shimizu and M. Hirose, Proc. of 25th Int. Conf. on. Phys. of Semicond., (Osaka, 2000) p.373.

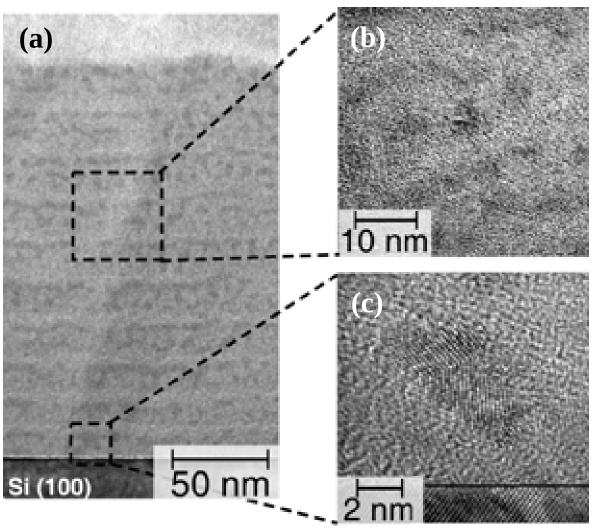

Fig. 1. Cross-section TEM images of multiple stacked structure of Si dots and SiO_2 interlayers.

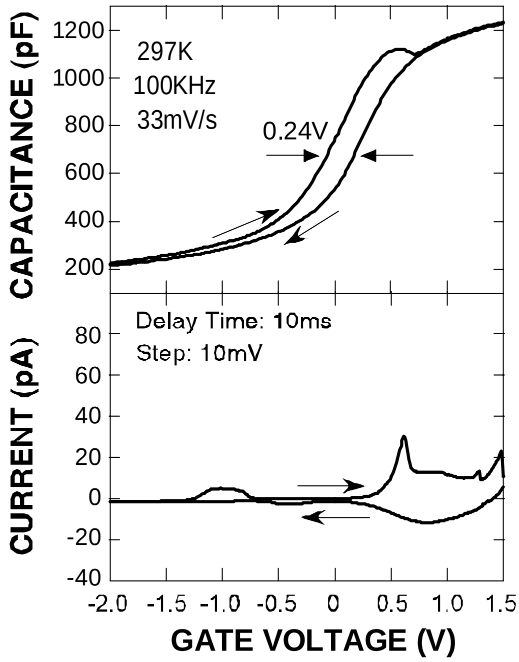

Fig. 2. Capacitance-voltage (a) and current-voltage (b) characteristics of Si dots floating gate MOS capacitors fabricated on n^+-Si(100) at room temperature. The sweep rate was 33 mV/s for C-V measurements and for I-V measurements, the delay time was set at 10 ms.

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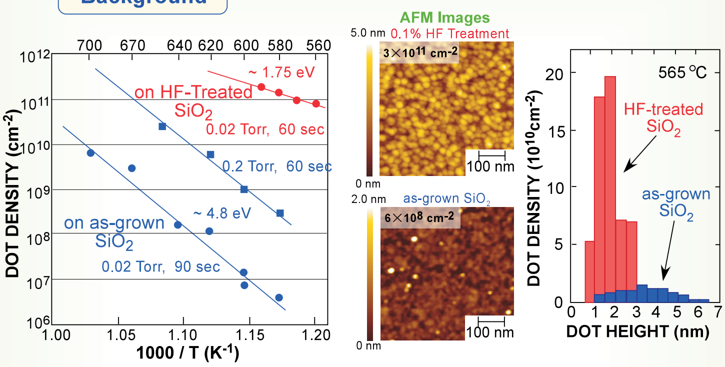
Abstract

We fabricated **multiply-stacked structures** consisting of Si-QDs and ultrathin SiO_2 by alternately repeating the Si dot formation by SiH_4-LPCVD and the dot surface modification by remote plasma treatments in which surface oxidation and subsequent OH termination are preformed by exposing to remote O_2 plasma and remote Ar/H_2 plasma, respectively. And electron charging and discharging characteristics of Si-QDs stacked structure as a floating gate in MOS capacitors has been studied.

Background

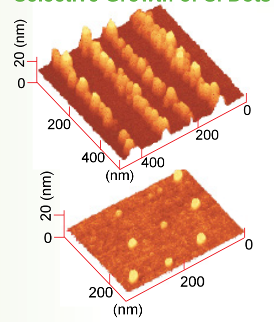


S. Miyazaki et al., Thin Solid Films ***369****(2000) 55-59.*

Dilute HF Treatment

The dot density as high as $10^{11}cm^{-2}$ can be achieved and also the dot size uniformity is improved significantly.

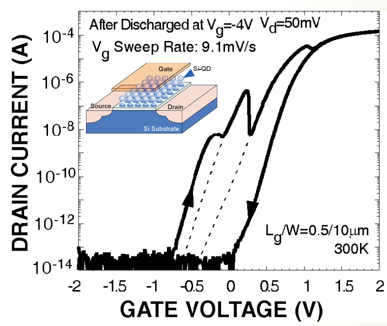
Selective Growth of Si Dots



Spatial control in Si dot formation

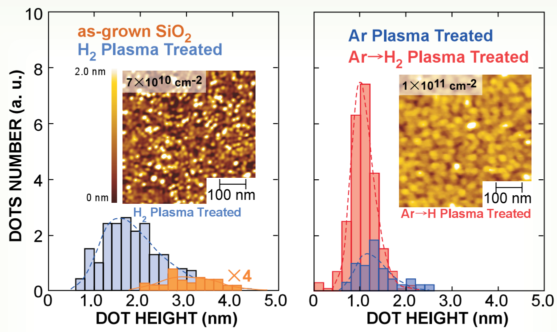
S. Miyazaki et al., Proc. of 25th Int. Conf. on.Phys. of Semicond, (Osaka, 2000) 373.

Si-QDs Floating Gate MOSFETs



Multivalued memory operations even at room temperature

M. Ikeda et al., Jpn. J. Appl. Phys. ***42*** *(2003) 4134-4137*



K. Makihara et al., Proc. of 12th Int. Conf. on Solid Films and Surface, (Hamamatsu, 2004) 373.

This Work

Fabrication of Multiply Stacked Structure consisting of Si dots and Ultrathin SiO_2

Si dot formation by SiH_4-LPCVD and dot surface modification by remote plasma treatment (remote O_2 plasma and remote Ar + H_2 plasma)

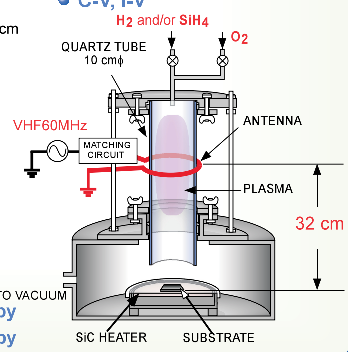
Experimental

Substrate : n^+-Si(100)

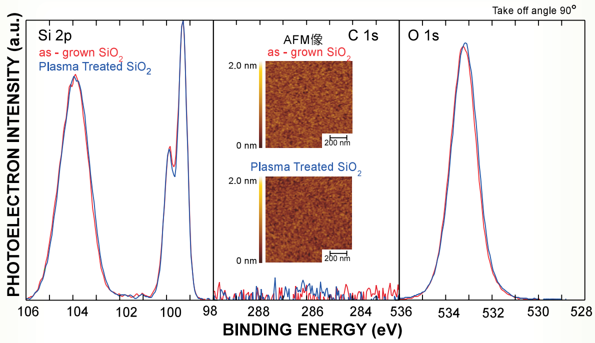
- **Thermal Oxidation**
  - ~ 4.2 nm-thick SiO_2
  - 1000 ℃, 2% O_2 in N_2
- **Surface Modification**
  - Inductively-Coupled Plasma
    - 60 MHz
    - Single-turn Antenna
    - Antenna-Substrate Distance : 32 cm
  - Remote **Ar** Plasma
    - 100 W, 0.1 Torr, 1 min,
  - Remote H_2 Plasma
    - 200 W, 0.2 Torr, 1 min,
- **Si-Dots Formation**
  - LPCVD (**560 ℃ , 0.2 Torr,** SiH_4)
- **Remote Plasma Oxidation**
  - Remote O_2 Plasma
  - ~ 2nm-thick SiO_2
    - 560 ℃ 1%O_2 in He
    - 50 W, 0.1 Torr, 10 min,
- Atomic Force Microscopy
- Transmison Electron Microscopy
- X-ray Photoelectron Spectroscopy

3, 6, 9, 10 cycles

- **a-Si Deposition & Oxidation**
  - a-Si Deposition
    - Si_2H_6, 440 ℃, 0.2 Torr
  - a-Si Oxidation
    - 1000 ℃, 0.2 Torr, 25 min,
    - ~7.5 nm-thick SiO_2
- **C-V, I-V**

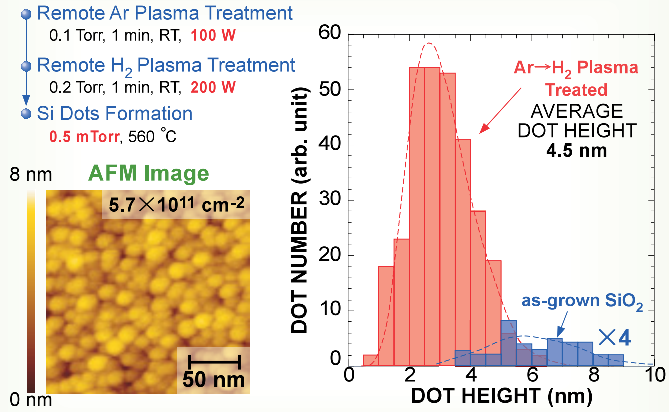


Si2p, C1s & O1s Spectra and AFM Images for SiO_2 Before & After Remote Ar + H_2 Plasma Treatment



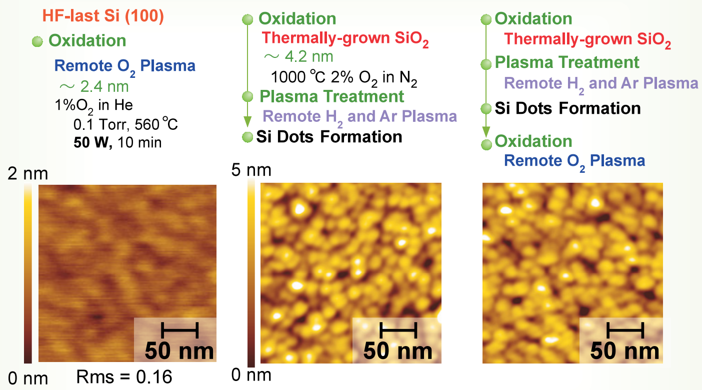
- No change in the surface microroughness was observed, by the remote plasma treatments in the experimental conditions.
- No changes in Si2p and O1s signal intensity indicate no changes in the oxide thickness and also no surface contamination especially with CHx were detected before and after the remote plasma treatments.

Influence of Remote Plasma Treatments on the Si Dot Formation



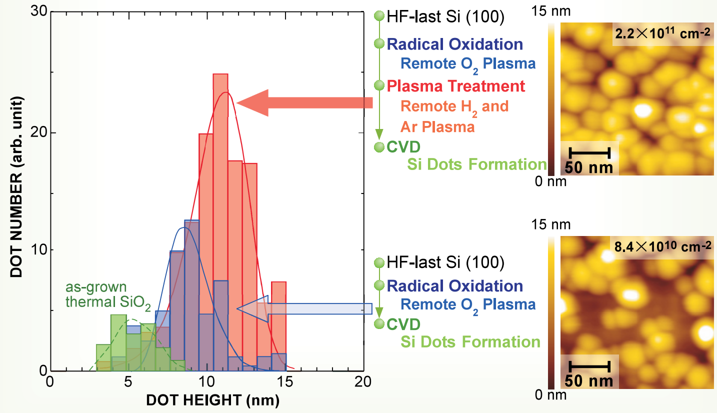
- The combination of a remote Ar plasma pretreatment with subsequent H_2 plasma treatment enables us to form Si dots with a high density and good size uniformity.

Influence of Remote O_2 Plasma Oxidation of Si Dots

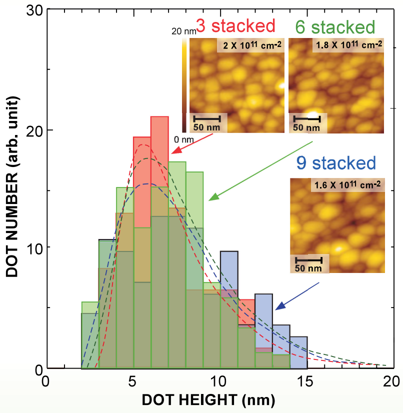


- No change in the surface morphology was detected after exposing to remote O_2 plasma, indicating uniform oxidation of Si-QDs surface.

AFM Images and Dot Size Distribution Influence of Radical Oxidation on the Si Dot Formation

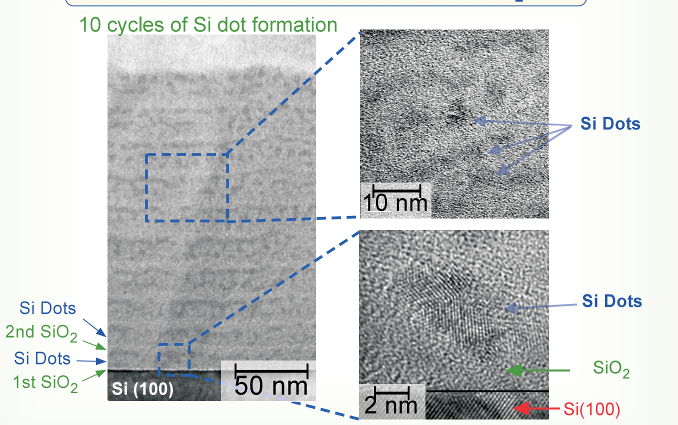


AFM Images and Dot Size Distribution of 3, 6 and 9 Stacked Structure



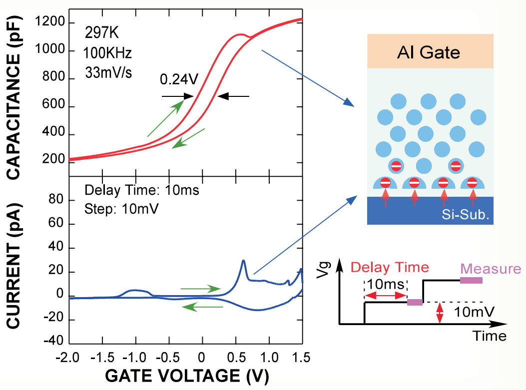
- Dot size distribution is almost unchange with increasing number of stack.

Cross-Sectional TEM Images for Multiple-Stacked Structure of Si Dots Embedded in SiO_2



- Si nanocrystallites with a size of ~ 4 nm are stacked with ~2 nm-thick SiO_2 interlayers.

C-V and I-V Characteristics of MOS Capacitors with a Floating Gate Consisting of 6 Stacked Si Dots



- C-V and I-V characteristics of MOS capacitors with a floating gate consisting of 6 stacked Si-QDs show unique hystereses.
- The capacitance peak measured around the flat-band voltage can be attributed to the electron injection to the Si-QDs floating gate from the substrate as seen in the I-V curve.

Conclusions

- The combination of the remote Ar plasma and subsequent H_2 plasma is quite effective to achieve a **uniform size distribution** of Si dots with an areal density of the order of **10^{11} cm^{-2}**.
- The combination of LPCVD and remote plasma treatments is a practically promising way to fabricate **multiply-stacked structures consisting of Si-QDs** and **ultrathin SiO_2 interlayers**.

The result will lead us to **optoelectronic device application** as well as to the floating gate application.

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