Characterization of Interfacial Oxide Layers in Heterostructures of Hafnium Oxides Formed on NH₃-nitrided Si(100)

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1. Introduction
Control of interfacial oxidation is one of key issues to implement high-k gate dielectrics in the sub-100nm CMOS generations where the SiO₂ equivalent thickness of the high-k dielectrics stack structures below 1.2nm is required imperatively [1]. From the requirement for the gate dielectric application such as high dielectric constant (~25) and favorable band offset energy (>1.2eV), HfO₂ and ZrO₂ are promising candidates for SiO₂ substitution [2]. However, since such transition oxides are good conductors for oxygen ions, the oxide deposition on Si(100) and post-deposition anneal are always accompanied with the interfacial oxidation [3]. In this work, the interfacial oxidation in the heterostructures ultrathin HfO₂ formed on thermally-nitrided Si(100) has been studied by x-ray photoelectron spectroscopy (XPS) and Fourier transform infrared attenuated total reflection (FT-IR ATR) measurements.

2. Experiment
2.5nm-thick HfO₂ layers are prepared on thermally grown SiNx(x=−1.3, ~1.0nm in thickness) /Si(100) at room temperature by HfO₂ evaporation in ambient O₂ at ~1x10⁻⁹Pa. The thermal nitridation of Si(100) was carried out at 700°C in ambient NH₃ at 54Pa. After the HfO₂ evaporation, the samples were annealed at 300~500°C in ambient O₂ at 34Pa for 5min.

3. Results and Discussion
The stability of ultrathin silicon nitride so prepared against oxidation was first examined. No changes in Si2p and N1s spectra between the samples before and after O₂ anneal at 500°C were observed. The result indicates that the nitrided surface is stable enough against the O₂ anneal. In contrast to this, when the stack structure of HfO₂ on nitrided Si(100) was annealed in the same condition, the interfacial oxidation proceeds markedly. As shown in Fig. 1, an increase in the chemically-shifted Si2p signals by the O₂ anneal was observed, indicating the growth of interfacial oxide. From the intensity ratio of the chemically-shifted Si2p signals to the signals from the Si substrate, it is found that the interfacial layer is grown up to 2.2nm in thickness from 1.0nm. By the complete removal of the top HfO₂ layer from the O₂ anneal sample with a dilute HF etching, the signals in the lower binding energy side of the Si⁴⁺ peak are reduced by amount of two monolayers at most. Considering the 2nd nearest neighbor effect on the Si2p chemical shift, the reduced signals can be attributed to Si⁴⁺ states at the interface between the top HfO₂ layer and the newly grown interfacial oxide because there exist less-electronegative Hf atoms as the 2nd nearest neighbors of Si at the interface. The observed change in the N1s spectrum by the HfO₂ deposition on nitrided Si(100) is interpreted in terms that the N-H bonds on the nitride surface are changed partly into HF-N bonds during the HfO₂ deposition. The O₂ anneal of HfO₂/nitrided Si(100) causes a new component in the N1s spectrum at the higher binding energy side, which is attributable to the oxidation of the nitride surface. The partially oxidized component in the N1s spectra was examined by subtracting the reference N1s spectrum of nitrided Si(100) from the N1s spectra measured at each thinning step in a dilute HF solution as shown in Fig. 2. Taking into account the fact that such a wet etching introduces a oxidized component on the surface with a monolayer level, the oxidized component detected in the case of 0.3nm in remaining layer thickness is thought to be caused by the wet etching. The result of Fig. 2 indicates that the silicon oxide layer is formed on the pre-grown nitrided layer and interestingly the nitride layer thickness almost remains unchanged. Namely, we suggest that the oxidation of SiNx is accompanied with the movement of N atoms towards the substrate side resulting in the nitridation of the Si surface. This was also confirmed by p-polarized FT-IR-ATR measurements using a Ge prism as shown in Fig. 3. In the case that HfO₂ was directly formed on HF-last Si(100), an absorption band peaked around 1230cm⁻¹ due to Si-O-Si LO phonons is remarkably increased by the O₂ anneal. In fact, the change in the spectrum between the samples before and after the O₂ anneal is almost identical to the ATR spectrum of ultrathin SiO₂, where the interfacial silicon oxide layer is grown up to 2.2nm form ~0.6nm (in the as-evaporated state) as obtained from the XPS analysis. In contrast, for the stack structure of HfO₂ on nitrided Si(100), an increase in the absorption band originating from the silicon oxide layer by the O₂ anneal with the same condition is suppressed significantly. Notice that there is no significant change in the absorption band around ~1100cm⁻¹ due to the Si-N network.
the chemical bonding features of N atoms is almost unchanged by the O₂ anneal although the silicon oxide layer is formed on the nitride layer. When the O₂ anneal temperature is decreased down to 300ºC, no interfacial oxidation proceeds for the stack structure of HfO₂ on nitrided Si(100) as indicated in Fig. 4. Consequently, even in the case with a use of ultrathin SiNx as an oxidation barrier layer, the control of O₂ partial pressure is required to avoid the interfacial oxidation during the thermal anneal higher than 350ºC.

4. Conclusions

For the stack structure of HfO₂ on nitrided Si(100), the formation of the interfacial oxide layer is not completely suppressed with a 1.0nm-thick SiNx layer pregrown by direct nitridation at 700ºC in ambient NH₃. This result is attributed to the fact that the surface oxidation of the SiNx layer induces the movement of N atoms towards the substrate side and results in the nitridation of the Si surface.

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References

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OUTLINE
1. Motivation & Background
2. Sample Preparation & Experimental Procedure
3. Characterization
   - Blocking Properties of Pregrown SiN$_x$ against Oxidation
   - Chemical Bonding Features in the Interfacial Oxide
4. Summary

SUB-100nm Technology Generation of CMOS Devices
Aggressive scaling of gate dielectric thickness below 1.5nm in EOT
Exponential increase in direct tunneling current with decreasing SiO$_2$ thickness
Intense efforts in the replacement of conventional SiO$_2$-based gate dielectrics with physically-thicker high-k dielectrics

One of the major research issues for the high-k gate dielectric technology
- Control of the interfacial layer between high-k materials and Si(100)
- Suppression of undesirable interfacial oxidation & interface defect generation

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SAMPLE PREPARATION & EXPERIMENTAL PROCEDURE
- Substrates: p-Si(100)
- Precleaning
  - NH$_4$OH:H$_2$O$_2$:H$_2$O=0.15:3:7 (80°C, 10 min)
  - Pure water Rinse
  - NH$_3$ Anneal : SiO$_2$:N
  - SiO$_2$-thinning to ~0.6 nm
  - 500°C in Dry O$_2$
- O$_2$ Anneal
  - NH$_4$OH:H$_2$O$_2$:H$_2$O=0.15:3:7 (80°C, 10 min)
- HfO$_2$ Evaporation
  - 850°C, 2.5 Torr
- HfO$_2$ Evaporation
  - 500°C; 10 s & 5 min
- In 0.1% HF Treatment for HfO$_2$ removal
- X-Ray Photoelectron Spectroscopy (XPS)
- Fourier Transform Infrared Attenuated Total Reflection (FT-IR-ATR)
- Transmission Electron Microscope (TEM)

Si$_2$p & N$_1$s Spectra for SiN$_x$/Si(100) Before & After O$_2$ Annealing

Si$_2$p & N$_1$s Spectra for SiN$_x$/Si(100) Before & After O$_2$ Annealing

Si$_2$p & N$_1$s Spectra for SiN$_x$/Si(100) Before & After O$_2$ Annealing
3.5nm-Thick HfO\(_2\) Evaporated on NH\(_3\)-nitrided Si(100) Before & After O\(_2\) Annealing

### Photoelectron Yield Spectra
- As-evaporated
- H-terminated
- O\(_2\)-annealed

### Energy Band Diagram
- \(\Delta V\)
- \(E_v\)
- \(E_c\)
- \(h\nu = 5.7\text{eV}\)

### The Electronic-Active Defect States in SiN\(_x\) & the Interfacial Layer

### Photoelectron Yield Spectra
- As-nitrided
- H-terminated
- As-500anneal

### Filled Interface States
- As-nitrided
- 0.1%HF-etching (1.5nm)

### Summary
- The formation of the interfacial oxide layer is not completely suppressed with a 1.0nm SiN\(_x\) layer prepared by 700°C NH\(_3\)-nitridation.
- SiN\(_x\) surface oxidation induces the movement of N atoms towards the substrate interface and promotes the nitridation of Si surface.
- The control of O\(_2\) partial pressure is required to avoid the interfacial oxidation during the thermal anneal higher than 350°C.

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