Anomalous Behavior of Interface Traps of Si MOS Capacitors Contaminated with Organic Molecules

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1. Introduction

Recently, influences of gas phase organic contaminants on the Metal-Oxide-Semiconductor (MOS) devices are attracting much attention. However, the influences of organic molecules on the characteristics of MOS devices are not yet understood well. We have reported the influences of organic contaminants on the reliability of gate insulators and interface traps of MOS devices.[1] Recently, we found that the interface traps are generated by the reverse bias stress for the organic contaminated samples, and they are self healed after stop of the bias stress.[2] In this paper, we have investigated this phenomenon further in detail. As a result the mechanism of the anomalous capacitance change is analyzed, and we newly propose a model for the self-healing of the interface traps.

2. Experiment

We fabricated MOS capacitors by oxidizing (5 nm) Si wafers with different surface contamination levels. The structure and fabrication process of the samples are shown in Fig. 1. Three kinds of samples were fabricated after storing (1) in Front Opening Unified Pod (FOUP) made of plastic for 24 h (highest contamination level), (2) in FOUP with photocatalyst cleaning unit[3] for 24 h (medium contamination level), and (3) immediately oxidized without storage (control samples). Capacitance-Voltage (*C-V*) measurements were carried out at 1 kHz.

3. Results and Discussions

3.1. Evaluation of stress induced interface traps

C-V characteristics for three kinds of the samples with different contamination levels after reverse bias stress (V_G=+10 V, E_{ox}=2.04x10^7 V/cm, current=5.37x10^{-8} A/cm^2) are shown in Fig. 2 with a parameter of stress time. The theoretical low frequency *C-V* curve is also shown. In this figure, anomalous capacitance peaks appears in inversion region. Since the position of the measured capacitance increase is close to the increase position of the theoretical low frequency *C-V* curve in inversion region, the origin of the capacitance peaks is thought to decrease in the generation life time (τ_g) of the minority carrier (electron).[4] The τ_g is roughly expressed as

$$\tau_g \propto \frac{1}{\sigma_n v_{th} N_t} \qquad (1)$$

where σ_n is electron capture cross section, v_{th} is the carrier thermal velocity, and N_t is the interface trap density.[5] The τ_g is shorter when σ_n or N_t becomes larger. Figure 3 shows histograms of the generated peak height (ΔC) at V_G=3.7 V for the three kinds of samples after 60 min stress. The ΔC is higher for the higher contamination level as expected. Table 1 shows the amount of organic molecules adsorbed on the Si wafer stored in FOUP for 6 h. The measured organic contamination level is consistent with the result of the contact angle of pure water on SiO_2 (Fig. 4). Considering the above experimental results, it is thought that the τ_g becomes shorter with increase in interface trap density due to the organic contamination. The generated capacitance peak is healed with the time after remove of the bias stress as shown in Fig. 5. Figure 6 shows the time dependence of ΔC which decays roughly exponentially. The temperature dependence of the healing time constant is plotted in Fig. 7 and the activation energy of ~0.04 eV is obtained, which is about a half of the hydrogen bond energy. [6]

3.2 Model of interface traps

The proposed model for the interface traps associated with the organic contamination is shown in Fig. 8. The organic contamination may additionally supply carbon and hydrogen atoms to the interface and the structural deformation is further enhanced due to the short bond length of C-O bonds than that of Si-O bonds.[6] When electrons flow through this region, some of electron energies are transferred to the SiO_2 lattice and the defects will be generated, which act as interface traps. When the bias stress is removed, the structural defects are healed and the interface trap density is gradually reduced. One possible explanation is that the defect healing is caused by the hydrogen termination of the dangling bonds.

4. Conclusion

We have measured the influence of the organic contamination on MOS capacitors and the anomalous behaviors of the *C-V* characteristics are shown. The self-healing of the stress induced traps is analyzed and the model associated with the hydrogen bond is proposed. These results are useful for determining the acceptable organic contamination levels to the actual devices.

Reference

[1] Yoshino, *et al.*, Jpn. J. Appl. Phys. **40** (2001) 2849.
[2] Yoshino, *et al.*, Jpn. J. Appl. Phys. **41** (2002) 4750.
[3] M. Suzuki *et al.*, Jpn. J. Appl. Phys. (to be published)
[4] M. Suzuki and S. Yokoyama, Jpn. J. Appl. Phys. (to be published in 2005).
[5] S. M. Sze: *Physics of Semiconductor Devices* (Wiley, New York, 1981), 2nd ed., Chap. 1.
[6] L. Pauling, *The Nature of the Chemical bond* Chap. 12.

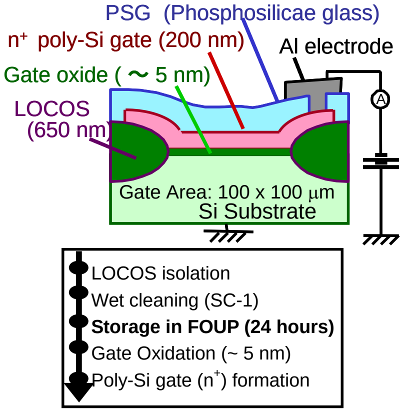


Fig. 1 Cross sectional structure and fabrication procedure for MOS capacitors.

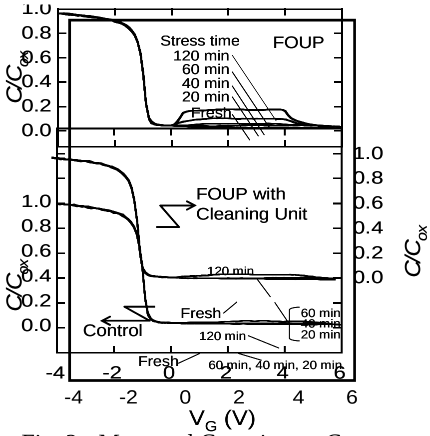


Fig. 2 Measured Capacitance C as a function of gate voltage V for samples with different contamination levels.

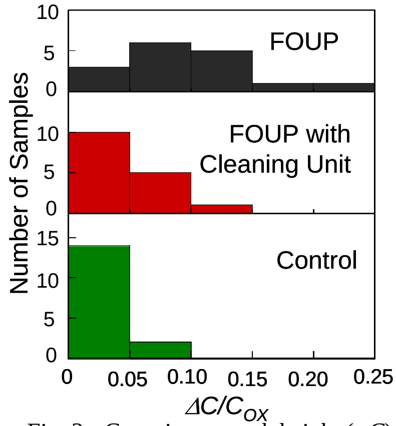


Fig. 3 Capacitance peak height (ΔC) histograms of MOS capacitors after bias stress for 1 h.

Table. 1 Quantitative organic compounds (hexadecane equivalent) adsorbed on Si wafers, fresh and stored for 6 h measured by GC/MS method. (Unit: ng/cm^2)

	Before storage	After storage
BHT	ND*	0.006
Aliphatic alcohol	ND	0.062
PGMEA	ND	ND
2-Ethyl-1-hexanol	0.039	0.029
DBP, DOP, DEP	ND	ND

*ND means "Not Detected".
BHT: di-buthylhydroxytoluene,
PGMEA: propyleneglycol monomethyl ether acetate,
DBP: dibutyl Phthalate, DOP: dioctyl phthalate
DEP: diethyl phthalate.

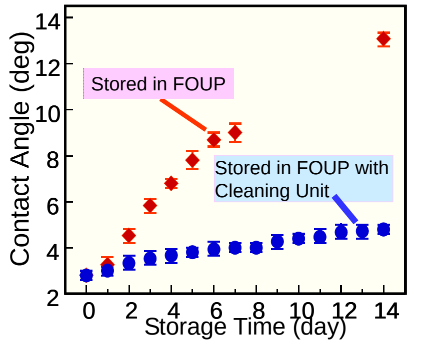


Fig. 4 Contact angle for SiO_2 surface stored in FOUP as a function of storage time.

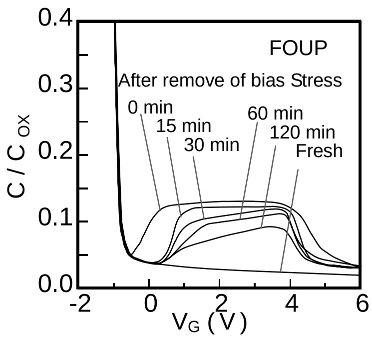


Fig. 5 Capacitance change after removing current stress.

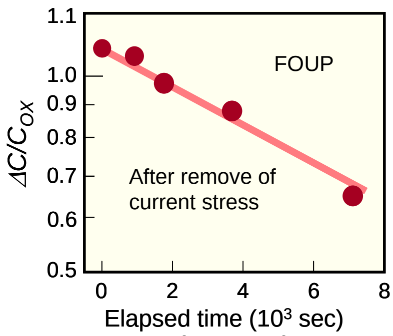


Fig. 6 D_{it} as a function of elapsed time after removing current stress for 1 hour.

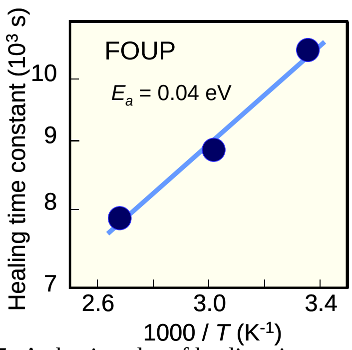
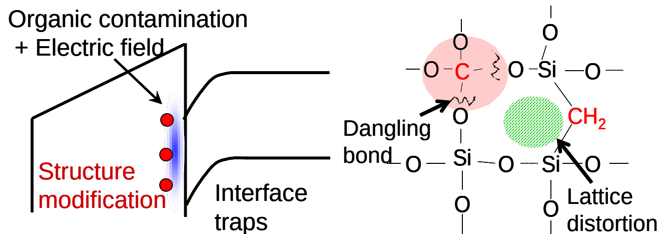


Fig. 7 Arrhenius plot of healing time constant versus reciprocal substrate temperature.



(a) Energy band diagram of MOS capacitor.

(b) Model of the defects in SiO_2 by organic contamination.

Fig. 8 Model for generation and self-healing of interface traps in organic contaminated SiO_2 film.

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Outline

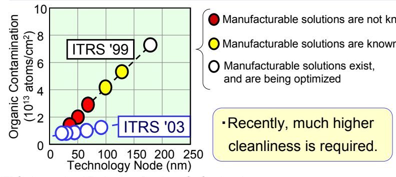
Introduction

Background

Influence of organic contamination

- Increasing in leakage current
- Reliability degradation of gate oxide
- Abnormal C-V characteristics

Maximum acceptable organic contamination on Si wafer



- Recently, much higher cleanliness is required.

ITRS : International Technology Roadmap for Semiconductors

Target

Evaluation of UV/photocatalyst cleaning method

- Contamination level control : Storage in FOUP
- Evaluation methods
  - Contact angle measurement
  - MOS Reliability : TDDB measurement

Evaluation of influence of the organic contamination to Si/SiO_2 interface

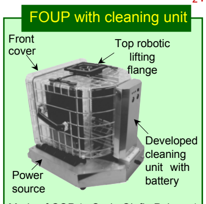
- C-V_G measurement after reverse bias stress
  - Stress time dependence
  - Elapsed time dependence after removing stress
  - Measurement temperature dependence

Model of interface traps by organic contamination

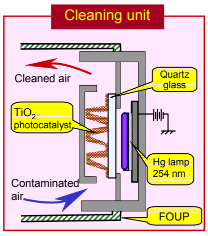
Evaluation of UV/photocatalyst method

Control Method for Organic Contamination

Utilization of UV/TiO_2 photocatalyst method



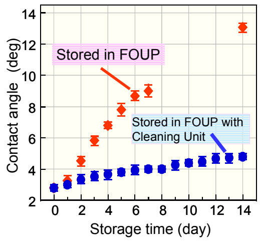
Made of COP (= Cyclo Olefin Polymer)
Store 300mm Si wafer (25 piece)

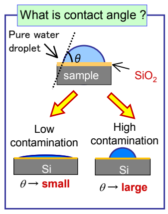


Characteristics

- Thermal convection → Fan less
- Outer light source → Contamination source is isolated

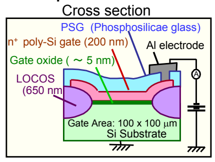
Contact Angle Measurement





Contact angle : Cleaning Unit < without Cleaning Unit

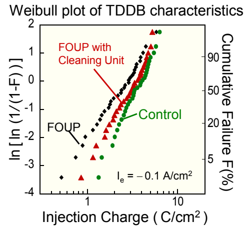
MOS Capacitor Evaluation by TDDB Measurement



Fabrication procedure

- Locos isolation
- Wet cleaning (SC-1)
- Storage in FOUP (24 h)
- Gate oxidation (~ 5 nm)
- Poly-Si(n+) formation
- Al electrode formation

TDDB measurement



Reliability

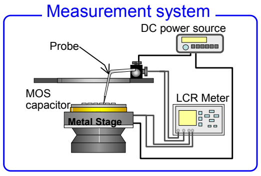
Control > FOUP with Cleaning Unit > FOUP

UV/photocatalyst method is effective to reduce organic contamination

Evaluation of stress induced interface traps

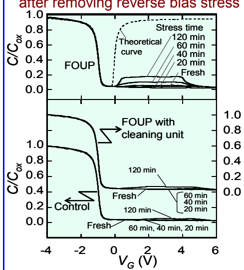
The C-V_G characteristics of MOS capacitors contaminated by organic molecules was measured.

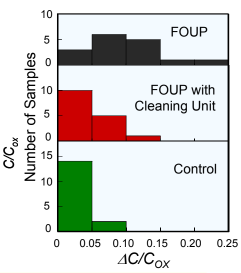
DC bias was applied to MOS capacitor before C-V_G measurement.



Stress condition
V_G = DC +10 V
Measurement frequency
1 kHz

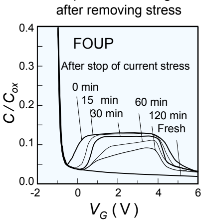
C-V_G characteristics

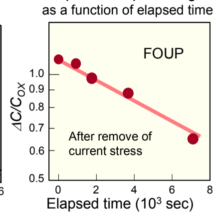


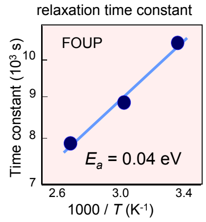


- Anomalous peaks appear in inversion region
- Organic contamination induces capacitance peaks

Self relaxation of capacitance peak







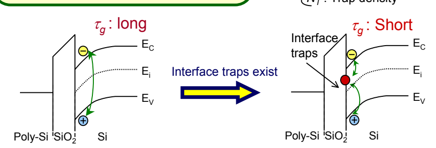
- Capacitance peak decays exponentially after removing the bias stress.
- Relaxation time constant of ΔC : ~ 10^4 sec
- At high temperatures, the time constant becomes shorter.
- Activation energy of relaxation time constant : 0.04 eV

Model of Capacitance Peak Appearance

Capacitance increase in inversion region
⬇
Short generation lifetime of minority carrier (τ_g)
⬇
Generation of interface traps

$$\tau_g \propto \frac{1}{\sigma \, v_n N_T}$$

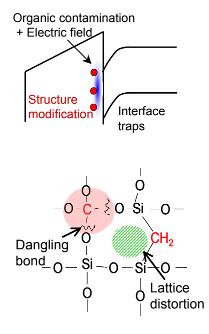
σ : Trap cross section
v_n : Thermal velocity
N_T : Trap density



- Reverse bias stress induces interface traps.
- Carrier response time decreases with interface trap density.

Model for Quenching of Interface Traps

Organic contamination + Electric field stress
↓
Lattice distortion + Dangling bonds
↓
Generation of Interface traps
↓
Self healing by thermal energy
↓
Disappearance of Interface traps



Summary

- UV/photocatalyst method is effective to reduce organic contamination.
- Organic contamination increases inversion capacitance of MOS capacitors through generation of interface traps.
- Stress induced interface traps are self-healed with activation energy of ~0.04 eV.
- Model of the self-healing mechanism is proposed.

★Future works

- application of UV/photocatalyst method to fabrication of high-κ dielectric film
- further elucidation of stress induced interface traps