Atomic-layer deposition of ultrathin gate dielectrics and Si new functional devices

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1. Introduction

Atomic-layer deposition (ALD) of ultrathin gate dielectrics are studied. ALD Si-nitride gate dielectrics, ALD Si-nitride/SiO_2 stack gate dielectrics, and ALD ZrO_2/ALD Si-nitride gate dielectrics have successfully been formed to date.

In addition, researches of new Si functional devices such as Si quantum devices or single electron transistor (SET) are carried out. Conduction mechanism of Si SETs having an one-dimensional regular array of multiple tunnel junctions are studied. Also, high temperature (Room temperature and 77K) operations of logic circuit using the SET have successfully been realized to date.

2. Atomic-layer deposition of ultrathin gate dielectrics

Low temperature growth of silicon nitride is one of the key technologies for the next generation gate dielectrics. Several methods have been proposed for such a growth. Recently, we have developed an ALD of silicon nitride [1]. The gate leakage current can be reduced due to the high dielectric constant of ALD silicon nitride [2]. Boron penetration can also be suppressed [1]. It has a superior control of film thickness and an excellent thickness uniformity especially in the thin region [1]. Also, the ALD silicon-nitride gate dielectrics have been found to be free from soft breakdown (SBD) phenomena [2,3], which are a severe problem in the progress of device scaling. The SBD free phenomena are considered to be due to a reduced interface and bulk trap generations [4].

The post-stress mobility degradation of n-MOSFETs with ALD silicon-nitride gate dielectrics has been evaluated under the electron-injection by direct tunneling [5]. Though slightly smaller electron mobility for the ALD silicon nitride than for the reference SiO_2 was obtained in the fresh samples, electron mobility degradation was substantially reduced for the ALD silicon nitride. This is also considered to be due to the reduced interface and bulk trap generations for the ALD silicon-nitride gate dielectrics.

Figure 1 shows V_{th} shift after the hot carrier injection. V_{th} shift is larger for the SiO_2 gate dielectrics than that for the silicon nitride ones at the same amount of carrier injection in the range from 10^{18} to 10^{21}electrons/cm^2 [6]. The reduced V_{th} shift for the ALD silicon nitride can be attributed to the smaller stress-induced bulk trap generations for the ALD samples than for the SiO_2 samples.

Therefore, ALD silicon nitride is a very promising candidate to replace conventional SiO_2 dielectrics for sub-100-nm technology applications.

In addition, the proposed ALD silicon-nitride dielectrics can be applied to a thin barrier layer to suppress the formation of an interfacial layer having a low dielectric constant during the growth of high-*k* gate dielectrics such as ZrO_2 [7,8] or HfO_2. ALD silicon-nitride/SiO_2 stack gate dielectrics [9-12] are also a promising application for sub-100-nm technology nodes.

3. Si new functional devices

Uniformly doped Si SETs consisting of a one-dimensional regular array of multiple tunnel junctions (MTJs) and islands (Fig. 2) have been fabricated [13]. Coulomb blockade effect (Fig. 3) is found to play an important role in carrier conduction in the MTJ system at low temperature (6K). The conduction mechanism can be interpreted well by considering soliton. The soliton extends less than three islands in our MTJs, and the energy of a single soliton is found to be 0.024 eV from an analysys of low-temperature current-voltage characteristics (Fig. 4). For high-temperature operation, it is effective to reduce the parasitic capacitance of each island, which leads to an increase in soliton length.

An exclusive-Not-OR operation (Fig.5) has been realized at 77 K using a highly-doped Si SET with MTJs and multiple side gates [14]. Using the SET with multiple gates reduces the number of required transistors for the logic circuit compared with using conventional complementary metal–oxide–semiconductor transistors. Up to date, an exclusive-OR operation has also been realized at room temperature [15]. Highly doped SETs with MTJs and multiple side gates are easy to fabricate, which should open up the development of SET logic circuits.

Acknowledgement

The author would like to thank Mr. T. Kitade, Mr. Y. Yokoyama, Mr. H. Ishii, Dr. K. Ohkura, Dr. S. Zhu, and Prof. S. Yokoyama for their help.

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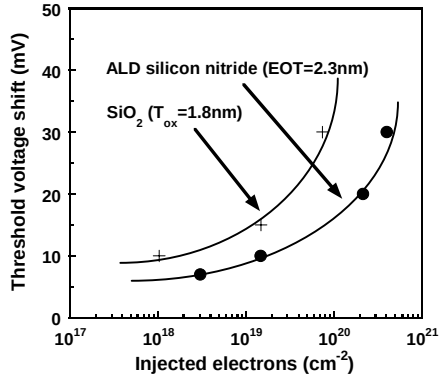

Fig.1 Threshold voltage shift of ALD silicon-nitride and SiO_2 gate dielectrics after hot carrier injection. Hot electrons were injected by satisfying the forward bias condition between an n^+-injector (V_{inj} =-2.1V) and the substrate (V_{sub} =-1.2V) for the silicon-nitride sample. For the SiO_2 sample, V_{inj} =-3.2V and V_{sub} =-2.3V was applied. The same forward bias voltage (0.9V) was applied to the n^+-injector/substrate junction for both samples.

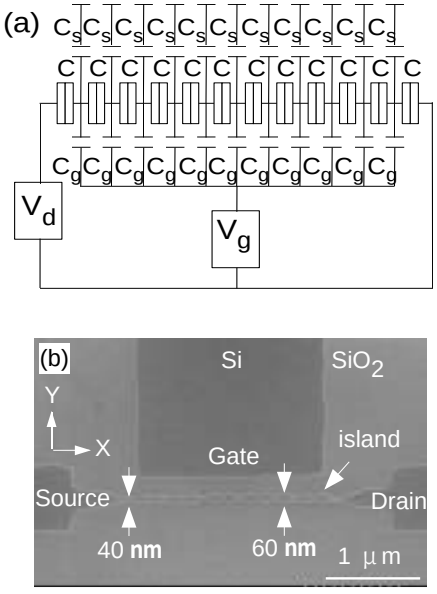

Fig. 2 (a) Equivalent circuit of a fabricated SET with MTJs consisting of 11 islands. C_s, C_g, and C represent the substrate capacitance, gate capacitance, and tunnel junction capacitance of a Coulomb island, respectively. Parasitic capacitance C_o of the island consists of C_s and C_g. (b) Plan-view scanning electron microscopy micrograph of the SET.

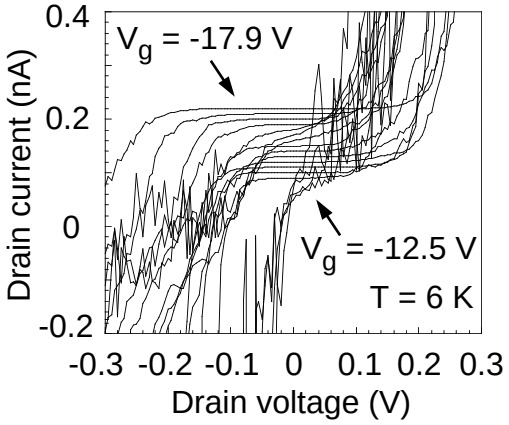

Fig. 3 Drain current vs drain voltage (I_d-V_d) characteristics as a function of gate voltage (V_g) at 6K. V_g from -17.9 to -12.5V in V_g steps of 0.3V. The curve for V_g of -13.7V is not shown due to measurement failure. Each curve is offset by 10pA per 0.3V of V_g to provide clarity.

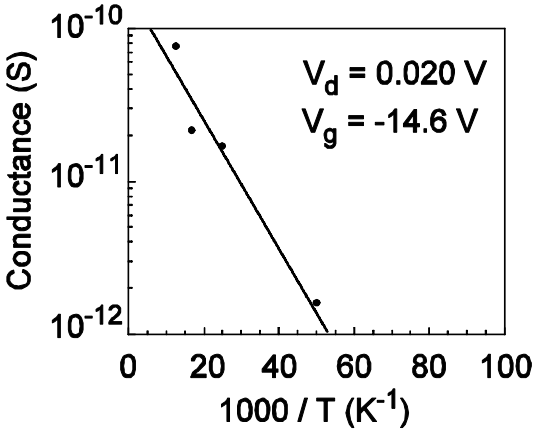

Fig. 4 Arrhenius plot of the conductance at drain voltage V_d of 0.020V. The gate voltage V_g is -14.6V.

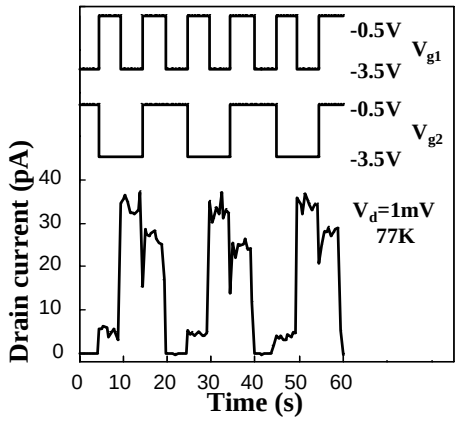

Fig. 5 Drain current switching characteristics when the input gate voltages (V_{g1} and V_{g2}) are switched between -0.5 and -3.5V at 77 K (drain voltage V_d=1 mV).

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Atomic-layer deposition of ultrathin gate dielectrics

ALD Si nitride gate dielectrics

Scaling of gate oxide thickness

Year of production	2005	2007	2009
DRAM 1/2 Pitch [nm]	80	65	50
T_{ox} [nm]	2.1	1.6	1.4

(***Low-standby-power***)

International Technology Roadmap for Semiconductors 2003

Background

- Gate leakage due to direct tunnel current
- Boron penetration in *p*-MOSFET

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- Low temperature growth of Si nitride gate dielectrics is a key for future ULSIs

Purpose

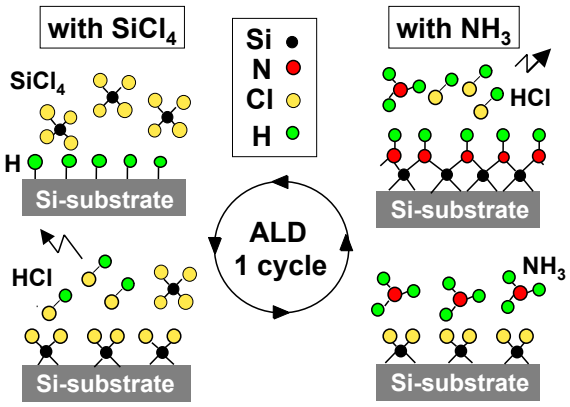
- There are several low temperature fabrication methods of Si nitride
  - Jet vapor deposition
  - Microwave-excited plasma deposition
  - Catalytic CVD
  - Atomic-layer deposition (ALD)

Clarifying advantages of ALD Si nitride gate dielectric

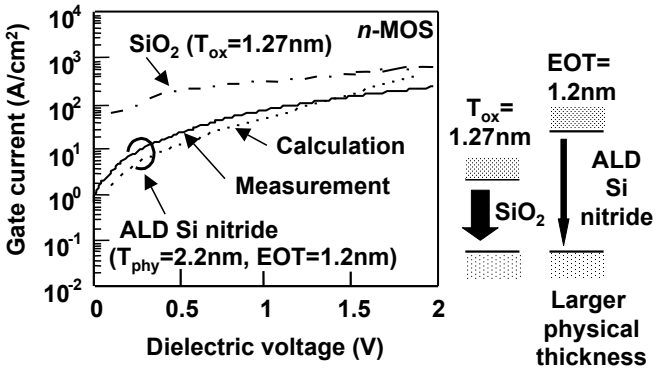
ALD Si nitride

- Alternate exposure of $SiCl_4$ and NH_3
  - Merits of self limiting property
    - Extremely flat surface in thin region
    - Excellent thickness controllability in atomic scale (≲ 2 nm)
    - Low thermal budget (≤600°C)

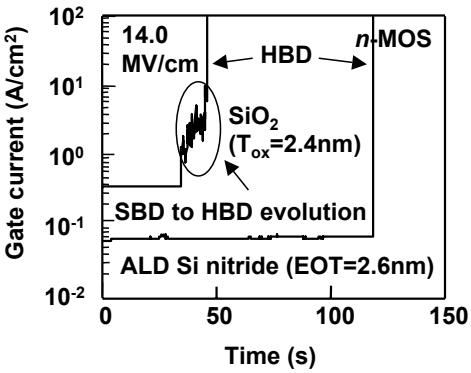
Reaction mechanism



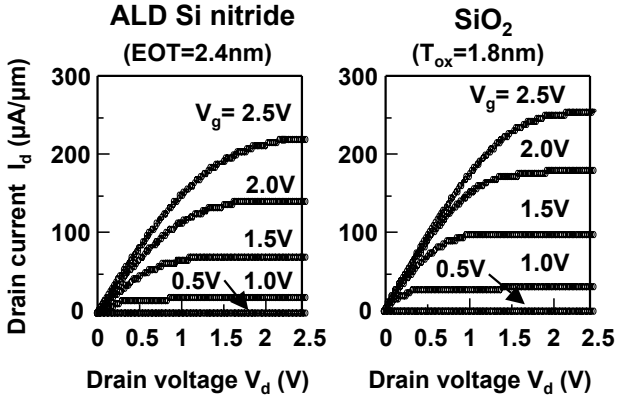
Gate leakage characteristics



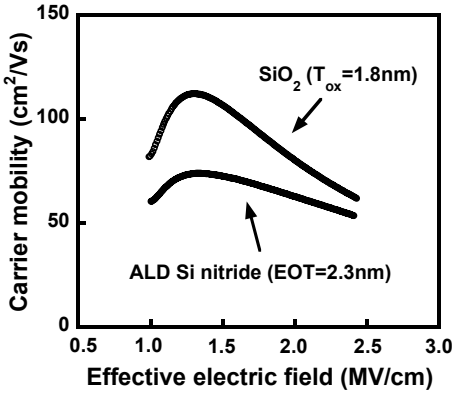
Current-time characteristics at constant dielectric field



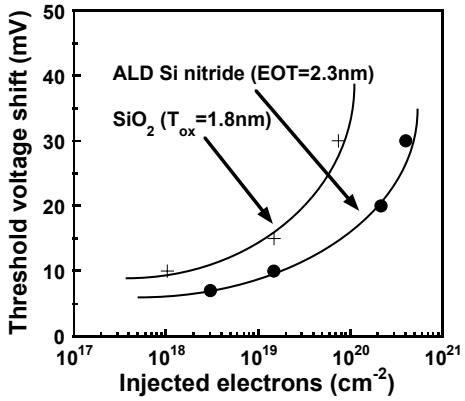
I_d-V_d characteristics of *n*-MOSFETs



Effective electron mobility



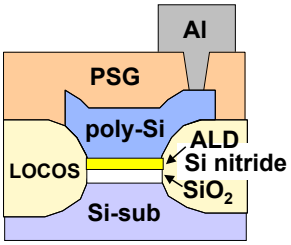
V_{th} shift after hot carrier injection



Sub-summary

- ALD Si nitride is a promising candidate for gate dielectrics of sub-100 nm technology node
  - Lower leakage current than SiO_2
  - Higher reliability in TDDB characteristics
  - Soft breakdown free
  - Lower stress-induced interface and bulk trap density
  - Slightly smaller inversion layer mobility than SiO_2
  - Reduced post-stress V_{th} degradation

ALD Si-nitride/SiO_2 stack gate dielectrics



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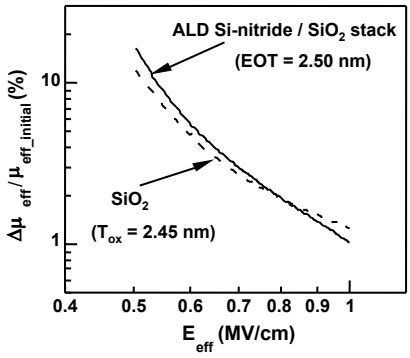
Merit of ALD Si nitride

- suppression of boron penetration into the dielectrics, which leads to the suppression of reliability degradation
- suppression of mobility degradation

Mobility reduction after hot carrier injection

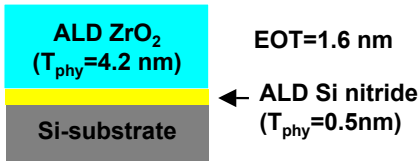


Sub-summary

ALD Si-nitride / SiO_2 stack gate dielectrics is promising for sub-100 nm technology generation

- Soft breakdown free
- Identical hole mobility to SiO_2
- Identical post-stress mobility degradation to SiO_2
- Lower leakage current than SiO_2
- Higher reliability in TDDB characteristics

ALD ZrO_2 / ALD Si-nitride stack gate dielectrics

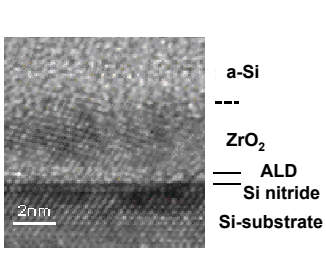


To suppress the growth of interfacial layer having low dielectric constant

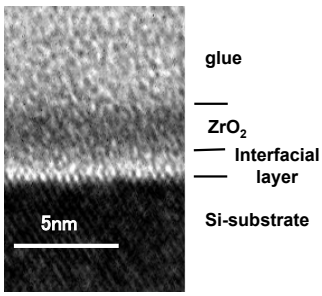
Merit of ALD Si nitride

- Extremely flat surface in thin region
- Excellent thickness controllability in thin region
  - **APL 81, 2824 (2002) Nakajima *et al.***
  - **JAP 95, 536 (2004) Ishii *et al.***

TEM cross section



ALD ZrO_2 on ALD Si nitride



ALD ZrO_2 on Si substrate

Sub-summary

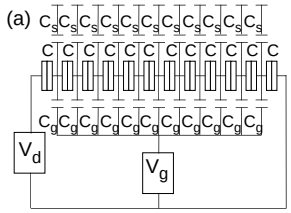
ALD Si-nitride is promising as a barrier layer of high-k gate dielectrics

- Suppression of formation of SiO_x interfacial layer having low dielectric constant
- Reduced leakage current by about one order of magnitude compared with ZrO_2
- ZrO_2 / Si-nitride stack gate dielectrics can be fabricated using all ALD processes

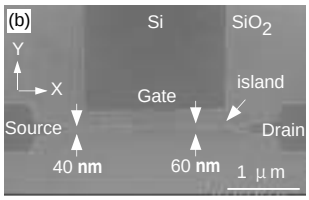
Si new functional devices

- Si single-electron transistor with a one-dimensional regular array
- Logic circuit application

Si single-electron transistor with a one-dimensional regular array

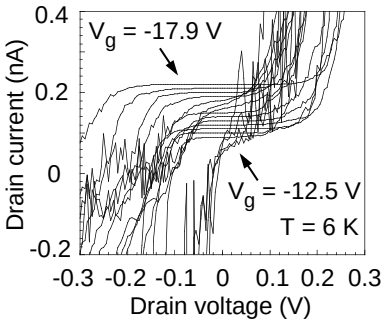


Equivalent circuit

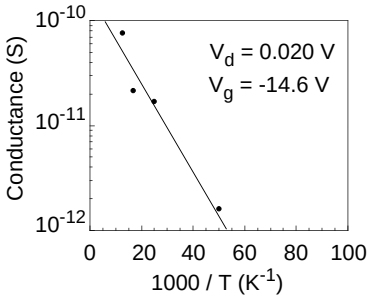


Plan-view SEM micrograph

I_d-V_d characteristics



Arrhenius plot of conductance



Δ=0.01eV

↓

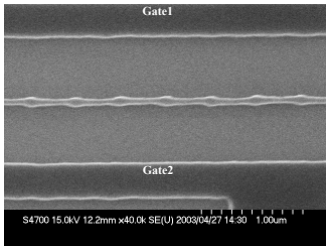
E_s=0.02eV

Sub-summary

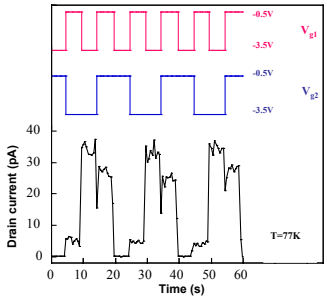
- Uniformly doped Si SETs consisting of a one-dimensional regular array of multiple tunnel junctions and islands have been fabricated.
- Coulomb blockade effect is found to play an important role in the carrier conduction.
- The conduction mechanism can well be interpreted by considering soliton with soliton energy of about 0.02 eV and soliton length of about three islands.

Logic circuit application

- SET with double side gates and with an array of nanoscale islands



Exclusive-NOR operation at 77K



Sub-summary

- Logic circuit operation has been realized using an uniformly doped Si SET with multiple gates and multiple tunnel junctions.
- An exclusive-Not-OR operation has been realized at 77K using the SET.
- The number of required transistors is reduced compared with the case using CMOS transistors.

Conclusion

- Atomic layer deposition is a key technology for gate dielectrics of sub-100 nm technology node.
- Highly doped SET with multiple tunnel junctions and islands are useful for realizing Si new functional devices.

Acknowledgement

- The author would like to thank Mr. Kitade, Mr. Y. Yokoyama, Mr. H. Ishii, Dr. K. Ohkura, Dr. S. Zhu, and Prof. S. Yokoyama for their help.