Preface

On behalf of Hiroshima University 21st century COE program committee on “Nanoelectronics for Tera-Bit Information Processing”, I would like to welcome you to the Fourth Hiroshima International Workshop on Nanoelectronics for Tera-bit Information Processing.

Within the COE program “Nanoelectronics for Tera-bit Information Processing”, the scientific staff of Research Center for Nanodevices and Systems (RCNS) and members of the Graduate School of Advanced Sciences of Matter (ADSM), Hiroshima University are working on an extension of their world-class research position, and on the formation of the COE for innovative research and education in information electronics. This COE program aims at the fusion of silicon-based nanodevices, circuits, and integrated circuit-architectures. Silicon technology has emerged over the last decade as the predominant technology of the industry. The concept of MOS device scaling has consistently applied over many technology generations, resulting in the nanometer regime. This nanotechnology leads to develop the high speed computer, communication network, robots, medical diagnosis technique, etc.

Our main goals are as follows.

- Unification of researches in (1) architecture and system/circuit design, (2) device-modeling and (3) device fabrication and integration technologies.
- Solutions for three-dimensional-integration utilizing wireless- and optical-interconnections, and implementation of 3D integration prototype systems with high-level recognition and learning capabilities
- Development of device technologies for high performance ultra-small transistors as well as wireless- and optical-interconnects and nanometer Si quantum dots.

The cooperative research aiming at the fusion of research fields has started. The research for combining high frequency MOS device modeling and RF circuit design, the research on electromagnetic wave transmission and devices structure has progressed substantially. We have already proposed a three dimensional integration technology utilizing wireless communication and applied a basic patent. The research at the system level such as the image recognition processing using associative memory or bio-inspired information processing utilizing wireless interconnection has also started. In addition, the research on new 3D MOS devices, memory devices using quantum dots, and light resonance devices have substantially progressed.

The first workshop was held on March 17, 2003. The second workshop was held on January 30, 2004, in which modeling and simulation tasks of the COE were focused. The third workshop was held on December 6, 2004 focusing on wireless interconnection in ULSI. The fourth workshop focuses on ultra small devices and process technologies.

Besides focusing of the COE achievement, five distinguished researchers from abroad and two domestic researchers are invited and will review the state of the art technologies.

I hope the Fourth Hiroshima International Workshop on Nanoelectronics for Tera-Bit Information Processing will be a fruitful one for all attendees.

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