Recent Progress of the COE

Atsushi Iwata
Graduate School of Advanced Sciences of Matter,
Research Center for Nanodevices and Systems, Hiroshima University
1-3-1, Kagamiyama, Higashi-Hiroshima, JAPAN 8739-8526, iwa@dsl.hiroshima-u.ac.jp

1. Target of the COE

The features of the COE on "Nano-electronics for Tera-bit Information Processing" are to fuse the 3 research fields of (1) circuit design and system architecture, (2) device molding, and (3) nano-devices and processing. Research efforts cover next generation nanodevice technologies collaborated with device modeling, high performance circuit design and architecture for high performance system. Our targets are to realize three dimensional integration utilizing inter-chip wireless interconnects and on-chip optical interconnects, (Fig.1) and to demonstrate its feasibility by implementing multi- and moving-object recognition systems for hyper robot brains.

2. Research Fields and Subjects

Device modeling is a key to organize research collaboration between the field of circuit/system and device/process. RF circuit design utilizing the advanced device model realizes the wireless interconnects with low power dissipation. In the device field, for realizing tera-bit processing, new MOS devices, RF transceiver with integrated antennas, and integrated optical components has been studied. Research on multi-layered Si quantum dot structure will results in new optical sensor and memory devices. Synthesizing these bases, we are aiming innovative 3D integration technologies and system applications.

4. Major Achievements

4.1 MOSFET Model:

HiSIM model has been developed for ultimately scaled MOSFETs. Its concept is to describe devices utilizing surface potential, based on physical principles of drift and diffusion. *HiSIM2-NQS* including Non-Quasi-Static effects realizes sufficient accuracy in GHz and Gbit/s circuit operation. (Fig. 2) The Compact Model Council selected *HiSIM* as the final stage candidate for the standard model with *PSP* model proposed by Penn. State University and Philips in March, 2005. The HiSIM Research Center has been established in Hiroshima University in June, 2005, and now supporting the final evaluation by affiliations over the world for standardizing at the end of 2005. Moreover, the new techniques have been investigated for modeling of sensitivity to photons and electromagnetic wave.

4.2 Wireless Interconnection

[Wireless interconnects using on-chip antennas]

A new inter-chip and intra-chip connection technique using radio wave propagation using on-chip dipole antennas was proposed. We have confirmed by measurements that antenna transmission gain is about -28dB at 20GHz, and it decreases 0.14dB/chip with 270μm chip thickness. (Fig.3) UWB transmitter and receiver chips have designed with a 0.18μm CMOS. By measurement of the test chips, generation and receiving of UWB pulse were confirmed. We call this technique Global Wireless Interconnection (***GWI***) which is applicable to clock distribution and wide bandwidth busses.

Received UWB signal was interfered by DC noise as well as distorted rectangular wave noise. Differential mode operation could eliminate the digital noise in the lower frequency range. However, digital noises with the spectrum above 5GHz could not be removed. High pass filter above 5.1 GHz could suppress the digital noise interference and recover the UWB signal. Bit error rate (BER) was degraded by increasing noise voltage, but improved by increasing the resistivity of the Si substrate. BER of the antenna with 4 mm long was the lowest because the transmission loss of interference signal became maximum. (Fig.4)

[Wireless interconnects using on-chip spiral inductors]

Wireless interconnection using on-chip spiral inductor pair was proposed for inter-stacked chip connection. Resonation phenomena of inductor pair are utilized for reducing dissipation power and increasing bit rate with a simple transmitter and receiver. (Fig.5). In order to replace via-holes used in 3D stacked chips, an asynchronous scheme is necessary as well as a source synchronous system. The asynchronous scheme was realized with double pulse coding and a self-biased detector.

We have designed and fabricated a test chip with 12 channels using 0.18μmCMOS. Power dissipation was reduced to 0.95mW per 1Gps. Bit error rate of 10^{-10} was attained with relaxed alignment of 20μm (Fig.6)[2]

The inductive coupled interconnection is applicable to parallel data transfer at arbitral points of chip. We call it Local Wireless Interconnection (***LWI***).

4.3 Concept of 3D integration using wireless technologies

3D integration using *GWI* and *LWI* called 3-dimensional custom stack system (***3DCSS***) was proposed.[1] Alignment accuracy of stacked chips is relaxed as low as about a half of the inductor size. The distinguished feature of *3DCSS* is to implement a customized system composed of various kinds of chips with multi functions and devices, with an on-chip standard wireless interconnect interface. Yield and Known Good Die (KGD) problems are also resolved by chip testing using wireless pads.

In order to verify inter-chip data transfer concept of 3DCSS, an experimental setup which consists of LWI test

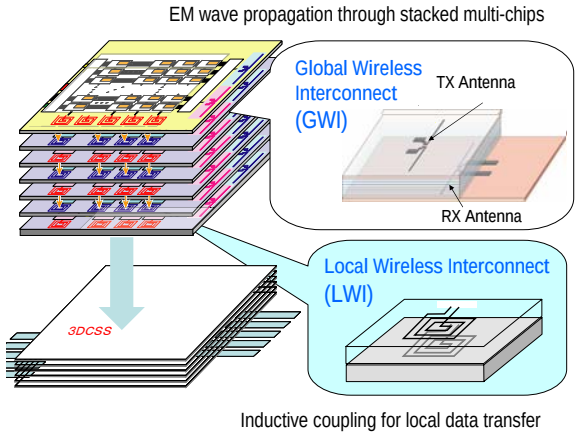


Fig. 1 3-dimentional Custom Stack System (3DCSS) utilizing Wireless Interconnections

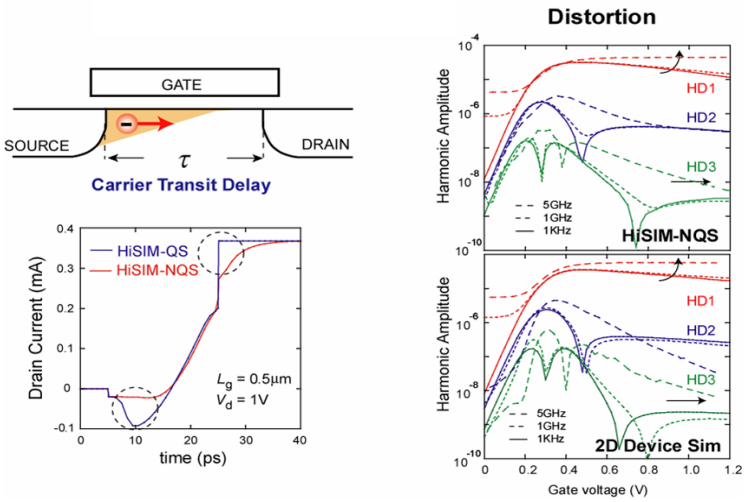
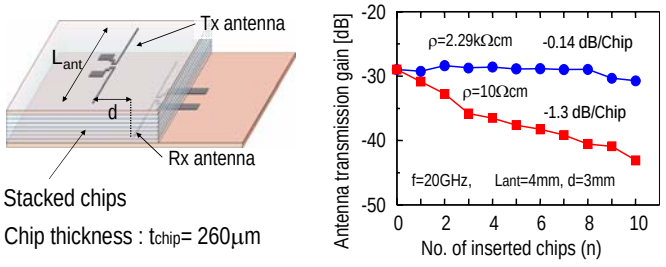
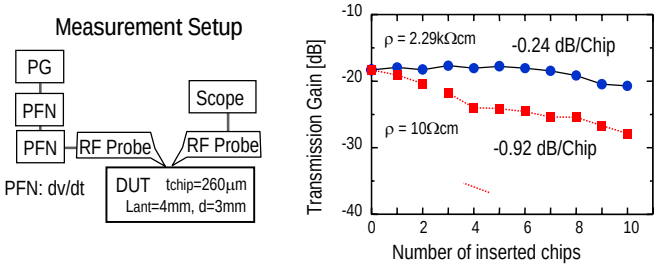


Fig. 2 MOS device Model (HiSIM2-NQS)



(b) Transmission of Sinusoidal waves



(b) Transmission of Gaussian Monocycle Pulses

Fig. 3 Radio Wave Transmission through Si Chips
Measured Transmission Loss using on-chip antennas

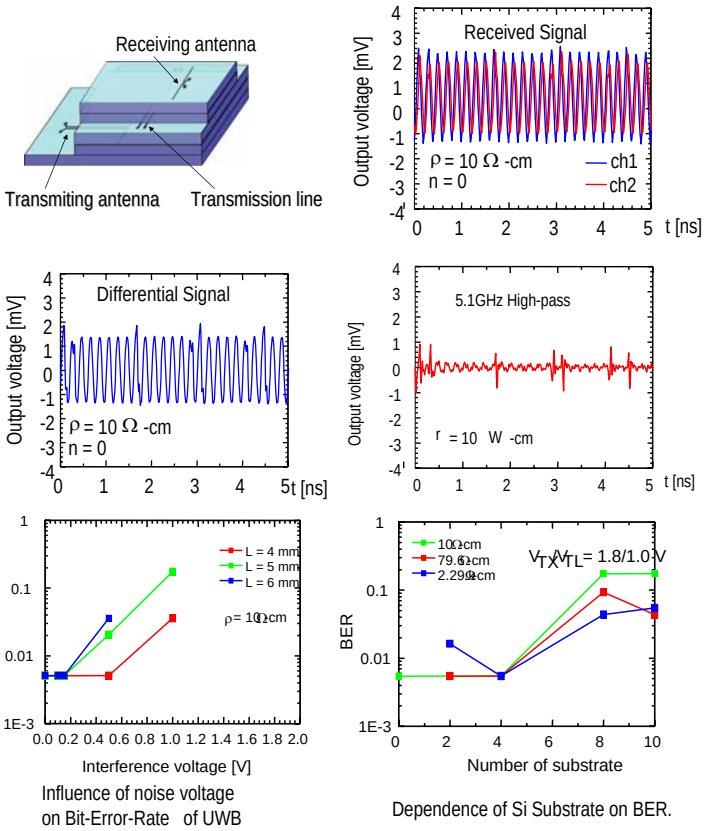


Fig.4 UWB Signal Interference for Inter-Chip Signal Transmission

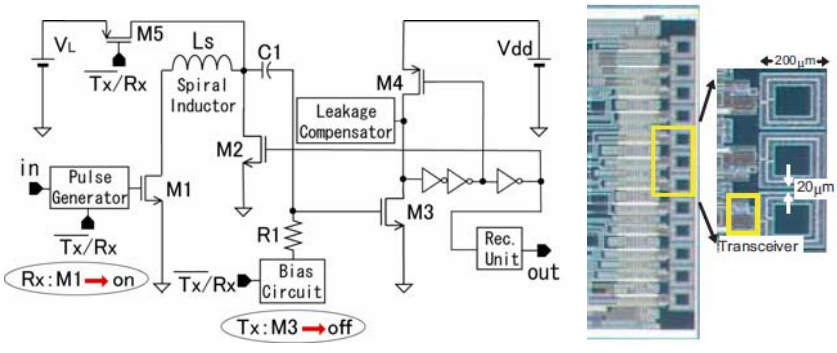


Fig. 5 LWI Transceiver and its test chip

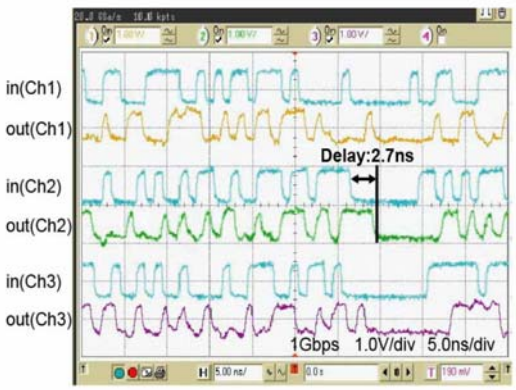


Fig. 6 Measured waveforms of LWI test chip

chips and vision chips was made. A multi-chip vision (MCV) based on hierarchical biological processing with a PWM-based line parallel I/O interface are implemented with a 0.35μm CMOS technology which consist of neurons, a resistive network for horizontal connection. Two chips, MCV1 and MCV2 are connected by two LWI chips, TX-LWI and RX-LWI using analog PWM signaling (Fig. 7). P_{1o} and P_{2i} are the PWM output of MCV1 and the PWM input of MCV 2, respectively.

4.4 Associative memory integrating learning capability

A system concept which realizes high-speed pattern matching and automatic pattern learning has been developed on the basis of an associative memory (AM) with short-term and long-term storage regions. The applied learning algorithm (Fig. 8(a)) uses a 4-step process for each learning cycle. An LSI architecture is proposed, which implements the algorithm with a fully-parallel AM, a reference-pattern-learning block and a reference-pattern-optimization block. A CMOS test-chip, which verifies the architecture for an storage capacity of 64 pattern and Manhattan-distance search, has been designed. (Fig. 8(b)).

4.5 Architecture and Implementation of 3DCSS proto type brain system

For implementing the hyper brain with real-time/ and high-level object recognition, a concept of multi-object recognition system using *3DCSS* has been studied. A higher resolution of pixels and customized functions are realized by 3DCSS. We have adopted the Principal Component Analysis and the Eigen face method for realizing multi-object detection in a natural scene and recognition under significant image variations. It is composed of wireless interconnected multi chips, early vision processor, object detector, objects recognizer and reference database composed of AM (Fig. 9). The expected performance of the system is 10 flame/s flame rate, 10 objects and 1000 data/object matching.

4.5 New MOS devices and process technologies

[Work function tuning technology]

NiSi FUSI (fully silicided) gate is one of the most promising candidate for a metal gate material that replaces current dual-gate poly-Si structure to remove performance penalty due to a gate depletion effect in poly-Si gate. To realize dual metal gate structure workfunction tuning must be developed. We have evaluated NiSi workfunction shift using the Sb pre-doping. As indicated in C-V characteristics of MOS diodes, flat band voltage shift was increased by reducing silicidation temperature. Sb atoms doped to poly-Si were swept out toward remained poly-Si during silicidation. (Fig.10(a))

[Atomic-layer deposition of gate dielectrics]

Atomic-layer-deposited (ALD) Si-nitride/SiO_2 stack gate dielectrics were applied to transistors for future scaled DRAMs. The stack gate dielectrics of the peripheral PMOS transistors excellently suppress boron penetration. It exhibits only slightly worse negative-bias temperature instability (NBTI) characteristics than pure gate oxide (Fig.10(b)). Enhanced reliability in NBTI was achieved compared with that of plasma-nitrided gate SiO_2. NBTI of p-MOS with ultrathin SiON gate dielectric has also been investigated. The NBT-induced interface trap density (ΔN_{it}) under bipolar pulsed bias of frequency larger than about 10 kHz is significantly enhanced and exhibits a strong frequency dependence. The enhancement was found to be mainly governed by the fall time (t_F) of the pulse waveform.

4.5 Integrated Optical devices

In order to overcome the speed limit of the wire interconnection, we are studying compact ring-resonator optical switches using electro-optic (EO) material, which can be monolithically integrated in LSI. We have fabricated Mach Zehnder (MZ) interferometer optical switch as shown in Fig.11, by using poly-crystal (Ba,Sr)TiO_3 film. And we have, for the first time, succeeded in observing the optical modulation in BST MZ modulator. The electro-optic constant calculated from the modulation efficiency is γ=0.45 pm/V which is about 1/100 of the single crystal $LiNbO_3$. Although the modulation efficiency observed in this study is very small, it is meaningful that the operation of the optical modulation using monolithically integrated device is demonstrated. (Fig. 11)

4.6 Charging state of Si quantum dots

To realize multi-valued charge storage using nanometer Si dots, the precise control of electronic charged states of Si dots is one of major concerns. In that regards, we fabricated Si dots on ultra-thin oxide in a self-assembled manner by controlling the early stages of low pressure CVD. And the charge storage in nanometer Si dots has been studied. The surface potential changes were measured by an AFM/Kelvin probe technique. After electron injection and emission, unique surface potential images are observable. They indicate Coulomb repulsion among retained carriers in the dot. Such a torus-shaped potential image is smeared out with time as a result of progressive electron tunneling to the substrate, and almost completely disappeared in 90 min after the electron injection. (Fig.12)

5. Conclusions

Fusing the research fields, interdisciplinary fields were formed, and innovative 3D integration technology utilizing wireless interconnections and related device and modeling techniques have been proposed. 3DCSS vision chip was designed and prototype systems are now under development.

Reference

[1] A. Iwata, M. Sasaki, T. Kikkawa, et. al., A 3D Integration Scheme utilizing Wireless Interconnections for Implementing Hyper Brains, ISSCC2005 Dig. of Tech. Papers, pp.262-263, 2005.

[2] M. Sasaki and A. Iwata, A 0.95mW/1.0Gbps Spiral Inductor Based Wireless Chip-Interconnection with Asynchronous Communication Scheme, Symposium on VLSI Circuits, 22-3, 2005.

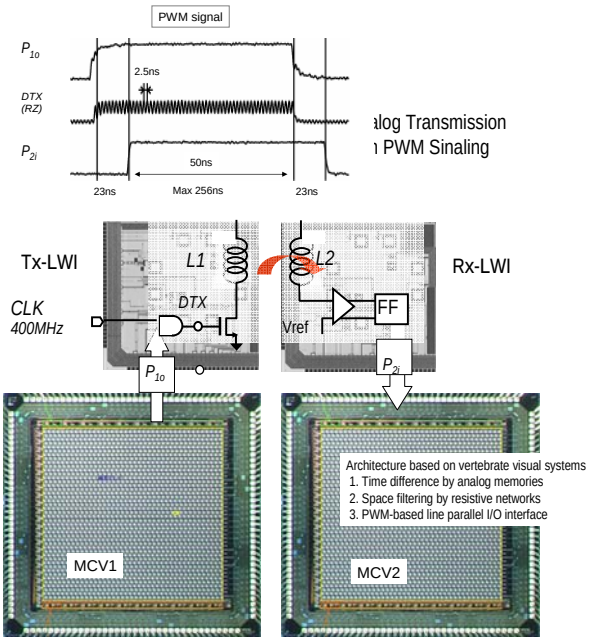
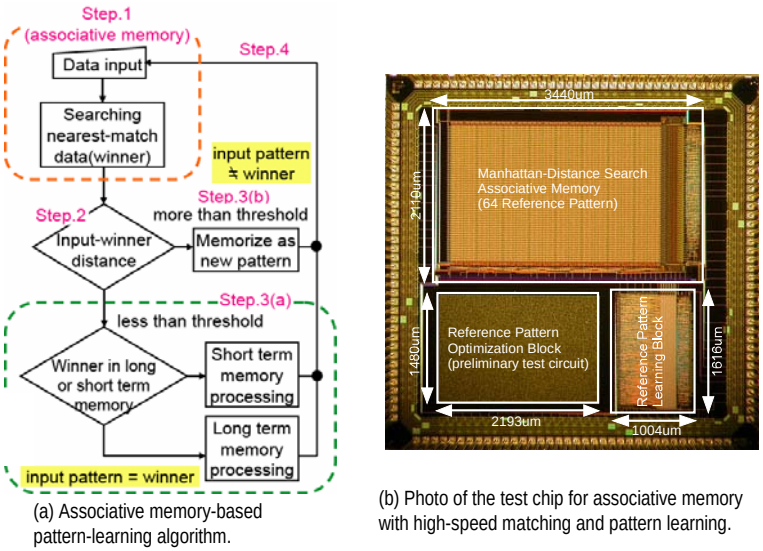


Fig.7 Measurements of Multi-Chip Vision with LWI



(a) Associative memory-based pattern-learning algorithm.

(b) Photo of the test chip for associative memory with high-speed matching and pattern learning.

Fig.8 Automatic Associative Memory based Reference Pattern Learning and Optimization

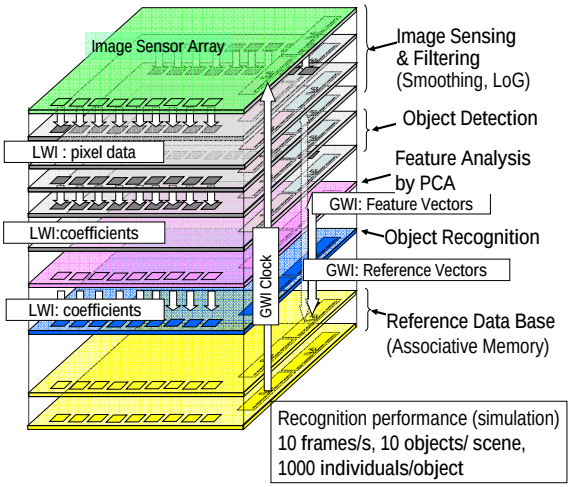
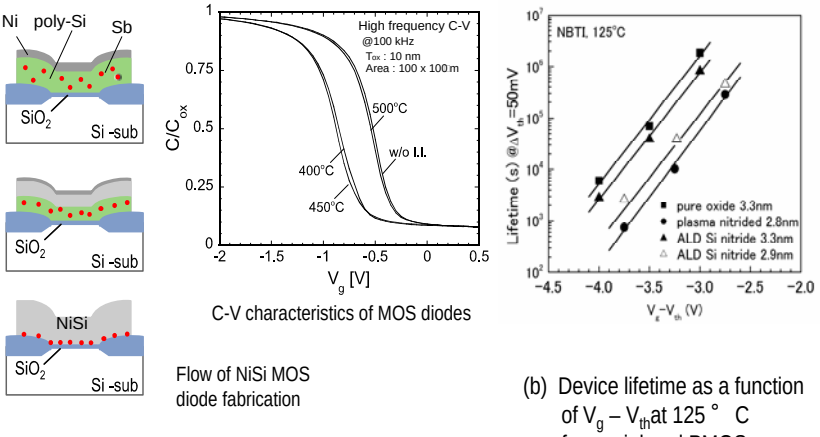


Fig.9 Architecture of Multi-object Recognition System



Flow of NiSi MOS diode fabrication

C-V characteristics of MOS diodes

(a) Workfunction Tuning of NiSi Gate with Sb

(b) Device lifetime as a function of $V_g - V_{th}$ at 125 ° C for peripheral PMOS.

Fig.10 Ultra-small MOS Device Technologies

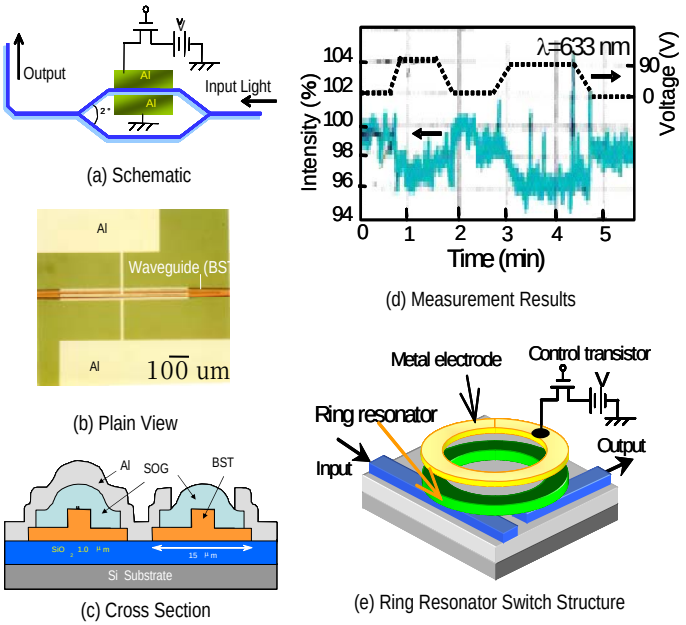


Fig. 11 Succeed in Operation of Mach Zehnder Optical Switch using $(Ba,Sr)TiO_3$ Film Monolithically Integrated on Si

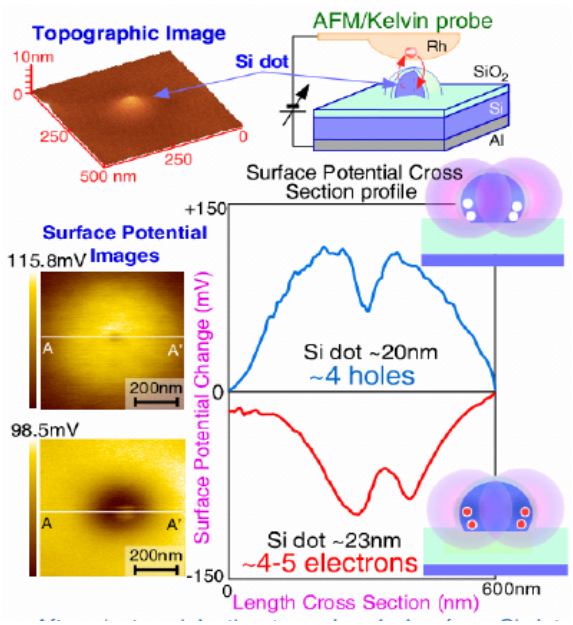


Fig. 12 Evaluation of Charge and Discharge state of Single Si Dot

21st Century COE, Hiroshima University
Nanoelectronics for
Tera-bit Information Processing

Recent Progress of the COE

Wireless Interconnects and Nanodevices for 3D Integration

Atsushi Iwata, COE Leader

Concept and Target of the COE

Concept

Fusion of the 3 research fields of
(1) circuit design and system architecture,
(2) device modeling, (3) nanodevices and processing.

Targets

(1) 3D integration utilizing Wireless Interconnects, and nanodevice integration techniques
(2) Demonstrate its advantages by implementing prototype hyper brains.

Target of education

To bring up highly-capable human resources who become leaders in microelectronics Society.

Three Core Research Fields and Members

I. Circuit and System Architecture

1. RF analog circuits (Prof. Iwata, Prof. Sasaki, Dr.Yoshida)
2. Associative-memory based systems (Prof. Mattausch Prof. Koide)
3. Processing system with highly cognitive level (Prof. Iwata)

II. Device Modeling

1. Integration of electron and optical devices
2. Three Dimensional SOI-MOS device (Prof. Miura, Prof . Esaki, Prof. Mattaush)

III. Nanodevice and Process

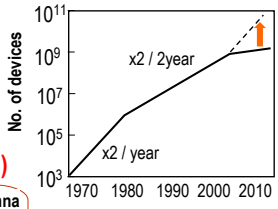
1. Fundamental device scaling techniques (Prof. Shibahara, Prof. Nakajima Prof. Miyazaki)
2. Ultra-small SOI-MOS devices (Prof. Sunami, Prof. Miura)
3. Functional nano-devices (Prof. Miyazaki, Prof. Higashi, Dr. Murakami)
4. Wireless interconnection (Prof. Kikkawa, Prof. Sasaki)
5. Optical interconnection (Prof. Yokoyama)

HiSIM Research Center
started in May 2005
for next generation international standard of MOS device

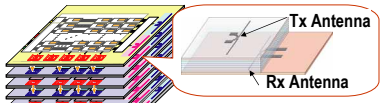
10 PD researchers and 16 doctoral students in 2005.

3D Integration using Wireless Interconnects

To overcome the Moore's law by utilizing 3D integration, **new chip inter connection** is required.

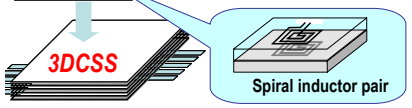


Global Wireless Interconnect (GWI)



EM wave propagation through stacked multi-chips

Local Wireless Interconnect (LWI)

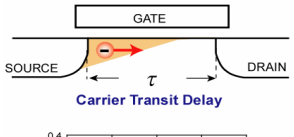


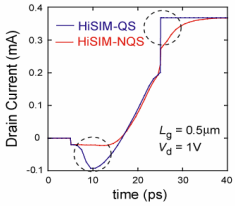
Inductive coupling between adjacent chips for local data transfer

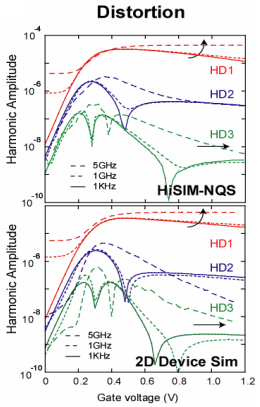
Presented in ISSCC2005

RF MOS device Model: HISIM2-NQS

Final Candidate for International Standard model in CMC





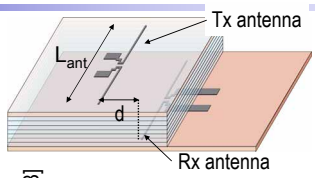


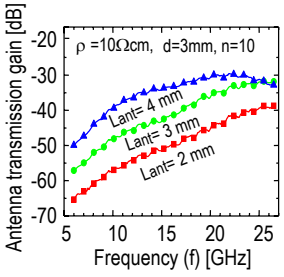
EM Wave Transmission using on-chip Antennas

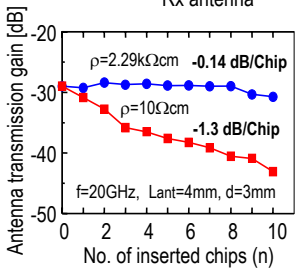
Inter-chip Transmission

Chip thickness : t_{chip}= 260μm

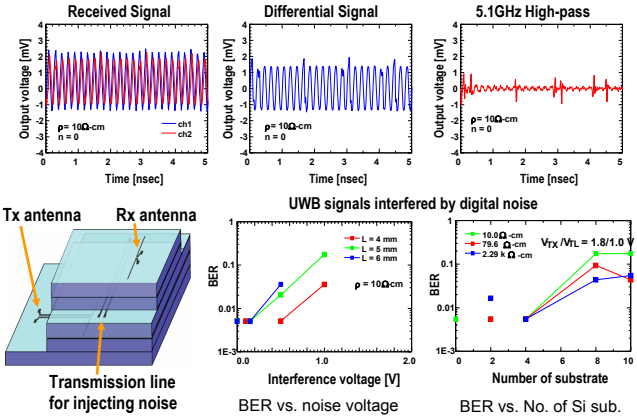
Stacked chips







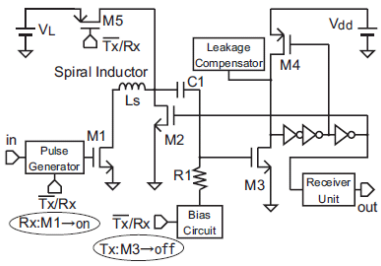
UWB Signal Interference for GWI



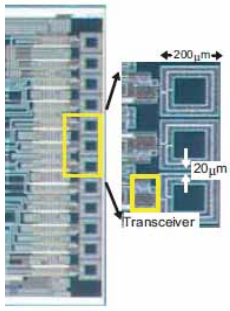
BER vs. noise voltage

BER vs. No. of Si sub.

Inductor Couple Transceiver for LWI



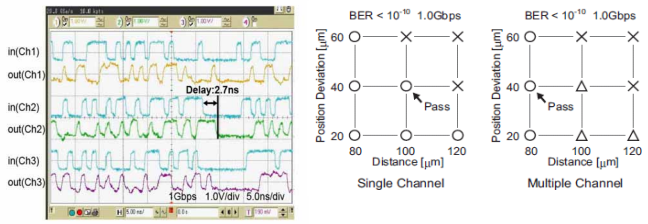
Utilizing LC resonance, a high receive voltage is obtained with a low drive current.



Transceiver Chip
0.18um CMOS
4 layer spiral Inductor

M.Sasaki, Presented in 2005 VLSI Sympo. on Circuits

1Gbps Asynchronous Transmission of LWI



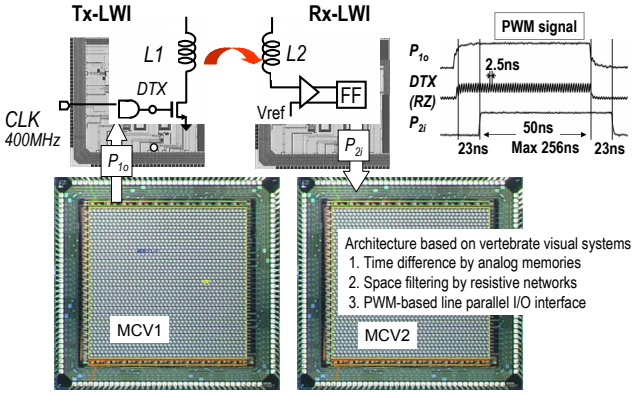
Measured Waveforms of LWI test chip

Alignment Tolerance: 20um
Bit Error Rate : 10^{-10}

Power dissipation of 1mW @ 1Gbps is obtained.
Asynchronous data transfer is available.

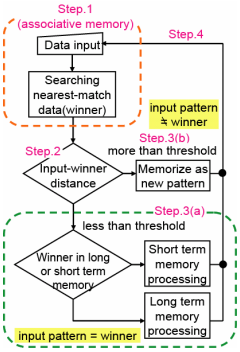
Measurements of Multi-Chip Vision with LWI

Analog Transmission with PWM Signaling

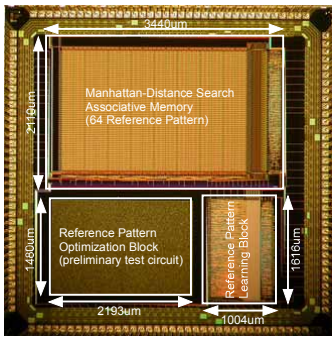


Architecture based on vertebrate visual systems
1. Time difference by analog memories
2. Space filtering by resistive networks
3. PWM-based line parallel I/O interface

Automatic Associative Memory based Reference-Pattern Learning and Optimization

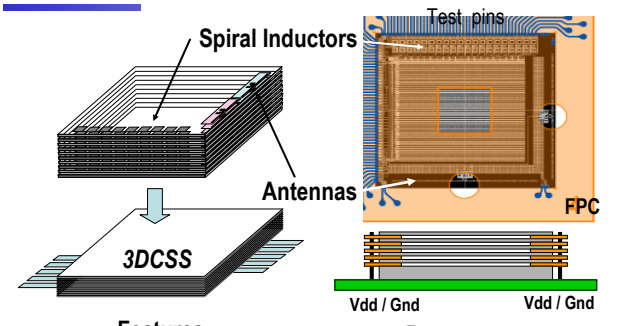


(a) Associative memory-based pattern-learning algorithm.



(b) Test chip for associative memory with high-speed matching and pattern learning.

Vision Chip with LWI and GWI and 3DCSS Prototype



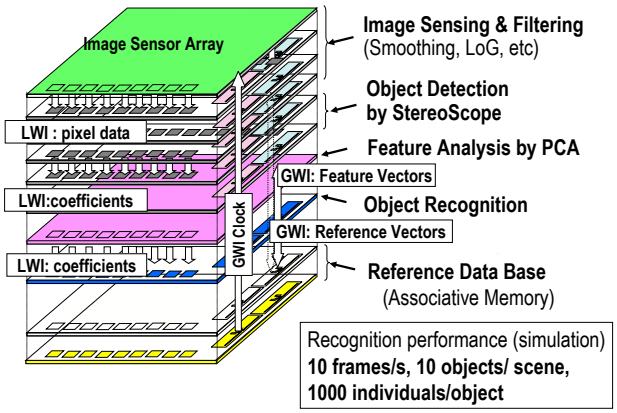
Features

1. Improve Reliability and Yield
2. Resolve problems in KGD and heat radiation

Parameters

Lant= 2-4 mm, Lind= 50 - 200μm
No. of Chips= 10-100
t_{chip}= 50 -100μm

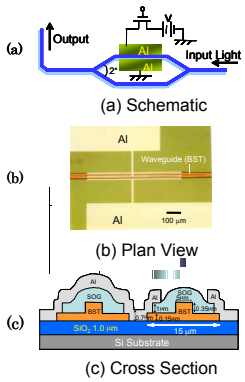
Architecture of Multi-object Recognition System

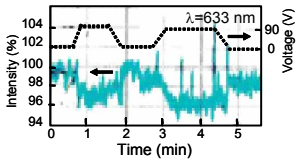


Process technologies for scaled MOS devices

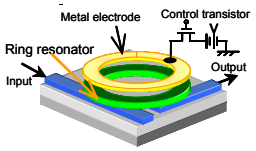
1. **High-k gate dielectrics formation**
   by **Atomic Layer Deposition (ALD)**
   - Si-nitride/SiO2 stack gate dielectrics for future scaled DRAMs.
   - Enhanced reliability in NBTI was achieved.
2. **Work function tuning for NiSi Gate MOS FETs**
   - NiSi workfunction tuning method by Sb pre-doping to poly-Si before silicidation
3. **Three-Dimensional MOS Devices**
   - **Beam Channel Transistor**
     with high current driving capability
     aiming at applications to power control with small chip area.
4. **Functional Low-k materials for on-chip wiring**.

Succeed in Operation of Mach Zehnder Optical Switch using $(Ba,Sr)TiO_3$ Film Monolithically Integrated on Si

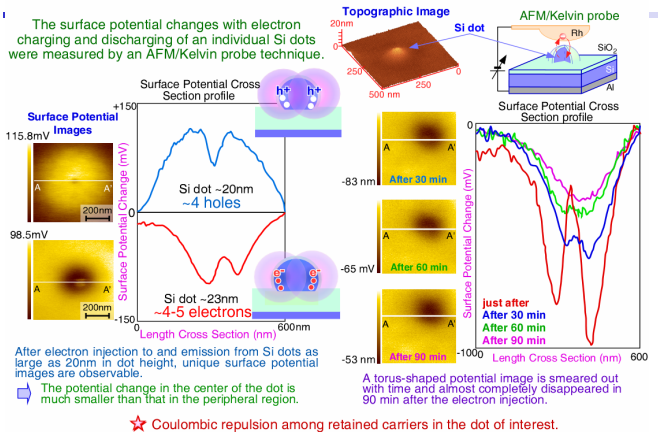




This result (operation of MZ switch) is promising for the following ring resonator switch.



Evaluation of Charged & Discharged States of Single Si Dot



Conclusions

1. **Fusing the research areas, innovative ideas and technologies for tera-bit information processing have been proposed.**

   The key idea : Combination of Nanoelectronics and Communication

2. ***3DCSS:* 3D integration system utilizing Wireless interconnects was proposed, and 3DCSS vision prototype was designed toward hyper brains.**

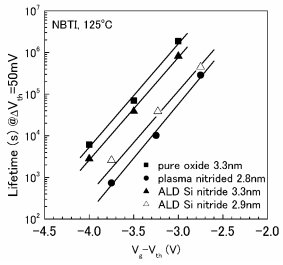


Fig. 1. Device lifetime as a function of $V_g - V_{th}$ at 125 ° C for peripheral PMOS transistors with L/W=2μm/10μm.

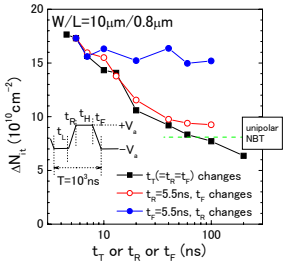
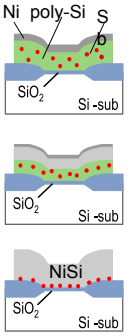


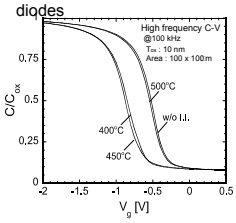
Fig. 2. Interface trap generation ΔN_{it} as a function of t_R (or t_F) under bipolar stresses at 10^6 Hz with a trapezoidal waveform. Inset shows a schematic waveform to define t_L, t_R, t_H and t_F. Devices have size of W/L= 10μm/0.8μm and are stressed at 125°C for 10^3s. For comparison, ΔN_{it} under unipolar stress with a square waveform (t_T = t_R = t_F = 4.5 ns) is also shown.

Workfunction Tuning of NiSi Gate with Sb

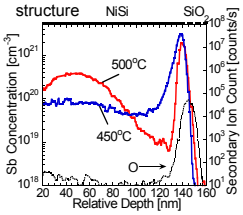
Flow of NiSi MOS diode fabrication



C-V characteristics of MOS diodes

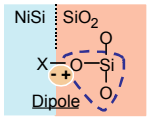


Sb profiles in NiSi MOS structure



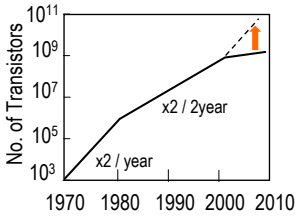
NiSi workfunction can be modified by Sb pre-doping to poly-Si before silicidation. Reducing silicidation temperature and slicidation rate was effective to obtain larger flat-band voltage shift. Increase in Sb concentration by slow slicidation was a key to increase the shift

A model of workfunction shift



Motivation to develop Advanced Integration

To overcome the Moore's law by utilizing 3D integration, **an inter-chip connection** is required.



Wireless inter-chip connects (reported)

	L,C distance	Stacked multi-chips	Power dissipation
C coupling on-chip pads	1-2μm Insulator thick.	Not applicable Via holes needed	>1mW /connect
L coupling on-chip inductors	50-100μm Chip thick.	Applicable Chip-to-chip	>10mW /connect

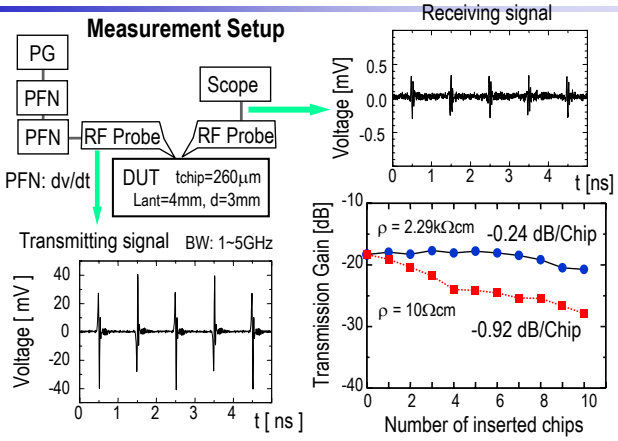
HiSIM MOS Model

Model	Year (96 98 00 02 04)	Nr. of model parameter	Physics based	Accuracy, reliability
BSIM (UC Berkeley)	Ver.Ⅲ Ver.Ⅳ	300	×	×
Model 11 (Philips) SP2000 (U. Penn. St.) Surface Potential (anal.)			○	×
HiSIM (Hiroshima U.) Surface Potential(exact)	Ver. Ⅰ Ver. Ⅱ	75	○	○ Gm/Id, Noise, Distortion

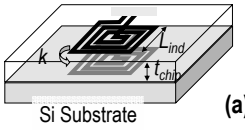
Compact Model Council will select the next MOS model by the end of 2005. HiSIM was selected a promising candidate of 1st stage in July 2004, and is now under the testing by affiliations over the world.

By the joint research with the modeling group and the design group, HiSIM parameters of 0.18μm RF CMOS were extracted and simulation environment installing the latest HiSIM model was developed.

Transmission of Gaussian Monocycle Pulses

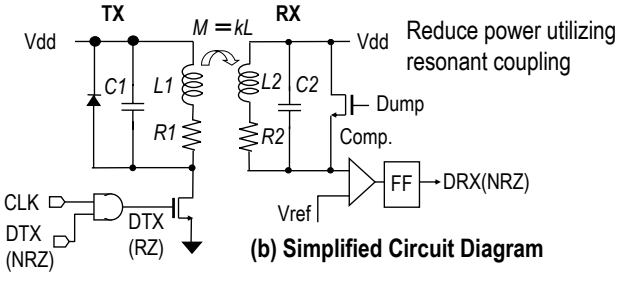


Wireless Interconnect using Inductor Coupling



tchip= 50 - 100μm
Lind= 50 - 200μm

(a) Inductor Structure



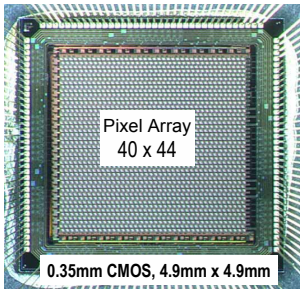
Reduce power utilizing resonant coupling

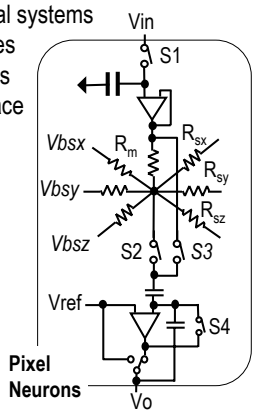
(b) Simplified Circuit Diagram

Multi-chip Vision (MCV) and Pixel Circuit

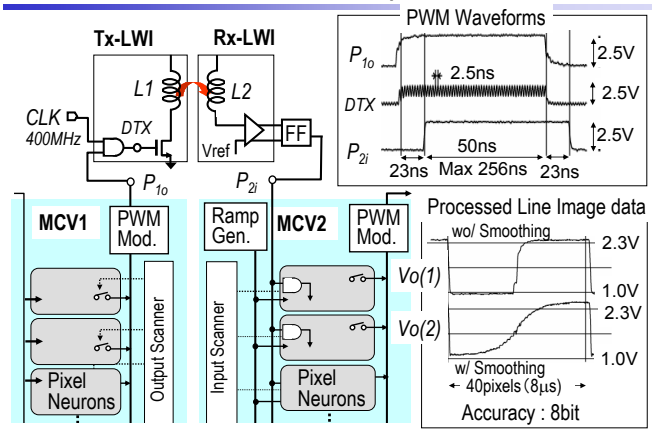
Architecture based on vertebrate visual systems

1. Time difference by analog memories
2. Space filtering by resistive networks
3. PWM-based line parallel I/O interface





Measurements of Multi-Chip Vision with LWI



Optoelectronic Devices and Integration

Integrated Optoelectronic Functional Devices

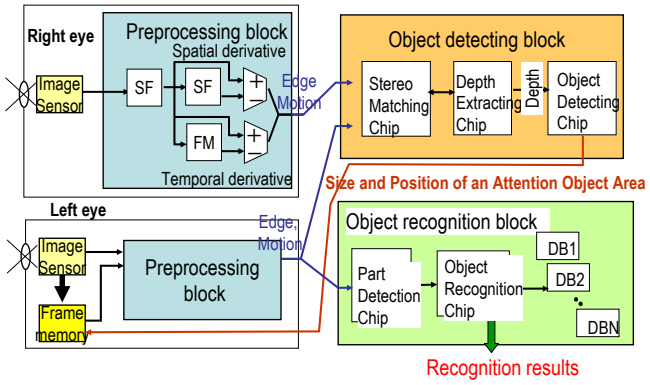
In order to overcome the speed limit of the metal interconnection in LSI, we are studying compact ring-resonator optical switches using electro-optic (EO) and magneto-optic (MO) materials, which can be monolithically integrated in LSI.

Si-based Quantum Dots Floating gate Device

Optical Input Switching & Memory Operation at Room Temp.

- Measurements of C-V char. of QD floating gate MOS capacitors and displacement current under light illumination and in dark.
- Unique hysterics due to electron charging and discharging are observed.

Multi-object Recognition System

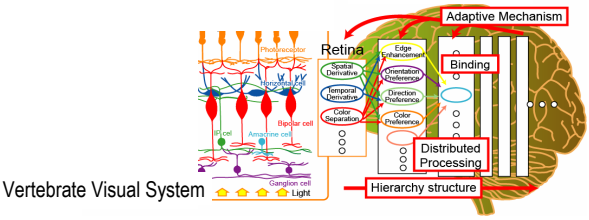


Motivation to implement Brain Function

Development of architecture and algorithms to implement **brain function** utilizing advance integration technologies.

Image Processing of Vertebrate brain:

1. Image feature extraction & its binding by Neural Nets
2. Adaptation to environment change by FB mechanism



I. Ring Resonator Optical Switches using EO Material

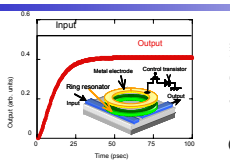


Fig. 1 Simulated response characteristics of the ring resonator optical switch using electro-optic material.

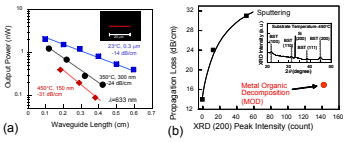


Fig. 2 (a) Output light power of the BST waveguide versus waveguide length, (b) propagation loss versus XRD peak intensity of BST(200).

II. Ring Resonator Optical Switches using MO Material

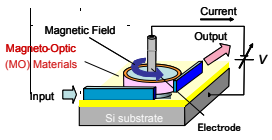


Fig. 3 Newly proposed ring resonator optical switch using magneto-optic material.

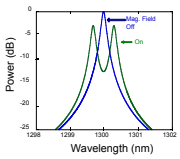
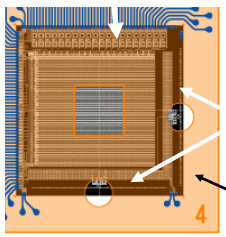


Fig. 4 Resonance characteristics of the ring resonator optical switches using magneto-optic material without polarizer

Vision Chip with LWI and GWI and 3DCSS Prototype

Spiral Inductors



Antennas

Flexible Printed Circuits: FPC

Features

1. Improve Reliability and Yield
2. Resolve problems in KGD and heat radiation

Parameters

L_{ant}= 2-4 mm, L_{ind}= 50 - 200μm

No. of Chips= 10-100

t_{chip}= 50 -100μm