System LSI: Challenges and Opportunities

Tadahiro Kuroda
Department of Electronics and Electrical Engineering
Keio University, Yokohama, Japan

Abstract

End of CMOS scaling has been discussed in many places since the late 90's. Even if the end of CMOS scaling is irrelevant, it is for sure that we are facing a turning point in semiconductor business. In this paper, challenges and opportunities of system LSI are discussed from three levels of perspectives.

Transistor Level (Physics)

What will happen if we continue to scale a CMOS device? Gate controllability will be degraded. If gate oxide thickness is kept constant in order to suppress gate leakage, and if channel length is scaled further, potential of silicon surface near the source that is associated with V_{TH} is lowered by depletion layer capacitance of the drain (C_D), as well as gate capacitance (C_G). When C_D is not small enough compared to C_G, MOSFET behaves like a resistor, not a transistor. In other words, MOSFET does not turn off sufficiently. On top of that, leakage from gate is rapidly increasing. It should be noted that I_{off} dependence on temperature is diminishing as technology scales. This indicates that the leakage is caused by tunneling leakage that depends on barrier thickness, not height. In the 45nm technology node, I_{off} will reach to an unacceptable level.

How to cope with the leakage problem? There are two approaches. One is to change material. High-*k* gate dielectric together with metal gate is a must. Another important change in material is strained silicon. Mobility is increased in NMOS by pulling silicon body, while in PMOS by pushing it. I_{on} can be increased by 10 to 25 percent for the same leakage current, or I_{off} can be reduced by 85 to 100 percent for the same I_{on}, or active power dissipation can be reduced by 15%. An advantage of the strained silicon technology is that its associated penalty is small. Two approaches are investigated, substrate-strained silicon and process-induced strained silicon.

The second approach to improve I_{on}/I_{off} is to change structure of a device. Degradation in I_{on}/I_{off} is caused by poor gate controllability. Leakage current flows deep in body where gate control does not reach sufficiently. Therefore, by thinning body, the leakage current can be suppressed. If body is as thin as about 1/3 of channel length, leakage current is sufficiently suppressed. Ultra thin body approach, however, has difficulty in scaling. Double gate can ease body thickness to 2/3 of channel length. Non-planer structure, such as FinFET, is widely investigated.

In this way, CMOS scaling will continue, but not in the same fashion as before. We need to introduce various new technologies, namely technology boosters. Even though each technology booster does not continue to improve device performance by scaling, various technology boosters are currently investigated and they will be introduced continuously. Device technology will further be evolve and revolve. 3D integration, carbon nanotube-FET, single-electron devices, molecular devices, DNA computing, and spintronics will emerge.

IC Level (Electronics)

Leakage problem of a transistor shall be solved by intelligence and enthusiasm of device engineers. Difficult problems are shifting from transistor level (physics) to integrated circuit level (electronics). Two issues will stand in our way: powerwall and variations.

A) Power Aware Computing

CMOS power dissipation is increasing as a natural result of device scaling. It was increased four fold every three years until the mid 90's, as a result of the constant voltage scaling. Recently, it is increased double every six years under the constant field scaling. Since it is very difficult to scale V_{TH} further, active power dissipation may increase rapidly again due to the constant voltage scaling, or active leakage current may increase due to further V_{TH} scaling. In any way, tradeoff between speed and power may be more and more difficult. Since it is based on a device scaling theory, which is the physical principle of semiconductor devices, it is very difficult to cope with this problem. Opportunities may be found in IC design level.

Best practices for power aware CMOS design are summarized as the following ten tips [1]:

Tip 1: Optimize and control V_{DD} and V_{TH}.
Tip 2: Total power is minimum when $P_{leakage}/P_{active}$ = 30/70.
Tip 3: If you don't need to hustle, relax and save power.
Tip 4: Utilize surplus timing with multiple V_{DD}'s and V_{TH}'s.
Tip 5: Total power is minimum when V_{DDL}/V_{DDH} =0.7.
Tip 6: Two types are sufficient.
Tip 7: Adapt to the change with variable V_{DD} and V_{TH}.
Tip 8: Two levels are sufficient.
Tip 9: Cooperate across various levels of design hierarchy.
Tip 10: Right circuit for the right job.

For instance, a tiny microprocessor is embedded in a next generation Intel microprocessor, Montecito (Itanium), that controls power supply voltage and clock frequency by monitoring power dissipation, temperature and supply voltage. Montecito outperforms the previous design named Madison with less power dissipation. In this way, dynamic voltage control and frequency control will be carried out more sophisticatedly and in finer granularity.

B) Power Aware Communications

As VLSI technology scales, the gap between chip performance and I/O bandwidth is widening. In order to fill the gap between the chip performance and pin bandwidth, various circuit techniques have been employed, such as pre-emphasis in a transmitter and equalization in a receiver, but at the cost of increase in power dissipation. Communications between chips may scale as well when distance between the chips scales, from board ranges to chip ranges, and beyond.

Obviously, System-on-a-Chip (SoC) is an ultimate solution. However, SoC is a very expensive technology. Good compromise between power, speed, and cost, turn-around-time, may be found in a System-in-a-Package approach, or SiP.

Through-Si-Via technologies with high density vertical interconnections through a chip have been investigated by many researchers for many years. They are not practical applications yet, though. The reasons are from the following issues and drawbacks of the approach. 1) yield degradation due to difficulty in screening a known good die. 2) cost increase caused by addition in process complexity, as well as reliability issues caused by mechanical contacts, and 3) scaling beyond 30μm may be very difficult in the mechanical contact.

Research on wireless inter-chip data communications has attracted attentions. All the above mentioned issues can be solved. Furthermore, the thinner the chip thickness, the shorter the communications distance, and the better channel performance. Thinning a chip has not been challenged before, just because there was no such a demand. A great opportunity may be found. A scaling scenario may be found where cost/performance ratio can be improved by scaling a chip not only horizontally but also vertically.

Two technologies have been investigated: capacitive coupling [2-3] and inductive coupling [4-9]. In the inductive coupling, chips are stacked, whether they are faced up or down, and inductively coupled by metal spiral inductors. Current change in a transmitter is transferred to a receiver as a voltage signal. Some of recent research achievements will be discussed in the presentation.

Business Level (Economics)

Mr. Gorden Moore from Intel mentioned in a plenary talk of ISSCC2003 that no exponential is forever, but 'forever' can be delayed! Prof. Chemming Hu of U.C. Berkeley presented a grand view of CMOS technology and industry at the plenary talk at CICC2004, entitled "CMOS for one more century". The message was CMOS must and will meet world's needs for intelligent devices through 21st century. Dr. Kazuo Yano from Hitachi mentioned in a workshop of ISSCC2002 that wide ranges of the semiconductor technology from high-end microprocessors to tiny RFID chips will be used for a wide variety of new applications. Prof. Takayasu Sakurai of Univ. of Tokyo mentioned in his plenary talk of ISSCC2003 that power-aware electronics opens up vast new applications and markets. Dr. Tsuguo Makimoto, ex-CTO of Sony, gave a message in his luncheon talk at CICC2003 that robotic chip will be a technology driver in the coming decades.

I think that computers will be invisible behind broadband networks as servers, while terminals will come closer to us as wearable and implantable devices, more friendly devices with intelligent Human Computer Interactions. I think three key technologies are essential: short range wireless interface and intelligent Human Computer Interactions for access networks, and broadband high-speed links for backbone networks. IC chips will be implanted everywhere so that things can think and talk for distributed information processing. For example, it will be possible to automatically detect who enters a room so that air conditions can be locally adjusted according to his/her preference.

Summary

Scaling of CMOS integrated circuits is becoming difficult, due to increase in power dissipation and device variations. Post-CMOS device for mass production, however, is not on the horizon. Even though speed of technology improvement may be slowed down compared to that before, the semiconductor industry and technology will continue to develop and improve remarkably. We will enter the golden era of opportunities for both technology and industry. Computers and communications will be scaled further, merged together, and materialized in consumer applications. In order to make this ubiquitous society possible, intelligent interface based on low-power, high-speed CMOS design is inevitable. Especially, three key technologies are essential: short range wireless interface for access networks, broadband high-speed serial links for backbone networks, and intelligent Human Computer Interactions. In addition, integrated design engineering through system, circuit, device, process, lithography, and packaging, will be essential, as well as extended learning and knowledge such as nanotechnology, biology, and robotics. The era will transit from "Know-How (craftsman's age)" to "Know-What (visionary's age)", and further to "Know-Who (producer's age)".

Acknowledgements

The author would like to acknowledge Prof. Iwata, Prof. Yokoyama, and Prof. Kikkawa for encouragement.

References

[1] T. Kuroda, "10 Tips for Low Power CMOS Design," DAC, June 2003.
[2] K. Kanda, *et al.*, "A 1.27Gb/s/ch 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC*, pp.186-187, Feb. 2003.
[3] R. J. Drost, *et al.*, "Proximity Communication," *CICC*, pp.469-472, Sep. 2003.
[4] D. Mizoguchi, *et al.*, "A 1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-chip Signaling (IIS)," *ISSCC*, pp.142-143, Feb. 2004.
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[9] M. Sasaki, *et al.*, "A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication Scheme," *Symposium on VLSI Circuits*, pp. 348-349, June 2005.

System LSI : Challenges and Opportunities

Tadahiro Kuroda
Keio University
www.kuroda.elec.keio.ac.jp

End of CMOS Scaling ?

- ITRS roadmap: solutions are not known (red)

製造年	単位	2003	2004	2005	2006	2007	2008	2009	2012	2015	2018
ゲート長	nm	45	37	32	28	25	22	20	14	10	7
Equivalent Oxide Thickness (EOT)	Å	13	12	11	10	9	8	8	7	6	5
ゲート絶縁体、最薄厚度	Å	8	8	7	7	4	4	4	4	4	4
最大ゲート・リーク電流	A/cm²	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03	2.4E+03	1.0E+04	2.4E+04
サブスレショルド・リーク電流	nA/um	30	50	50	50	70	70	70	100	300	500
サブスレショルド特性劣化係数		1	1	1	1	1	0.8	0.7	0.5	0.5	0.5
飽和電流最大係数		1	1.3	1.3	1.4	2	2	2	2	2	2
動作温度最大係数		1	1	1	1	1	1	1	1.1	1.3	1.3
相対性能		1.00	1.26	1.39	1.60	1.86	2.20	2.49	4.05	6.80	10.77

- "Life after CMOS: Imminent or Irrelevant?" (DAC 2002, session)
- "Changing Vectors of Moore's Law" (IEDM 2002, luncheon)
- "Workshop on Implications of Near-Limit CMOS on Circuits and Applications" (ISSCC 2002, workshop)
- "Scaling Limit in a Power Limited Environment, Architecture versus Circuit Design" (Symp. VLSI Circuits 2002, panel)
- "For The LAST Time, Who is Going to Solve the POWER Problem!" (IEDM 2003, panel)

Strategy Shift

高速MPU開発を中止
インテル

【シリコンバレー＝小柳連彦】米インテルが、主力製品であるパソコン用超小型演算処理装置（MPU）の高速品の開発を中止することが明らかになった。

回路の線幅が微細化したことによる電流増もあるため、チップ内部が熱で溶けないようにしながら周波数を上げるのは極めて難しくなっている。

作周波数は一秒に三十六億回動作する三・六ギガヘルツ。

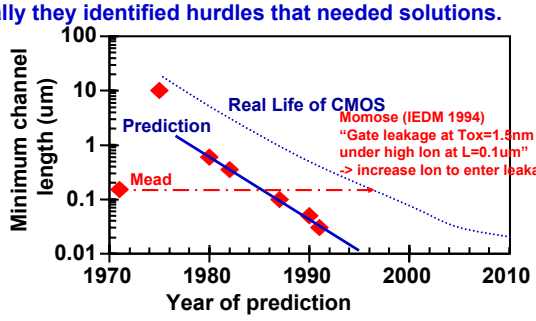
同社が販売している最高速のペンティアム4の動作周波数を性能向上の最大の武器にしてきた同社の技術戦略が根本的に変わる。

動作周波数はチップが一秒間に何回の処理動作をするかを表す。周波数を上げると処理速度が増す一方、チップ内に流れる電流が多くなる。現在

2004/10/16 日経新聞朝刊

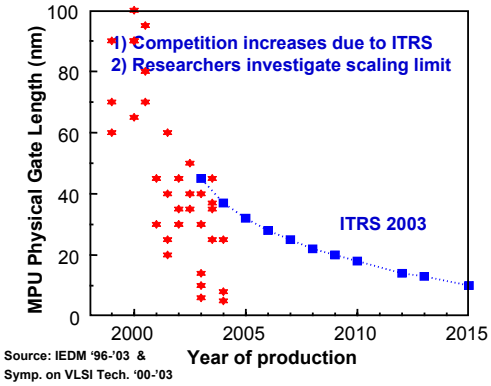
Prediction of Lower Limit

Pessimistic opinions have been proven wrong time & time again!
Actually they identified hurdles that needed solutions.

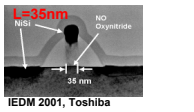


Carver Mead & Lynn Conway, "Introduction to VLSI Systems" (1980)
Section 9.8: Quantum mechanical lower limit (tunneling effect will dominate device operation)
"Thickness such as gate oxide and depletion layer should be larger than several nano-meters."

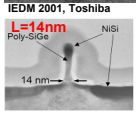
Accelerated CMOS Scaling Research



Source: IEDM '96-'03 & Symp. on VLSI Tech. '00-'03

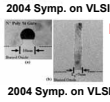


IEDM 2001, Toshiba



IEDM 2002. Toshiba

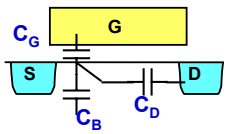
2004 Symp. on VLSI Tech., Toshiba



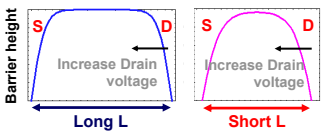
2004 Symp. on VLSI Tech., TSMC

Degraded Gate Controllability

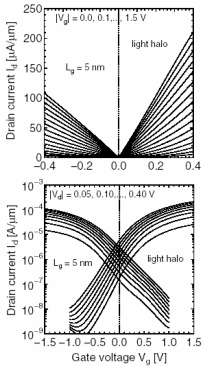
- When Tr is too small, it becomes a resistor, since C_D becomes comparable to C_G.



- Drain Induced Barrier Lowering (DIBL)



- Tr does not turn off, nor saturate.

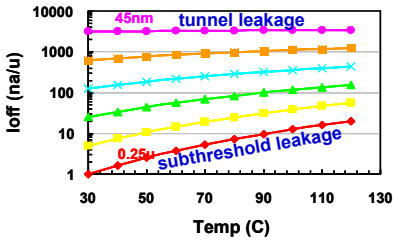


Courtesy: S. Narendra

Degraded I_{on} / I_{off}

Tradeoff: ON / Off
(V_{TH})

Leakage !

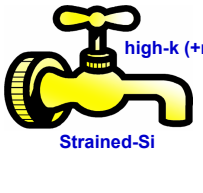


New Material

Tradeoff: ON / Off
(V_{TH})

1) material

Leakage !

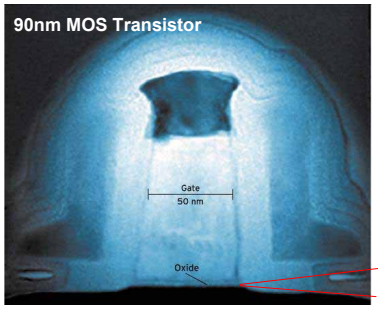


high-k (+metal)

Strained-Si

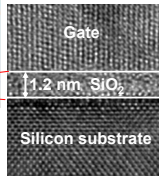
T. Kuroda, "Will SOI ever become a mainstream technology? " *IEDM'02*, panel.

Gate Leakage Reduction by High-k & Metal Gate



■ Gate oxide thickness is reduced by 2~4A/generation (1.2nm@90nm, 1.0nm@65nm, 0.8nm@45nm)

■ 3A equivalent oxide reduction by using metal gate to eliminate poly-gate depletion layer



~0.3nm: depleted

4 layer of SiO_2 molecule

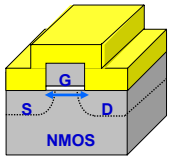
Gate Leakage Solutions:
High-k + Metal Gate

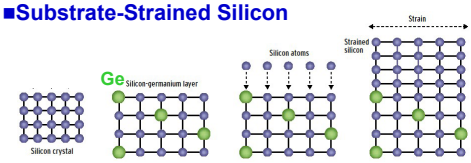
issues: mobility, reliability

Source: Spectrum IEEE, Pat Gelsinger, Intel

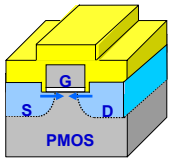
I_{ON} Increase by Strained Silicon

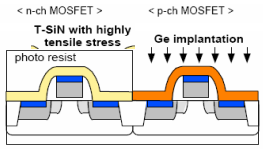
■Substrate-Strained Silicon





■Process-Induced Strained Silicon





■10-25% higher Ion, 80-100% Ioff reduction, 15% P_{active} reduction

■Small penalty

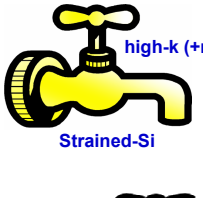
Source: Mark Bohr, Intel

New Structure

Tradeoff: ON / Off
(V_{TH})

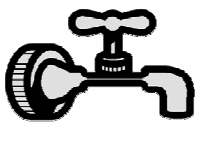
1) material
2) structure

Leakage !

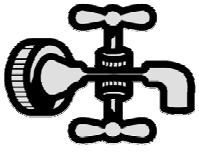


high-k (+metal)

Strained-Si



Ultra Thin Body



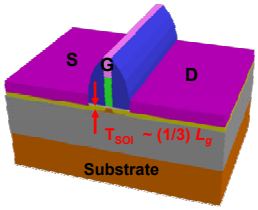
Double Gate

Surrounding Gate

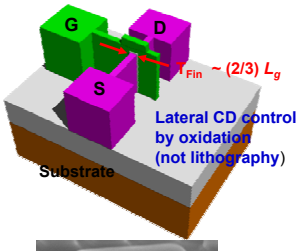
T. Kuroda, "Will SOI ever become a mainstream technology? " *IEDM'02*, panel.

Beyond Conventional CMOS

Ultra Thin Body



FinFET



Lateral CD control by oxidation (not lithography)

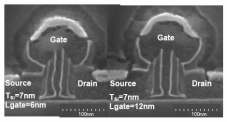
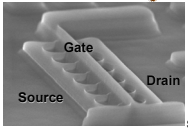
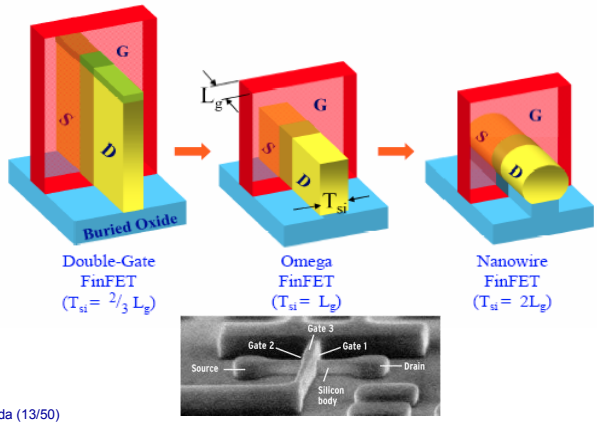


Fig.17: SEM cross-section of ultra-thin silicon channel pFETs with 6nm and 12nm gate lengths IEDM 2002 (IBM)



Source: Intel

Multi-Gate CMOS

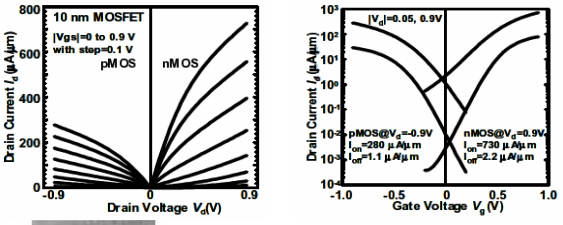


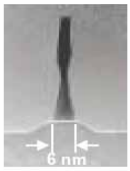
Double-Gate FinFET ($T_{si} = {}^2/_3 L_g$)

Omega FinFET ($T_{si} = L_g$)

Nanowire FinFET ($T_{si} = 2L_g$)

10nm CMOS (for 2016)

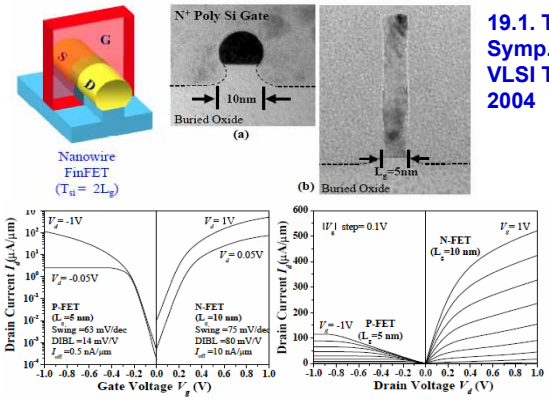




Bulk, SiON, 0.9V, metal-gate, elevated S/D
(ITRS: SOI, high-k, 0.5V, metal-gate)

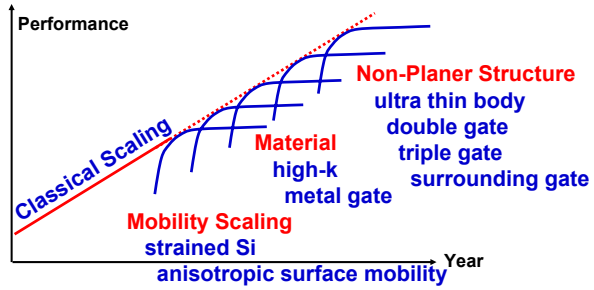
9.1. Toshiba
Symp. on VLSI Tech. 2004

5nm CMOS（for 2020）

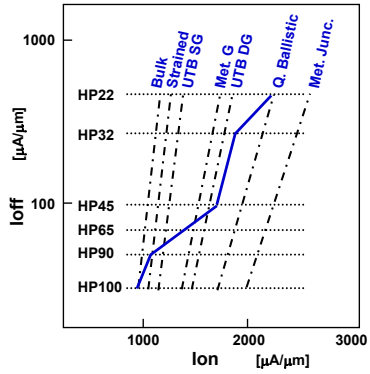


19.1. TSMC
Symp. on VLSI Tech. 2004

Technology Booster



Technology Booster

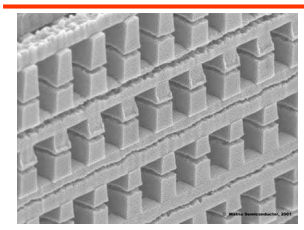


Const. Electric Field Scaling

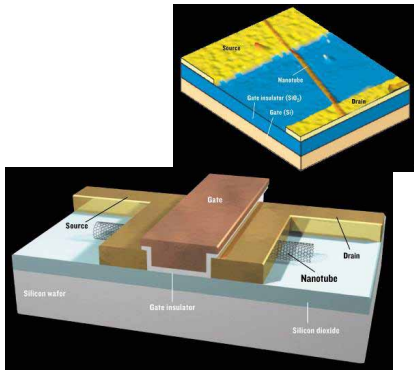
$$\frac{I_{on}}{W} \propto \frac{\varepsilon}{t_{ox}} \frac{(V_{GS} - V_{TH})^2}{L} \rightarrow const.$$

TB improves Ion and mitigates degradation of Ion/Ioff

From Evolutional to Revolutionary

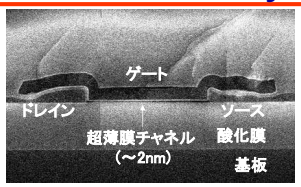


3D integration

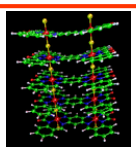


Carbon nanotube FET

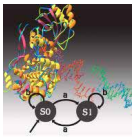
Revolutionary Nano Technology



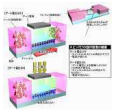
Single-electron memory (SESO, Hitachi)



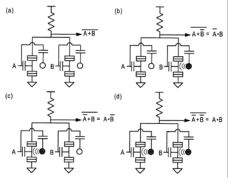
Molecular devices



DNA computing



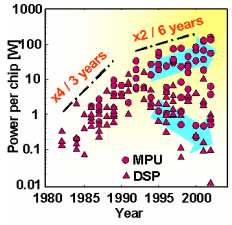
Spintronics

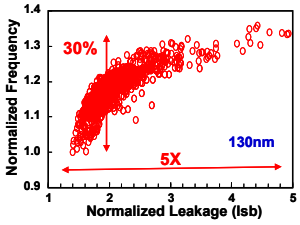


Single-electron logic (SET, Toshiba)

Challenges and Opportunities

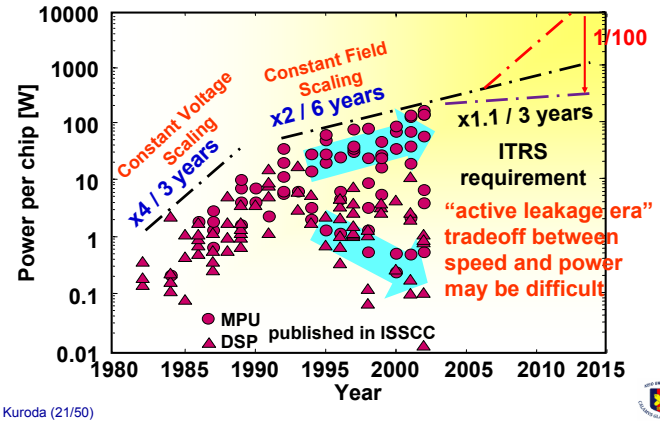
- Transistor Level (Physics)
  Leakage problem shall be solved.
- Integrated Circuit Level (Electronics)
  Powerwall (power vs. speed)
  Variations





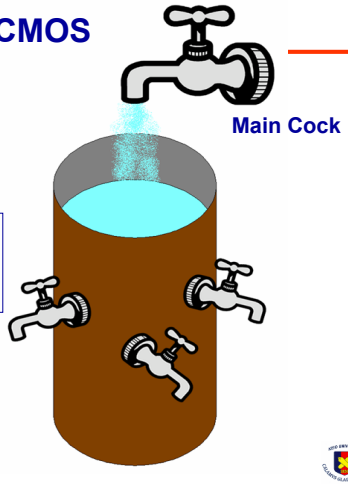
Source: S. Borkar, Intel

Power Increase by Device Scaling



MTCMOS

PLEASE TURN OFF AT THE MAIN
When Not In Use



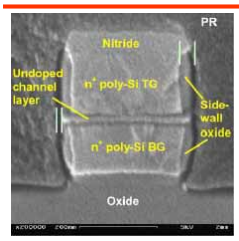
T. Kuroda, *IEDM'02*, panel.

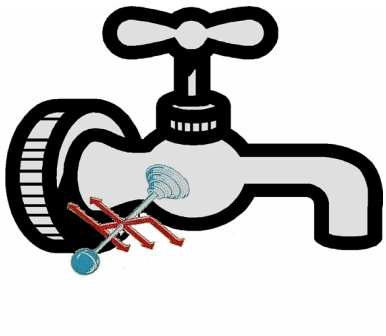
VTCMOS

PLEASE ADUST PERFORMNACE

T. Kuroda, *IEDM'02*, panel.

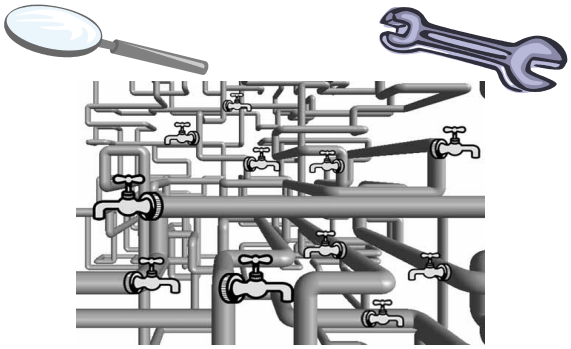
Please Give Us Controllability on V_{TH}





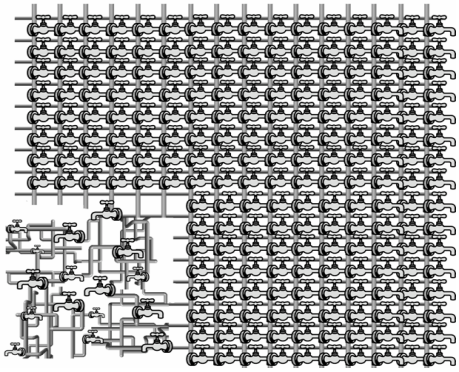
T. Kuroda, *IEDM'02*, panel.

EDA



T. Kuroda, *IEDM'02*, panel.

Mostly Regular



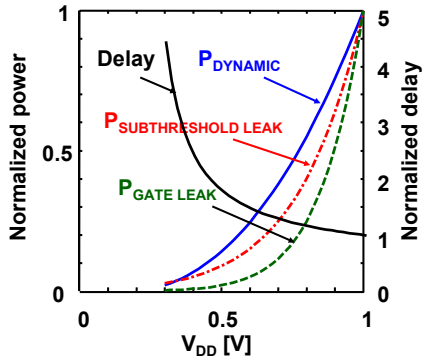
T. Kuroda, *IEDM'02*, panel.

Ten Tips

- **10 Tips for power aware CMOS design**
  - **Tip 1: Optimize and control V_{DD} and V_{TH}.**
  - **Tip 2: Total power is minimum when $P_{leakage}/P_{active}$ = 30/70.**
  - **Tip 3: If you don't need to hustle, relax and save power.**
  - **Tip 4: Utilize surplus timing with multiple V_{DD}'s and V_{TH}'s.**
  - **Tip 5: Total power is minimum when V_{DDL}/V_{DDH} =0.7.**
  - **Tip 6: Two types are sufficient.**
  - **Tip 7: Adapt to the change with variable V_{DD} and V_{TH}.**
  - **Tip 8: Two levels are sufficient.**
  - **Tip 9: Cooperate across various levels of design hierarchy.**
  - **Tip 10: Right circuit for the right job.**

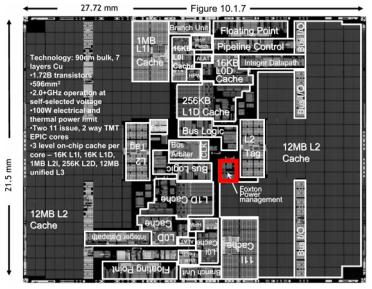
T. Kuroda, "10 Tips for Low Power CMOS Design," in *Proc. DAC'03*, tutorial, Jun. 2003.

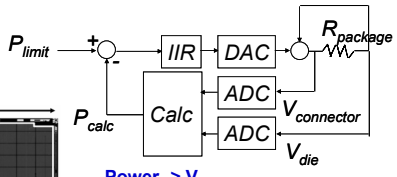
Dynamic & Leakage Power Reduction



65nm tech. Node
V_{TH}=0.15V
DIBL coeff.=0.2

Dynamic & Leakage Power Reduction

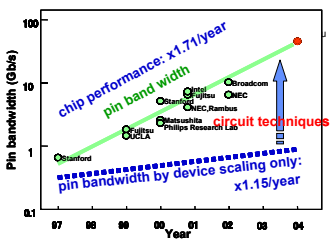


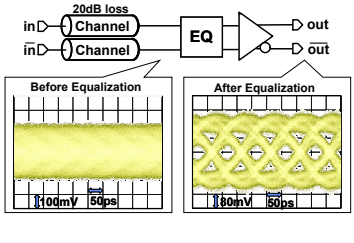


Power -> V_{DD}
Temp. -> V_{DD}
V_{DD} -> f

Montecito (90nm)
ISSCC'05 [16.2, 16.7]
1.5-2X performance
0.8X power
of Madison-9M (130nm)

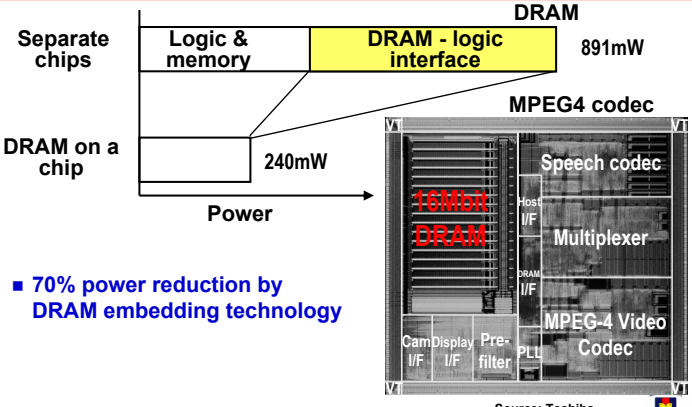
Challenges in Inter-Chip Interface





- **I/O is a primary bottleneck of system performance.**
- **Communications does not scale as computation scales by device scaling.**
- **Circuit techniques (e.g. equalization) consumes large power dissipation.**
- **Communications scale by distance scaling from board, to chip, and beyond.**
- **Moor's law in inter-chip communications is expected.**

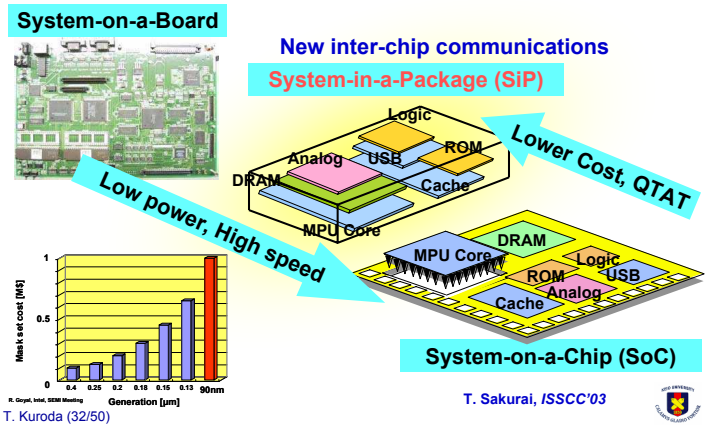
SoC Improves I/O Performance



Source: Toshiba

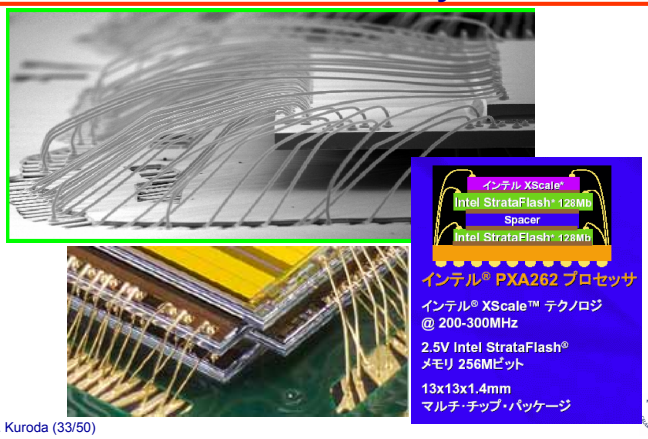
- 70% power reduction by DRAM embedding technology

From SoC to SiP

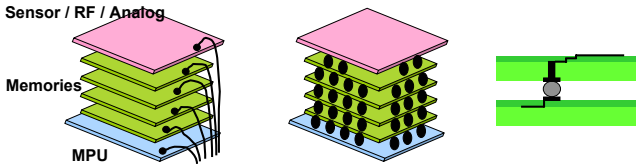


T. Sakurai, *ISSCC'03*

MPU + Memory

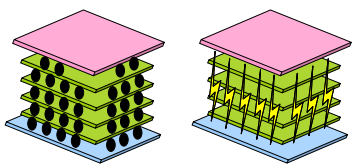


From Line to Area



- **Bonding (Conv.)**
  - (+) low cost, practical
  - (-) peripheral contact: long distance (~10mm) small # of connections (~100)
- **Through Si Via (Future)**
  - (+) area contact: short distance (~0.1mm) large # of connections (~10000)
  - (-) low yield due to Known Good Die issue : difficult to test in fine pitch
  - (-) expensive process / reliability issue
  - (-) scaling limit due to mechanical contacts (~30μm pitch)

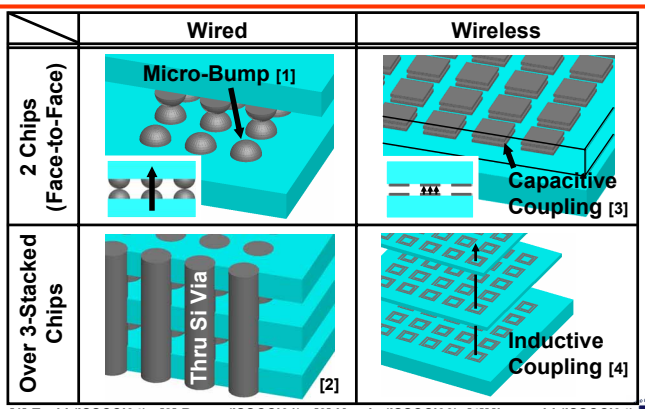
From Mechanical to Electrical



- Proposal
  - wireless transceiver arrays

- **3D-MEMS**
  - (-) KGD
  - (-) process
  - (-) scaling limit
- **Wireless Super-Connect (WSC)**
  - (+) KGD solvable : easy to attach and remove
  - (+) no addition in process, no reliability issue
  - (+) scalable (below 30μm pitch)
  - (+) opportunity of thinning a chip
  - (+) channels through active devices
  - (+) low power : no ESD protection required

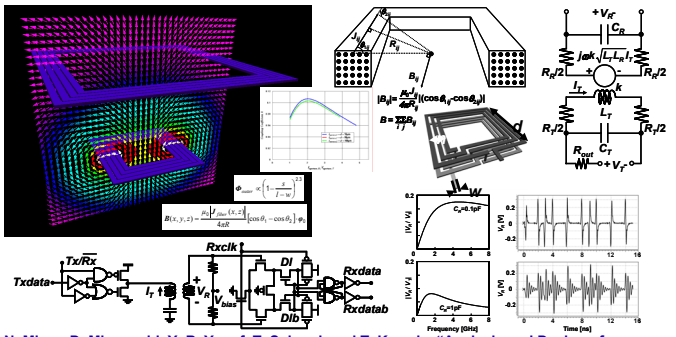
3D Interface



[1] Ezaki (ISSCC'04) [2] Burns (ISSCC'01) [3] Kanda (ISSCC'03) [4]Mizoguchi (ISSCC'04)

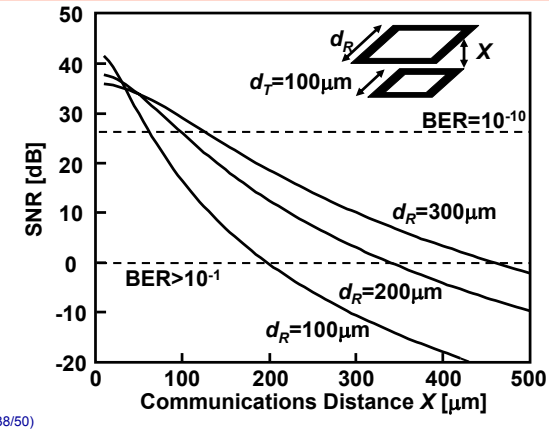
Integrated Design

- Electromagnetics, Electrical Circuits, LSI Layout, Signaling



N. Miura, D. Mizoguchi, Y. B. Yusof, T. Sakurai, and T. Kuroda, "Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-chip Wireless Superconnect," *2004 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 246-249 June 2004.

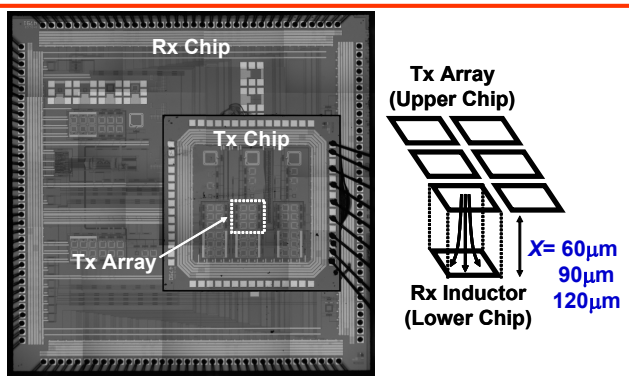
SNR Dependence on Distance



Scaling Scenario

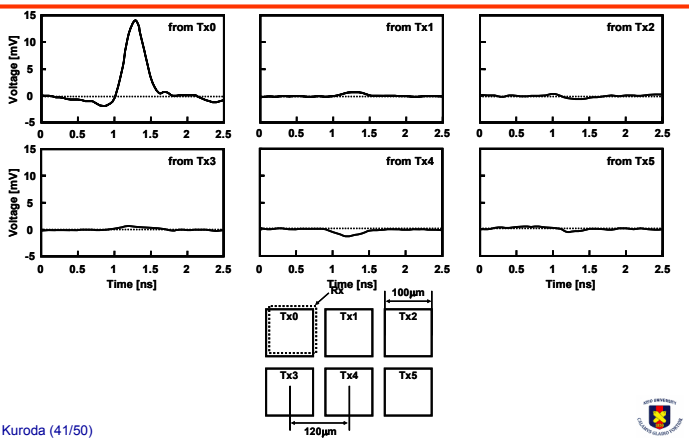
Process	Chip Thickness	Inductor Diameter	Transmit Power	Data Rate	Power
0.35μm	240μm	300μm	43mW	1.25Gb/s/ch	46mW
90nm	30μm	300μm	1mW	1.25Gb/s/ch	1.1mW
90nm	30μm	50μm	21mW	1Tb/s/mm^2	4.2W

Crosstalk Measurement

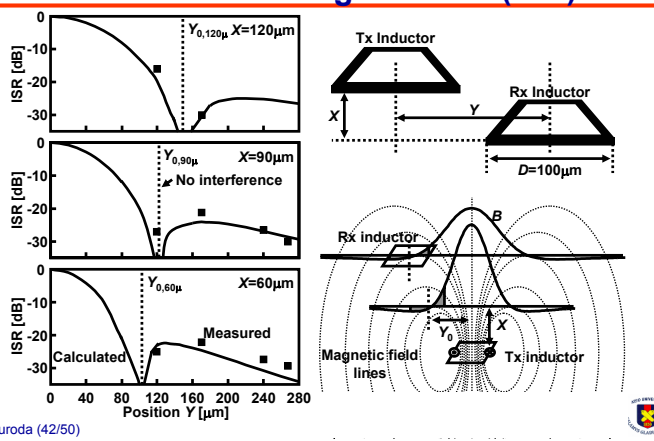


N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Cross Talk Countermeasures in Inductive Inter-chip Wireless Superconnect," *CICC'04*, pp.99-102, Oct. 2004.

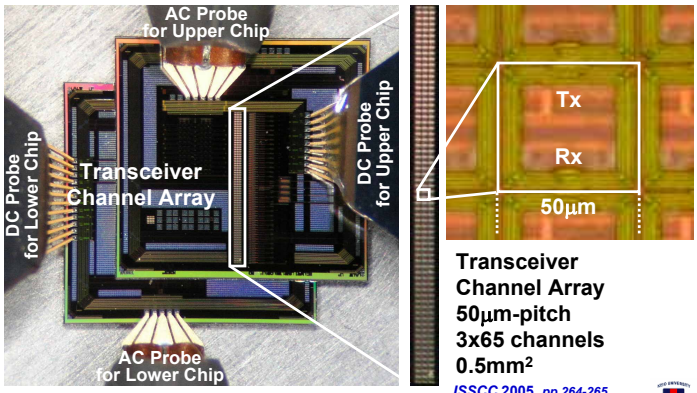
Crosstalk Measurement



Interference to Signal Ratio (ISR)



3 x 65 Channel Arrays

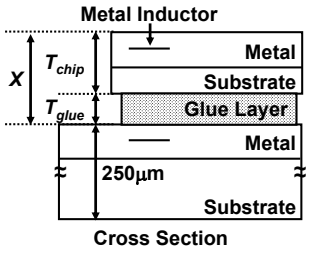


Transceiver
Channel Array
50μm-pitch
3x65 channels
0.5mm²

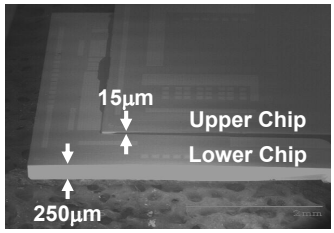
ISSCC 2005, pp.264-265

Communication Distance

- T_{chip}=10μm, T_{glue}=5μm, X_{min}=15μm



Cross Section



- Multiple stacking
  - Emulated by changing chip thickness, T_{chip}
    → X=15, 28, 36, 43, 59μm (=2, 3, 3, 4, 5 stacking)

Performance Comparison

	Inductive Coupling	Micro Bump	High Speed Serial Link
Aggre. Data Rate	195Gb/s (20)	160Gb/s (16)	10Gb/s (1)
Power Dissipation	1.2W (3.3)	No Data	0.36W (1)
Area	0.5mm² (0.25)	4.5mm² (2.25)	2.0mm² (1)
Process	0.25μm	0.15μm	0.13μm
	Keio (ISSCC'05)	Sony (ISSCC'04)	

Future Works

- BER<10^{-14}
- Enlarge array size (> 1000 channels).
- Investigate eddy current effect in substrate, interconnection, and package.
- Investigate influence to memory (DRAM/flash) circuits, and interference from digital (MPU) circuits.
- Find (define) killer applications.
- Build system; chips with transceivers in SiP + test header
- Investigate scaling scenario.
- Study C-coupling vs. L-coupling.

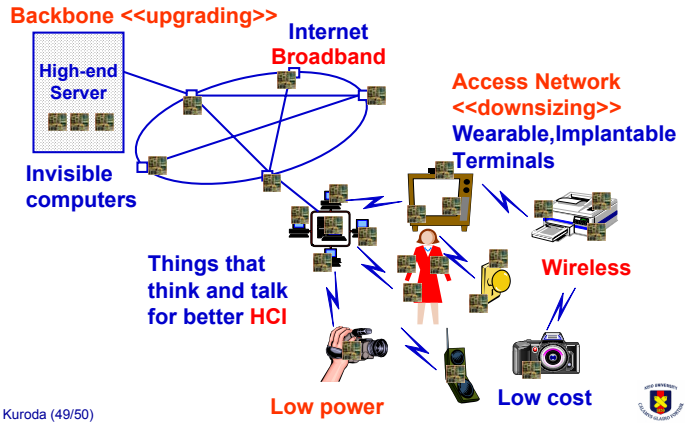
Challenges and Opportunities

- Transistor Level (Physics)
  - Leakage Problem
  - Variations
- Integrated Circuit Level (Electronics)
  - Powerwall (power vs. speed)
  - Variations
- Business Level (Economics)
  - Post PC Applications
  - SoC vs. SiP

Notable Remarks

- Gordon Moore, Intel (ISSCC2003, Plenary Talk)
  "No Exponential is Forever: But 'Forever' Can Be Delayed! "
- Chemming Hu, UCB (CICC2004, Plenary Talk)
  "CMOS for One More Century"
- Kazuo Yano, Hitachi (ISSCC2002, Workshop)
  "We will enter the golden era of opportunities for both technology and industry."
- Takayasu Sakurai, U. of Tokyo (ISSCC2003, Plenary Talk)
  "Power-aware electronics opens up vast new applications and market."
- Tsugio Makimoto, Sony (CICC2003, Luncheon)
  "Robotic chip will be a technology driver in the coming decades."

Ubiquitous Computing



Summary

Scaling of CMOS integrated circuits is becoming difficult, due to increase in power dissipation and device variations. Post-CMOS device for mass production, however, is not on the horizon. Even though speed of technology improvement may be slowed down compared to that before, the semiconductor industry and technology will continue to develop and improve remarkably for more than a century. We will enter the golden era of opportunities for both technology and industry. Computers and communications will be scaled further, merged together, and materialized in consumer applications. Computers will be small terminals that are implanted in every thing. They will be connected to a network by a wireless technology so that they can be used comfortably wherever you may go. In order to make this ubiquitous society possible, intelligent interface based on low-power, high-speed CMOS design is inevitable. Especially, three key technologies are essential: short range wireless interface and intelligent HCI for access networks, and broadband high-speed links for backbone networks. In addition, integrated design engineering through system, circuit, device, process, lithography, and packaging, will be essential, as well as extended learning and knowledge such as nanotechnology, biology, and robotics. The era transited from 'Know-How (craftsman's age)' to 'Know-What (visionary's age)', and will transit to 'Know-Who (producer's age)'. Role of academia will be more and more important.