High-k Gate Dielectrics for Future CMOS Technology

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Introduction

High-k dielectrics are being actively pursued by the semiconductor industry to replace SiO_2 as the gate dielectric for future generations of CMOS transistors. The 2004 ITRS [1] calls for gate dielectrics of less than 1 nm in equivalent oxide thickness (EOT) in the near future, with a very low gate leakage current. Most experts believe that only some sort of high-k gate dielectrics will be able to fulfill these requirements.

The first group of high-k dielectrics that was proposed to replace SiO_2 in recent years consisted of silicon nitride or silicon oxynitride [2,3]. The concept of using a high-k dielectric's larger physical thickness to achieve the same EOT so as to reduce the tunneling leakage current was clearly presented in [2], and the search for the best high-k gate dielectric has continued ever since.

As a result of intense research efforts throughout the world, significant progress has been made, and there is a clear understanding of the important scientific as well as technological issues that need to be resolved before a viable high-k gate dielectric technology may be implemented in production.

Among these issues, the gate leakage problem seems to be mostly under control, as essentially all research groups have reported high-k gate leakage currents several orders of magnitude lower than their SiO_2 counterparts of the same EOT's. In contrast, other issues such as thermal stability, interfacial layer control, EOT control, reactions with polySi, and metal gate electrodes are still posing varying degrees of challenges that require more R&D to overcome, and this talk will give an overview of these challenges and the progress that has been made by various R&D groups.

Because of the space limitation, this extended abstract cannot cover all of the research results that will be reviewed at the oral presentation; instead, only a few examples will be given here in this written document, and an emphasis will be given on the electrical characterization of high-k gate stacks because of the author's expertise.

Materials and Processing Related Issues

Figure 1 shows a schematic cross-section of a MOSFET, where some key regions surrounding the high-k gate dielectric are highlighted. Of these regions, the high-k/substrate interface is of utmost importance, as it could significantly affect the over-all EOT of the gate stack, as well as the MOSFET's electrical properties and reliability. Since it was suggested that HfO_2 and ZrO_2 should be thermodynamically stable on Si [4], these two dielectrics quickly replaced TiO_2 and Ta_2O_5 as the favorite high-k dielectrics among various R&D groups. Later on it was found that an interfacial layer inevitably formed between HfO_2 or ZrO_2 and Si substrate, despite the theoretical thermodynamic predictions. By then, the momentum was so high that the R&D community decided to lock in the HfO_2 system (as it has a more stable interface with Si than ZrO_2), and tried to use silicate or nitridation to stabilize the interface [7].

Similarly, the electrode/high-k interface is also very important, as the formation of an interfacial layer there normally lowers the effective dielectric constant, and could cause degraded electrical performance. In severe cases, the so-called Fermi-level pinning phenomenon could occur which adversely affects the threshold voltage [5]. Thus, proper engineering of the electrode/high-k interface is another important issue that is being actively pursued.

In addition to the two interfaces described above, the bulk of the high-k film must be thermally stable. While no consensus has reached, many hold the opinion that the high-k gate dielectric must be either amorphous or single crystalline. Since the viability of single-crystalline high-k gate dielectric is still in the distant future, amorphous high-k gate dielectric has become the desired form, instead of the polycrystalline alternative. This is primarily based on the uniformity argument. Essentially, it is known that some properties, such as the dielectric constant and leakage current, are different between the crystalline regions and the grain boundaries, and therefore one would expect significant non-uniformities of EOT, threshold voltage, and gate leakage distributions in high-density integrated circuits containing numerous small-size devices, of which some devices may contain primarily crystalline high-k gate dielectrics while others are primarily around grain boundaries. Given the requirement for an amorphous high-k gate dielectric, the ranking of HfO_2 as a desired high-k gate dielectric drops considerably, because it tends to crystallize at a relatively low process temperature (< 500 °C) [6]. In order to overcome this problem, one may add Al in HfO_2 to form HfAlO [6], or use Hf oxynitride, Hf silicate, or nitrodized Hf silicate [7-9]. All of these approaches raise the crystallization temperature at the expense of reducing the dielectric constant. Figure 2 shows that the dielectric constant is reduced, and the bandgap is increased, with the addition of Al in HfO_2, along with an increase in the crystallization

temperature.

Charge Trapping and Mobility Degradation

It is now well known that the channel mobility in a high-k gated MOSFET is typically lower than its SiO_2-gated counterpart. Since it is also well known that high-k gated MOSFET tends to have more oxide charge and interface traps than its SiO_2-gated counterpart, it's not surprising that many attribute the degraded channel mobility to Coulomb scattering by oxide charge and interface traps. Upon more careful examination, however, we found that part of the degradation may arise from the soft optical phonons in the high-k gate dielectric that act as "remote phonon scattering centers" and reduce the channel mobility, which is consistent with the theory proposed by Fischetti et al [10]

In the course of our study of channel mobility to determine the possible scattering mechanisms, we found that the conventional methodology used to obtain the channel mobility in high-k gated MOSFET gives rise to very large errors, due to the trapping of carriers. Basically, the use of the conventional split C-V method to extract the carrier concentration in the conduction channel over estimates that concentration due to trapping of carriers, which results in an underestimate of the channel mobility [11]. This error could be as high as 30-50%, based on the typical interface trap density of high $10^{11}/cm^2$ to low $10^{12}/cm^2$ [11]. Therefore, we have introduced a modified split C-V method to more accurately extract the channel mobility [11], and this methodology is briefly depicted in Fig. 3.

It should be noted that trapping/detrapping time constants for some of the high-k gate dielectrics, including HfO_2 and Al_2O_3, are much shorter than those for SiO_2 [12], and therefore the DC measurement methodology commonly used for MOS devices with SiO_2 gate dielectric will likely to miss these traps. A transient (pulsed) measurement methodology has been introduced to reveal more fully the traps in high-k gate dielectrics [12].

Using the more accurately determined mobility data, we have analyzed the possible scattering mechanisms that may have caused the degraded mobility in high-k gated MOSFETs, and concluded that Coulomb scattering indeed plays a critical role in reducing the channel mobility in high-k gated MOSFET, as expected. Figure 4 shows the strong correlation between the channel mobility and the density of interface traps which serve as Coulomb scattering centers. In addition, we have also gathered evidence that supports the "remote phonon scattering" theory proposed by Fischetti, et al [10]. Figure 5 shows that, compared to its SiO_2 counterpart, the sample made of HfO_2 as the gate dielectric suffers from additional source of phonon scattering, which can be attributed to the "remote soft optical phonons" in the HfO_2 layer

Inelastic Electron Tunneling Spectroscopy (IETS)

This section introduces a novel technique to probe phonons, traps, microscopic bonding structures, and impurities in high-k gate dielectrics with a versatility and sensitivity that are not matched by other techniques. This technique is called the Inelastic Electron Tunneling Spectroscopy (IETS), which basically takes the 2nd derivative of the tunneling I-V characteristic of an ultra-thin MOS structure.

The basic principle of the IETS technique is illustrated in Fig.6, where one can see that, without any inelastic interaction, the I-V characteristic is a smooth curve, and its 2nd derivative is zero. When the applied voltage causes the Fermi-level separation to be equal to the characteristic interaction energy of an inelastic energy loss event for the tunneling electron, then an additional conduction channel (due to inelastic tunneling) is established, causing the slop of the I-V characteristic to increase at that voltage, and a peak in its 2nd derivative plot, where the voltage location of the peak corresponds to the characteristic energy of the inelastic interaction, and the area under the peak is proportional to the strength of the interaction.

In a typical MOS sample, there are more than one inelastic mode, as a wide variety of inelastic interactions may take place, including interactions with phonons, various bonding vibrations, bonding defects, and impurities. Therefore, Fig.7 is shown to represent the typical IETS spectrum that one expects to see.

Figure 8 shows an actual IETS spectrum taken on an $Al/HfO_2/Si$ sample, where the features below 80 meV correspond to Si phonons and Hf-O phonons, and the features above 120 meV correspond to Hf-Si-O and Si-O phonons. The significance of this IETS spectrum is that it confirms the strong electron-phonon interactions involving optical phonons in HfO_2, and that the Hf-O phonons have very similar energy range as Si phonons which we know are a source of scattering centers that degrade the channel mobility. Therefore, these data indirectly support Fischetti's "remote phonon scattering model" [10].

Figure 8 also shows features corresponding to Hf-Si-O and Hf-O phonons. Since these phonons have much higher energies than kT at room temperature, they are not effective scattering centers at room temperature.

IETS can also be used to probe electronic traps in gate dielectrics. Figure 9 shows stress-induced trap features in a set of $Al/HfO_2/Si$ samples, where one can see the increase of trap density as the electrical stress time increases. We have found that it's possible to reveal the spatial locations and energies of these traps by analyzing the IETS spectra in both voltage polarities [13], and the details of which will be presented at the conference.

Acknowledgment

The author would like to thank former and current graduate students, Wenjuan Zhu, Whye-Kei Lye, Wei He, and Miaomiao Wang, for their contributions to this paper, and SRC and Sematech for their financial support.

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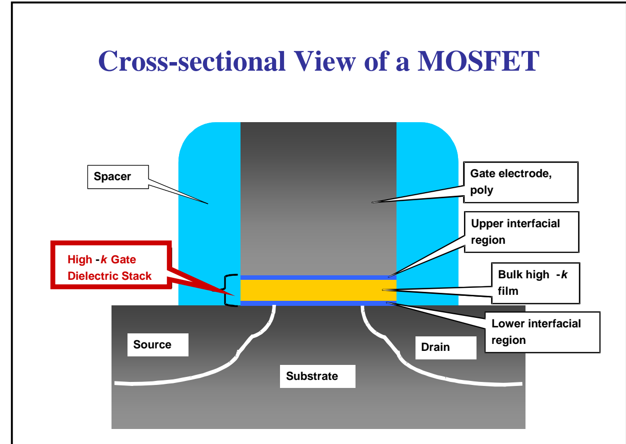

Fig.1 Cross-sectional view of a MOSFET with high-k gate dielectric

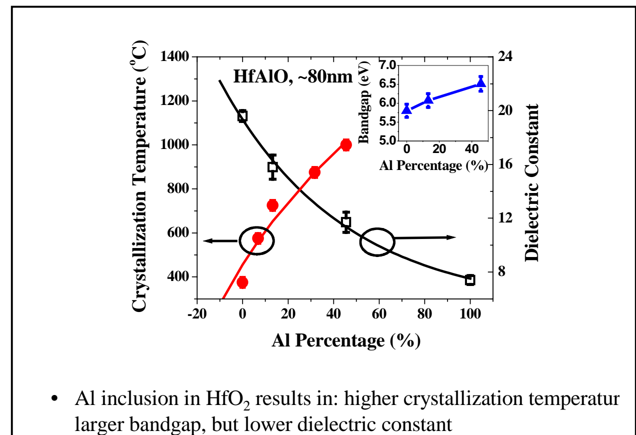

Fig.2 Crystallization temperature, bandgap, and dielectric constant as a function of Al concentration.

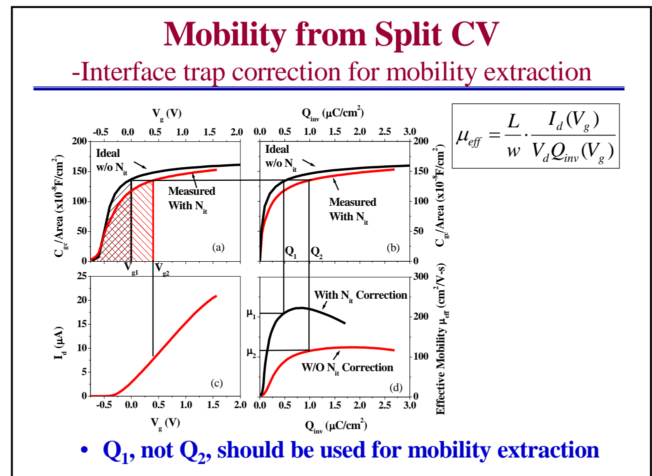

Fig.3 Illustration of the modified split CV method for extracting the carrier concentration and channel mobility.

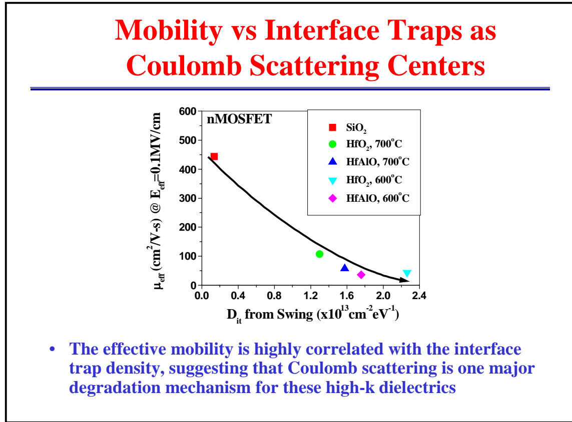

Fig. 4 Channel mobility is strongly correlated to the interface trap density

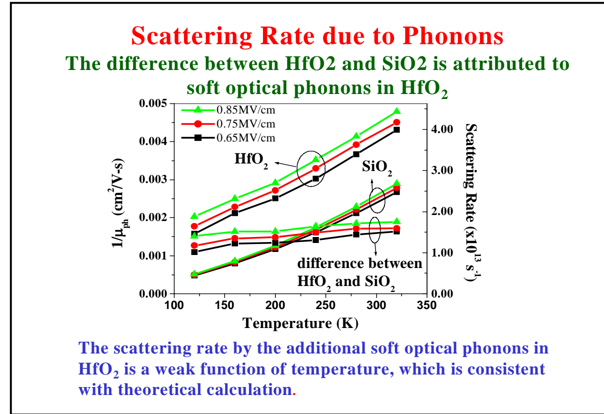

Fig.5 Additional phonon scattering in HfO2-gated MOSFET is attributable to soft optical phonons in HfO_2.

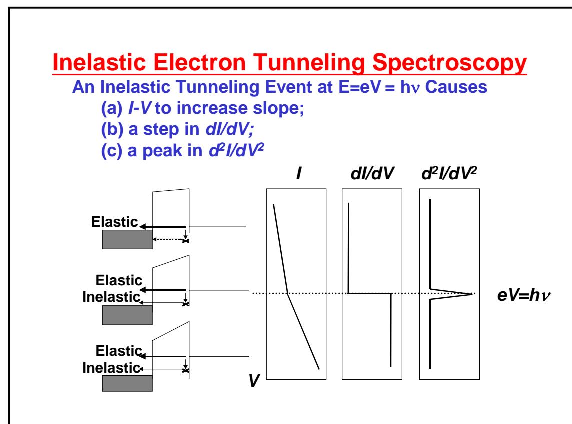

Fig.6 Inelastic interaction causes a slope increase of I-V, a step in dI/dV, and a peak in 2nd derivative, all occurring at the voltage corresponding to the characteristic energy.

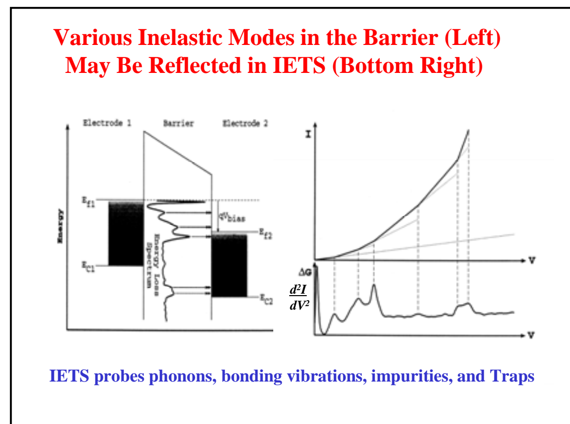

Fig.7 Typical IETS spectrum (lower right curve) reveals the various inelastic modes depicted in the energy diagram on the left.

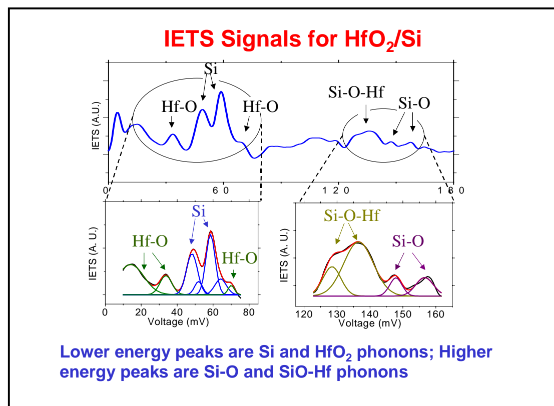

Fig. 8 IETS spectrum for Al/HfO2/Si sample, revealing Hf-O phonons between 15 and 75 meV, and Si-O, Si-Hf-O phonons at higher energies.

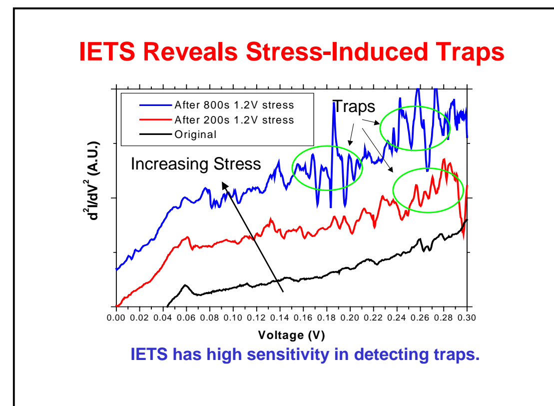

Fig. 9 IETS spectrum for Al/HfO2/Si sample, showing stress-induced trap features.

High-k Gate Dielectrics for Future CMOS Technology

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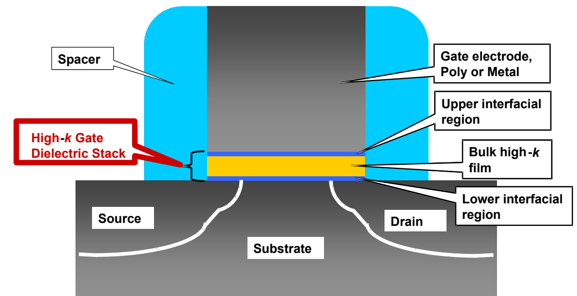
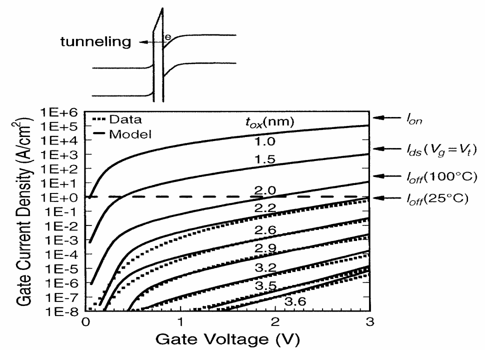
MOS Transistor Gate Stack



ITRS Gate Stack Parameters

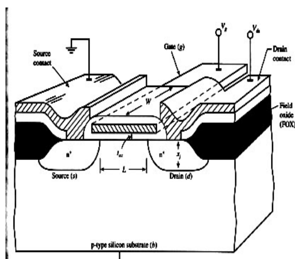
Year of Production	*2004*	*2005*	*2006*	*2007*	*2010*
DRAM ½ Pitch	*90 nm*	*80 nm*	*70 nm*	*65 nm*	*45 nm*
Physical Gate Length MPU/ASIC (nm)	37	32	28	25	18
Equivalent physical oxide thickness for MPU/ASIC Tox (nm)	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8
Gate dielectric leakage at 100˚C (mA/μm) High-performance	0.1	0.3	0.7	1.0	3.0
Equivalent physical oxide thickness for low standby power Tox (nm)	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	0.9-1.3
Gate Dielectric Leakage (pA/μm) LSTP	1.0	1.0	1.0	1.0	3.0
Thickness control EOT (% 3s)	<± 4	<± 4	<± 4	<± 4	<± 4

Tunneling current increases exponentially with decreasing oxide thickness



Taur, IEEE Spectrum, July 1999

Metal/Oxide/Semiconductor (MOS) Transistor



- **Speed Increases with Charge Carrying Capacity, Q.**

  Q = CV

  where **C = ε/d** (ε: Dielectric constant; d: Oxide thickness)
- **To Increase C:**
  - **Decrease d**
  - **Increase ε (ε = k ε_o)**

  ⇒High-k dielectrics

First viable high-k gate dielectric – Si_3N_4

Yale University

Thermal Oxide	**Silicon Nitride**
ε_{ox}: 3.9	ε_{ni}: 7.8
2 nm	4 nm

$C = \frac{\varepsilon}{T}$

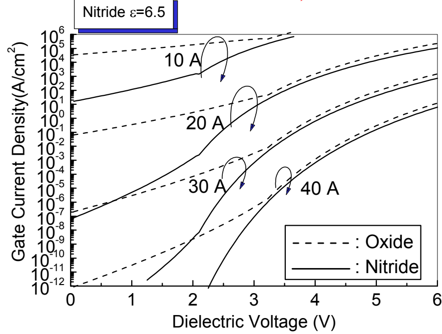
$J \propto \exp(-c \cdot \phi_b^{\frac{3}{2}} \cdot \frac{T_{ox}}{V_{ox}})$

$\varepsilon_{ni} = 2.\varepsilon_{ox}$

$T_{physical} = 2.T_{EOT}$

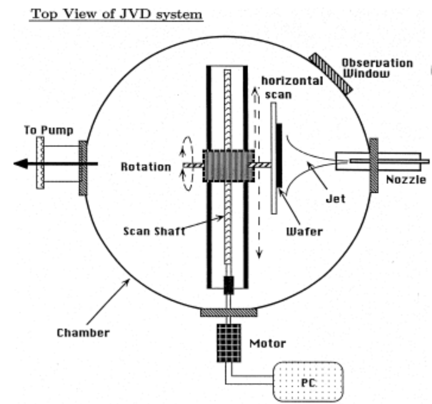
4 nm Silicon Nitride has 2nm of Equivalent Oxide Thickness (EOT)

Silicon Nitride Shows Lower Gate Tunneling Currents (Theoretical)

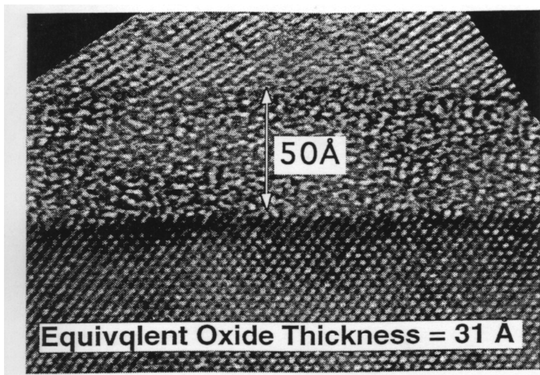


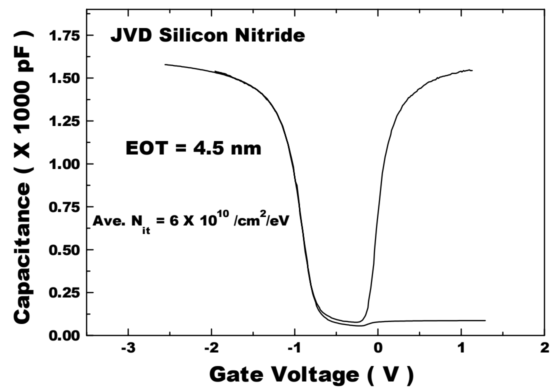
Yale Group, VLSI Technology Symposium, June 1995

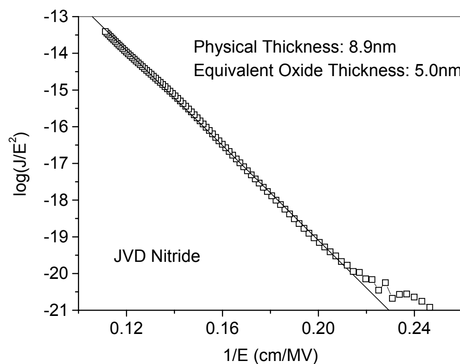
Top View of JVD System



JVD Silicon Nitride on Si

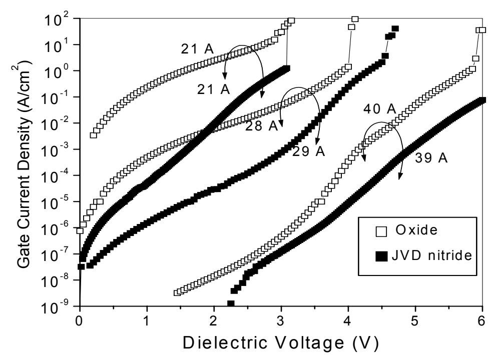




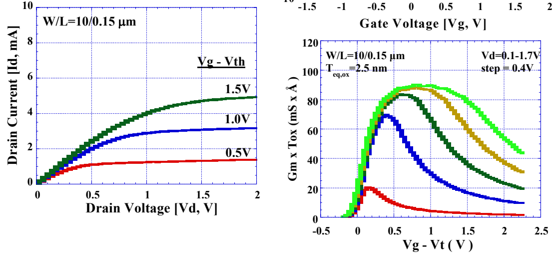


Fowler-Nordheim Plot of Current Through JVD Silicon Nitride

Comparison of Measured Gate Leakage Current



Transistor Characteristcs of Sematech's 0.15 um Technology with 2.0 nm JVD Silicon Nitride

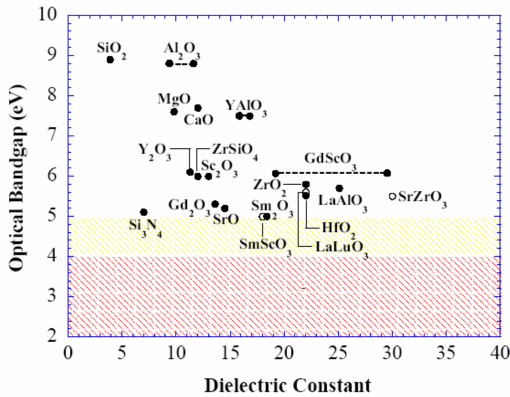


Karamcheti et al., MRS Fall Meeting, Nov. 1999

Dielectric Constants of Some High-k Materials

Table 2. Candidates for High-k materials

Material	k	$HfAl_xO_y$	10-15
NO stack	5-6	$HfSi_xO_yN_z$	10-15
Al_2O_3	8-9	ZrO_2, HfO_2	20-30
$HfSi_xO_y$	10-15	Lanthanide Oxides	15-30



D.G. Schlom and J.H. Haeni, *MRS Bulletin* 27 (March 2002) 198-204.

Challenges of High-k Dielectrics

- EOT Control
- Thermal Stability
- Mobility & Threshold Voltage
- Trapping Induced Instability

Challenges of High-k Dielectrics

- EOT Control
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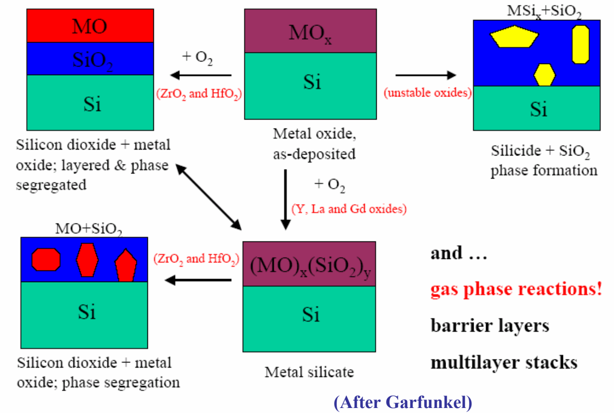
Interface reactions: structure & phase, kinetics/thermodynamics mixing/segregation, amorphous/crystalline, growth/reduction



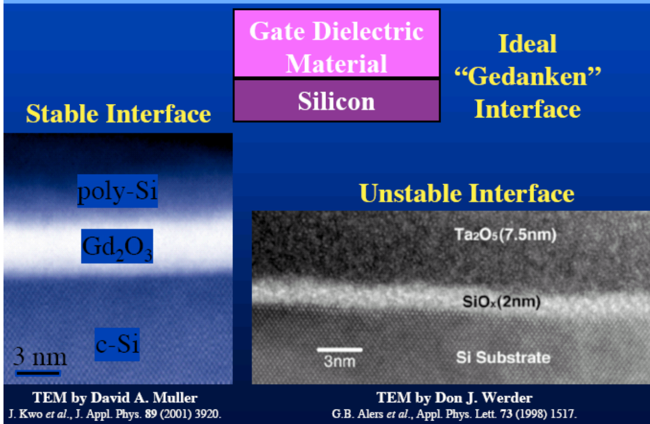
and …

gas phase reactions!

barrier layers

multilayer stacks

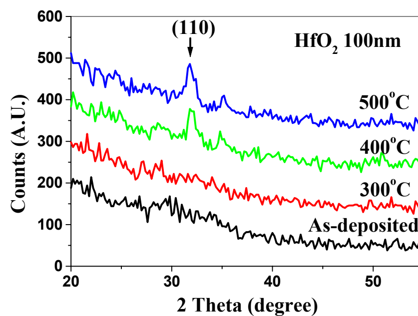
(After Garfunkel)



Challenges of High-k Dielectrics

- EOT Control
- **Thermal Stability**
- Mobility & Threshold Voltage
- Trapping Induced Instability

HfO_2 crystallizes between 300 and 400°C



Thermal stability of high-*k* oxides

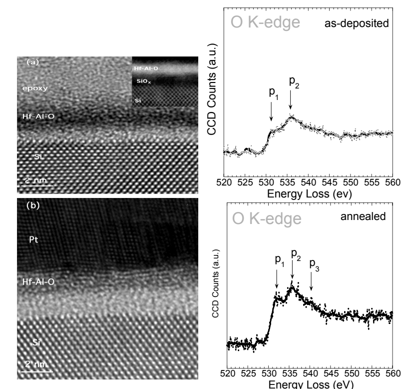
Hf-aluminate films grown at RT by jet-vapor deposition (T.P.Ma, Yale U.) w. 6.8 at% Al

As-deposited film:

- Low leakage and low EOT
- Amorphous
- Thin interfacial SiO_2 layer
- Broad ELNES

Annealed film (700 °C/N_2):

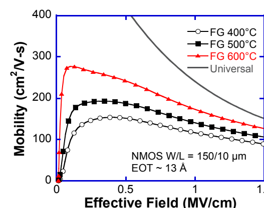
- Leaky, increased EOT
- Partially crystallized
- Thicker interfacial SiO_2 layer
- Narrower ELNES

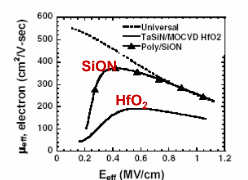


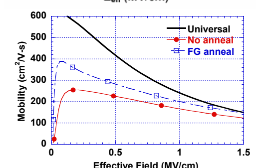
Challenges of High-k Dielectrics

- EOT Control
- Thermal Stability
- **Mobility & Threshold Voltage**
- Trapping Induced Instability

Degradation of Channel Mobility in High-k Gated MOSFETs





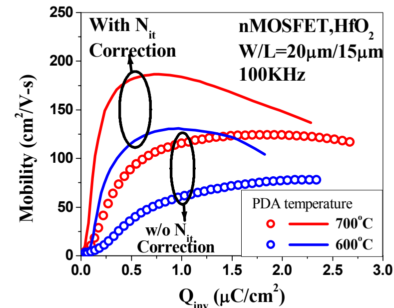


Common Errors in Measuring High-k Gated MOSFET Mobility

- **Trapping causes overestimation of carriers and thus underestimation of mobility**
- **High gate leakage current that results in underestimation of mobility at high fields**

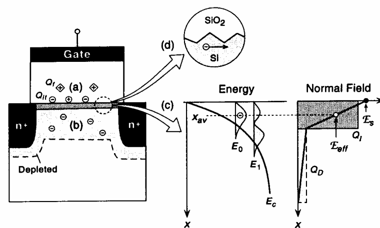
Mobility of HfO_2-Gated MOSFET

-Effect of Trapping



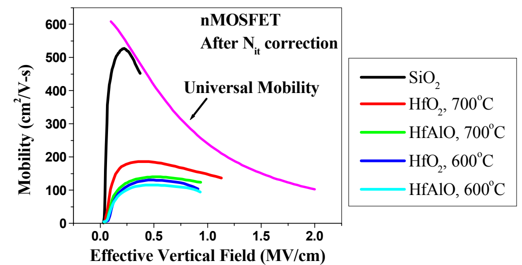
- **Corrected curves are higher**
- **Both show a peak, as predicted by scattering theory**

Scattering mechanisms



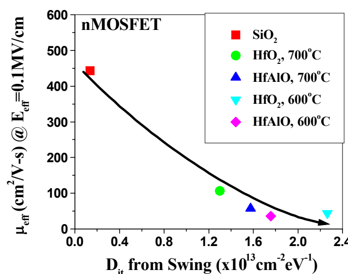
(a) Coulomb scattering due to trapped charge in dielectrics
(b) Coulomb scattering due to ionized impurities in depletion layer
(d) Surface roughness scattering
(e) Phonon scattering due to lattice vibration

Mobility of nMOSFET with various gate dielectrics



- The mobility of nMOSFET with SiO_2 are much higher than the one of HfO_2 and HfAlO.
- The mobility of nMOSFET with HfO_2 or HfAlO annealed at 700°C are higher than the one annealed at 600°C

The relation between mobility and interface trap density



- The higher the interface trap density, the lower the effective mobility, indicating that coulomb scattering is one major degradation mechanism of these high-k dielectrics

Remote Phonon Scattering

JOURNAL OF APPLIED PHYSICS VOLUME 90, NUMBER 9 1 NOVEMBER 2001

Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering

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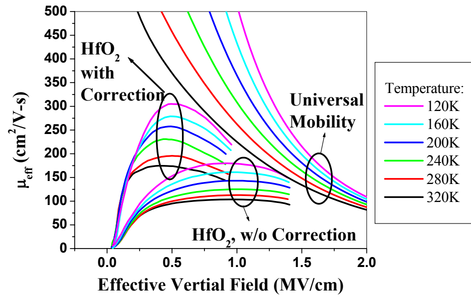
(Received 18 June 2001; accepted for publication 26 July 2001)

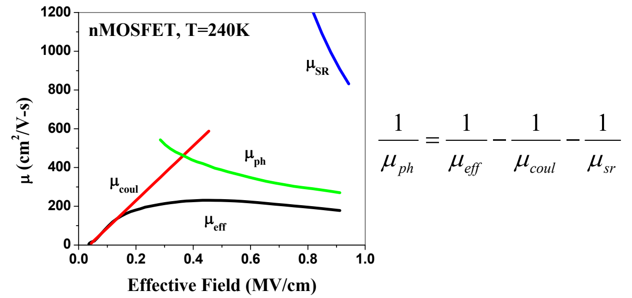
The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal–oxide–semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for "SiO_2-equivalent" thicknesses ranging from 5 to 0.5 nm. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1405826]

Temperature dependence of mobility



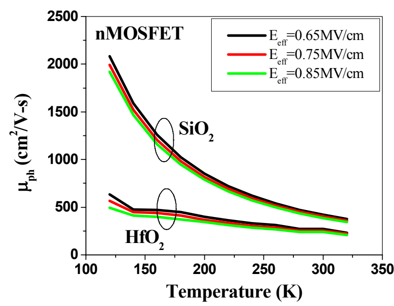
- Effective mobility for HfO_2 is lower than universal mobility even after interface correction.

Extraction of mobility limited by phonon scattering



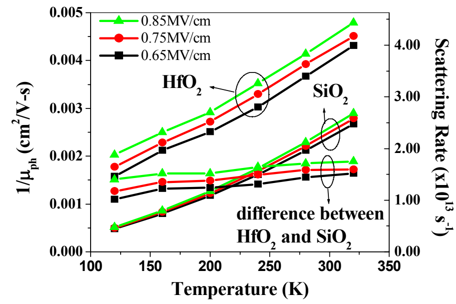
- The mobility limited by phonon is extracted according to Matthiessen's rule.

Temp. dependence of mobility limited by phonon scattering



- Mobility limited by phonon scattering for HfO_2 sample is much lower than that for SiO_2 sample

The difference between HfO2 and SiO2 is attributed to soft optical phonons in HfO_2



- The scattering rate by the additional soft optical phonons in HfO_2 sample is a weak function of temperature, which is consistent with theoretical calculation.

The scattering rate due to optical phonons:

$$\frac{1}{\tau_{op}} \propto [N_R + (N_R+1)u(E-\hbar\omega)]$$

Where $N_R = \dfrac{1}{e^{\hbar\omega/kT}-1}$ is phonon occupation number

u(x) is the unit step function.

1) For $\hbar\omega < E$

$$\frac{1}{\tau_{op}} \propto (2N_R+1) = \frac{e^x+1}{e^x-1} \quad where\ x = \frac{\hbar\omega}{kT}$$

When $\hbar\omega << kT$ $\quad \dfrac{1}{\tau_{op}} \propto T$

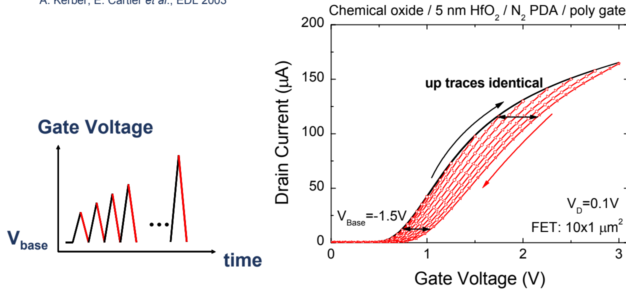
2) For $\hbar\omega > kT$ $\quad \dfrac{1}{\tau_{op}}$ ≈constant

Challenges of High-k Dielectrics

- EOT Control
- Thermal Stability
- Mobility & Threshold Voltage
- Trapping Induced Instability

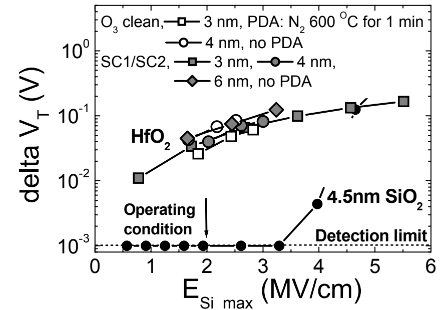
Drain current instability

A. Kerber, E. Cartier *et al.*, EDL 2003



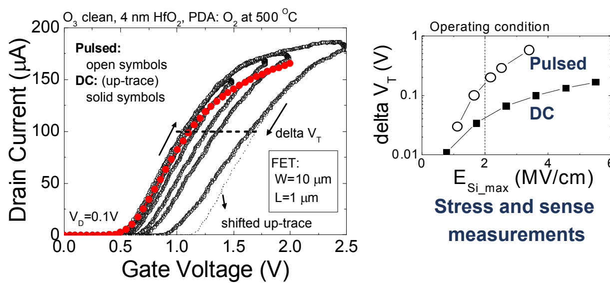
- Instability is unacceptably large

Vt-instability in scaled SiO_2/HfO_2 stacks: Comparison to SiO_2



- All SiO_2/HfO_2 stacks studied show comparable instability
- Instability is much larger than for SiO_2 control

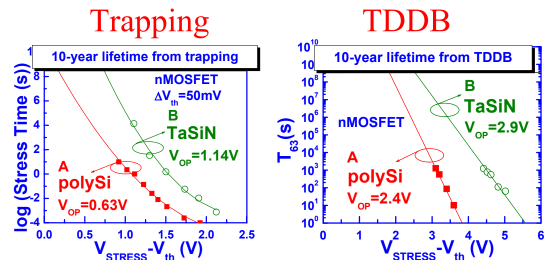
Pulsed and 'DC' measurements



Stress and sense measurements

- V_t instability due to charging is underestimated by 'DC' measurements
- Charging is leaking out during slow measurements
- For application, pulsed result more relevant

Lifetime Extraction Charge Trapping vs TDDB



- It is charge trapping rather than TDDB that limits device lifetime.

Examples of Innovative Approaches

- Ultra Rapid Thermal Annealing
- Inelastic Electron Tunneling Spectroscopy (IETS)
- MAD

Examples of Innovative Approaches

- Ultra Rapid Thermal Annealing
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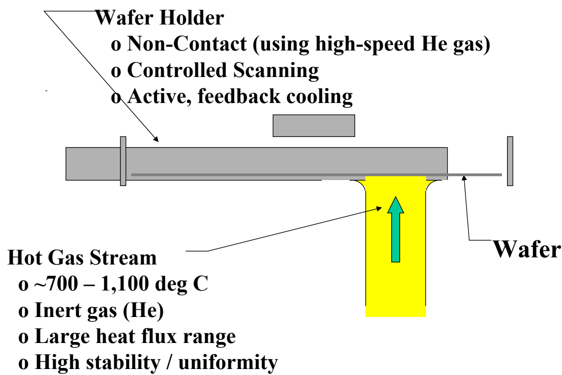
Atmospheric Hot Gas Annealing Concept

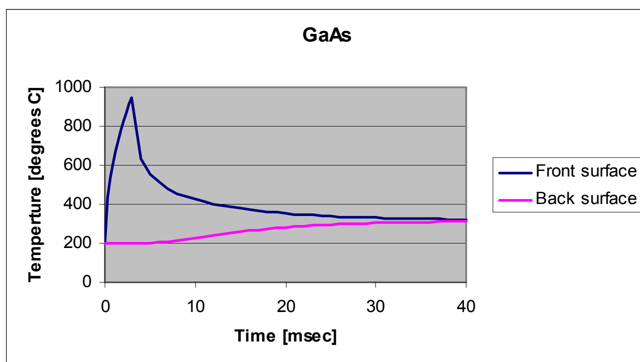


Inherent Advantages for Hot Gas RTP

- Heat transfer by gas conduction, not surface topography/material dependent
- Very Rapid Heating
- Very Rapid Cool-down

Wafer Heating & Cooling

at $5x10^7$ W/m² for 3msec



Examples of Innovative Approaches

- Ultra Rapid Thermal Annealing
- Inelastic Electron Tunneling Spectroscopy (IETS)
- MAD

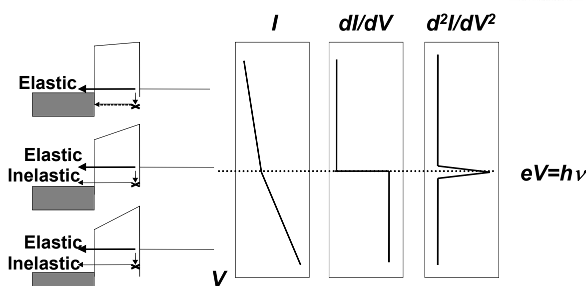
Inelastic Electron Tunneling Spectroscopy

An Inelastic Tunneling Event at E=eV = hν Causes

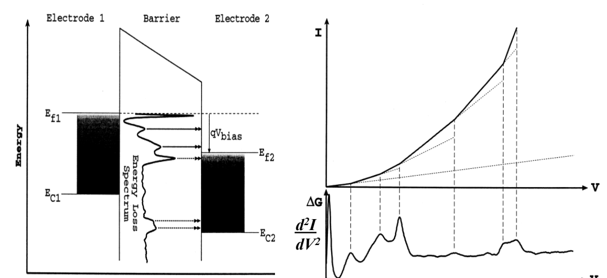
(a) *I-V* to increase slope;

(b) a step in *dI/dV;*

(c) a peak in *d²I/dV²*



Various Inelastic Modes in the Barrier (Left) May Be Reflected in IETS (Bottom Right)

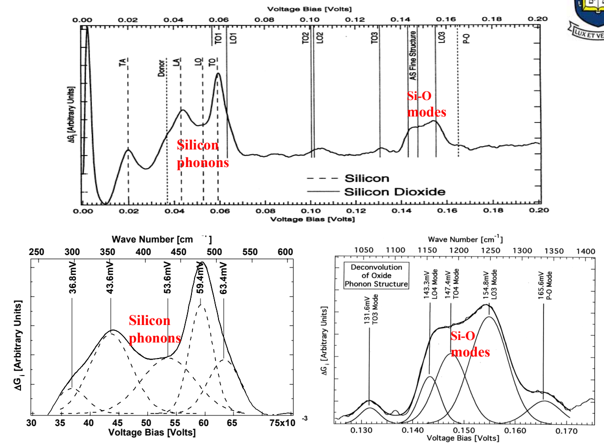


IETS probes phonons, bonding vibrations, impurities, and Traps

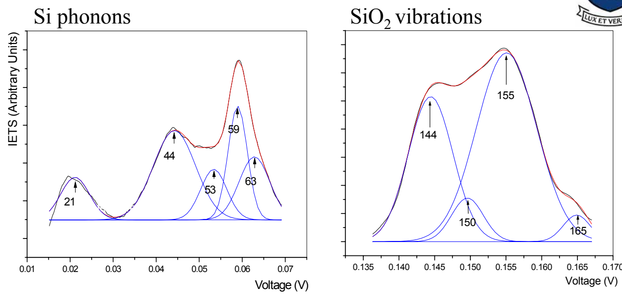
Interactions Detectable by IETS

- Substrate Silicon Phonons
- Gate Electrode Phonons
- Dielectric Vibrations (Phonons)
- Impurity Bonding Vibrations
- Trap States

IETS Spectrum of SiO_2/Si

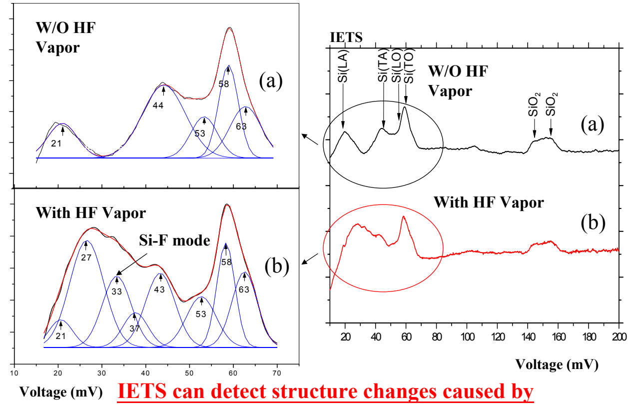


Si phonons and SiO_2 vibration modes



21 mV: Si TA mode
44 mV: Si LA mode
53 mV: Si LO mode
59 mV: Si TO mode

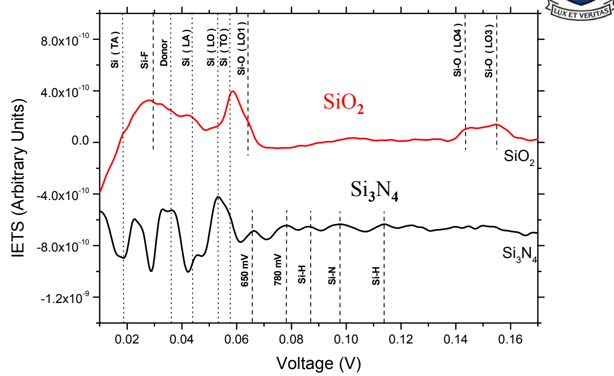
63 mV: Si-O LO1 mode (Rocking)
144 mV: Si-O AS1 mode (Asymmetric Stretch)
150 mV: Si-O AS2 mode (Asymmetric Stretch)
155 mV: Si-O LO3 mode (Symmetrric Stretch)
165 mV: P-O mode



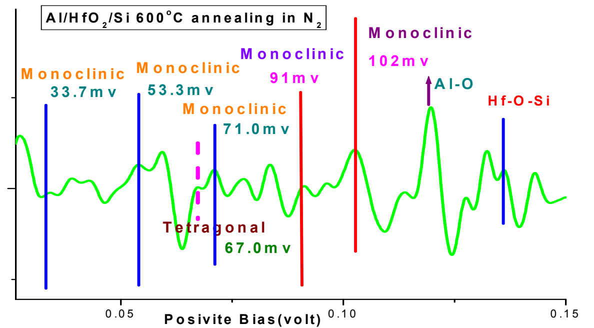
IETS can detect structure changes caused by different processing conditions.

(a) SiO_2/Si without HF vapor pre oxidation cleaning
(b) SiO_2/Si with the HF vapor pre oxidation cleaning

IETS of Thermal SiO_2/Si and CVD Si_3N_4/Si



IETS of $Al/HfO_2/Si$



Theoretical (LDA and GGA) and experimental (Raman and IETS) of phonon modes in HfO_2

Modes (cm-1)	Monoclinic Bu	Monoclinic Ag,Bg	Monoclinic Bg	Monoclinic Ag	Monoclinic Bg	Moniclinic Bg	Tetragonal
LDA	261	423,424	570	738	821	667	536
GGA	252	382,385	529	640	716	627	
Raman	256	382,398	551	672	773	640	
IETS	270 (33.7mv)	411 (51mV)	572 (71mv)	725 (91mv)	822 (109mv)	637 (79mv)	536 (66.4mv)

---Xinyuan Zhao and David Vanderbit, Physical Review B,vol. 65, 2002

Remote Phonon Scattering

JOURNAL OF APPLIED PHYSICS VOLUME 90, NUMBER 9 1 NOVEMBER 2001

Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering

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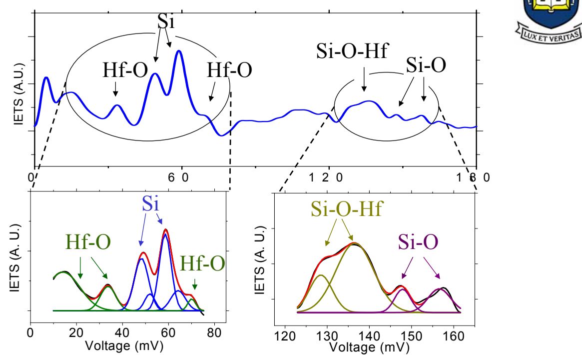
The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal–oxide–semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for "SiO_2-equivalent" thicknesses ranging from 5 to 0.5 nm. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1405826]

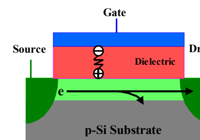
IETS Signals for HfO_2/Si



Lower energy peaks are Si and HfO_2 phonons; Higher energy peaks are Si-O and SiO-Hf phonons

Mobility Reduction due to Soft Phonon Scattering

Gate Dielectric	SiO_2	HfO_2
Bond strength	Strong Si-O bond	Weak Hf-O bond
Optical phonon energy (meV)	138	34, 48, 70
Rate of emission/absorption phonon	Low	High
Static permittivity $\varepsilon_{ox}^0/\varepsilon_o$	3.9	22.0
Optical permittivity $\varepsilon_{ox}^\infty/\varepsilon_o$	2.5	5.03
Electron phonon coupling strength	Low	High
Mobility limited by remote phonon scattering	High	Low



HfO_2 gated MOSFET might have reduced mobility due to soft phonon scattering.

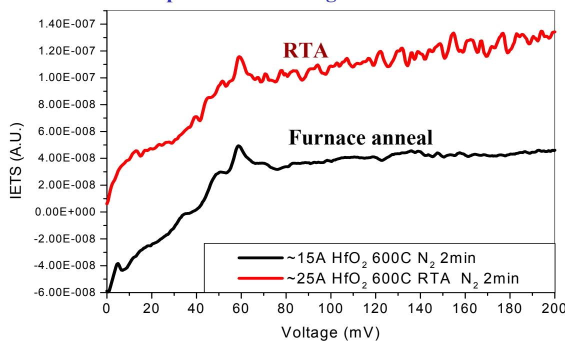
A) Phonon energies close to kT at room temp.

B) Scattering strength $\propto \dfrac{\varepsilon_{ox}^0 - \varepsilon_{ox}^\infty}{(\varepsilon_{si}^\infty + \varepsilon_{ox}^\infty)(\varepsilon_{si}^\infty + \varepsilon_{ox}^0)}$

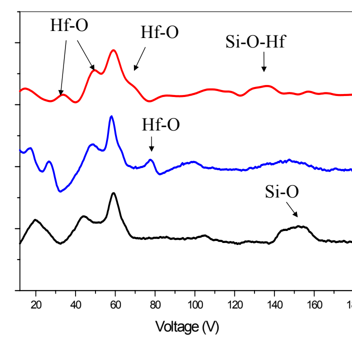
[M. Fischetti, et.al, J. Appl. Phys.,Vol.90, p4587, 2001]

IETS sensitive to process variations for Al/HfO_2/Si structure (1)

Post-deposition annealing: Furnace vs. RTA



IETS sensitive to process variations for Al/HfO_2/Si structure (2)



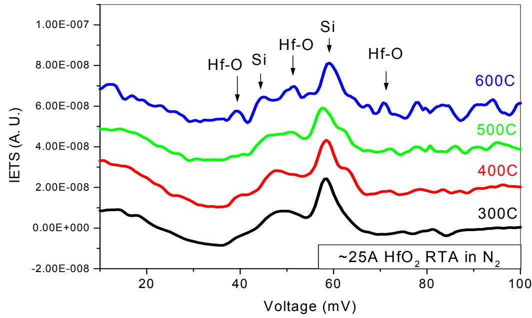
~15Å HfO_2
N_2 600C 3mins

~10Å HfO_2
N_2 600C 3mins + WV 600C 2mins

Thermal Oxide Reference

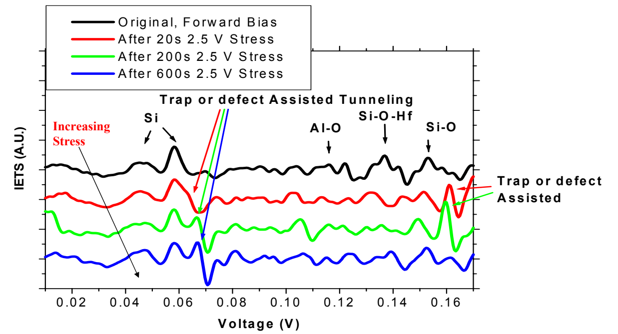
IETS sensitive to process variations for $Al/HfO_2/Si$ structure (3)

- Hf-O peaks stronger with increasing PDA temperature
- Linked to more HfO_2 crystallization at higher temperatures.

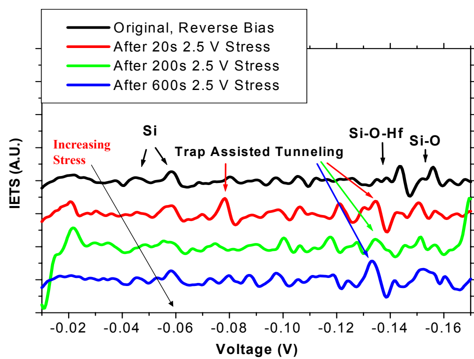


Voltage Stress Induced Effect

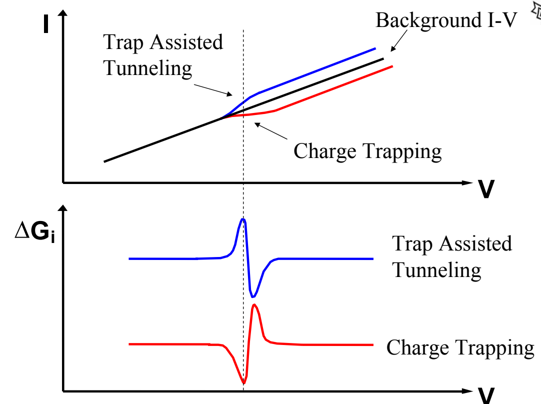
Features at 0.07V and 0.16V indicate trap assisted tunneling.



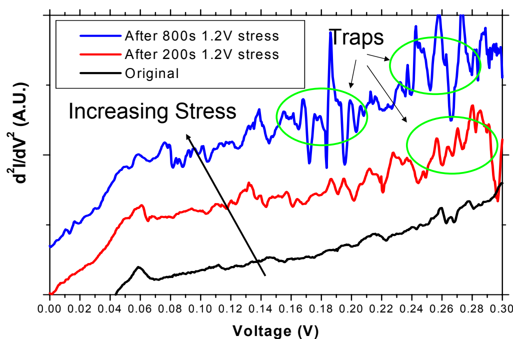
Voltage Stress Induced Effect (Reverse Bias)



Trap Related Effect from IETS

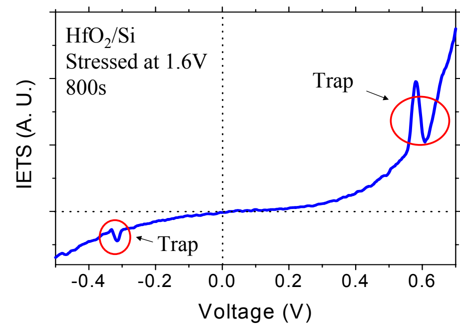


IETS Reveals Stress-Induced Traps



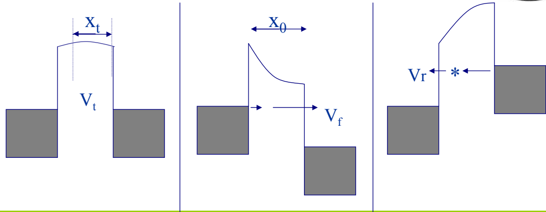
IETS has high sensitivity in detecting traps.

Strong Trap Assisted Tunneling Effect Revealed by IETS



Forward-bias trap features are stronger than reverse-bias ones, due to asymmetry of the barrier.

Determining Trap Energy and its Physical Location from Forward and Reverse IETS

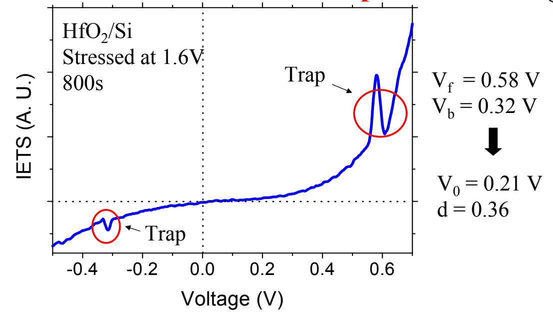


x_t is the physical location of the trap (assume total physical thickness is x_0).
eV_t is the trap energy above the Fermi level (at zero bias).
V_f is the forward bias voltage required for the Fermi level to reach the trap.
V_r is the reverse bias voltage required for the Fermi level to reach the trap.

Assume non-uniform dielectric constant: $\varepsilon=\varepsilon(x)$.

$V_t = V_f V_r / (V_f+V_r)$
$d_t = d_0 V_f / (V_f+V_r)$ where $d_0 = \int_0^{x_0} dx/\varepsilon(x)$, $d_t = \int_0^{x_t} dx/\varepsilon(x)$

Trap Energy and its Physical Location for a Particular Trap



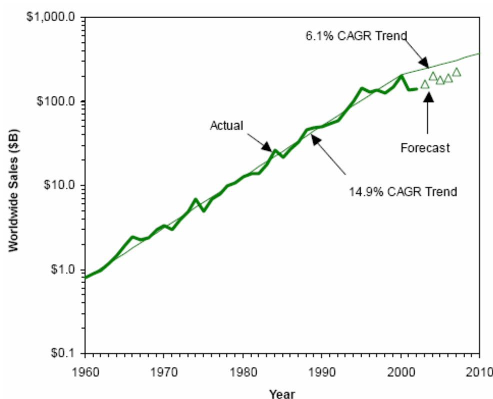
The EOT of the dielectric is ~2.5 nm. ➡ The trap is located ~ 0.9 nm from the dielectric/Si interface

Conclusion

Extensive R&D Efforts for High-k Gate Dielectrics Are Needed to Realize

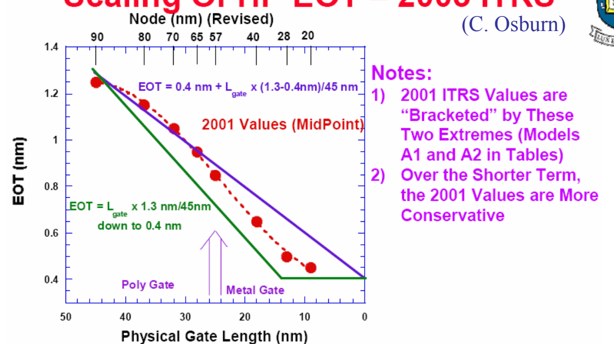
- EOT << 1 nm
- Low Gate Leakage Current
- Good Thermal Stability
- Desired V_T for Both Channels
- High Drive Current and Transconducttance
- Good Reliability

Worldwide IC Sales



Scaling Of HP EOT – 2003 ITRS

(C. Osburn)



Aggressive - EOT Scales with L_{gate} Until it Hits its Physical Limit (0.4 nm?); This Constant Field Approach is Essentially the one used by PIDS

Conservative – EOT Scales Linearly with EOT down to its Limit; Recommendation of the FEP SubTWG

N-Channel and P-Channel Transistors with < 2nm (EOT) of RTCVD Silicon Nitride as Gate Dielectric

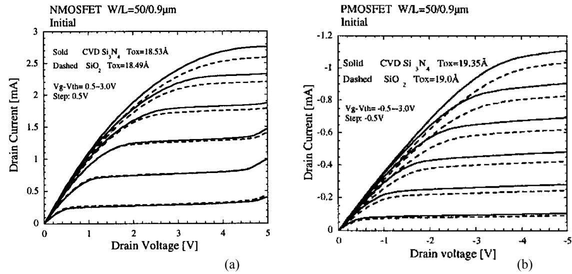
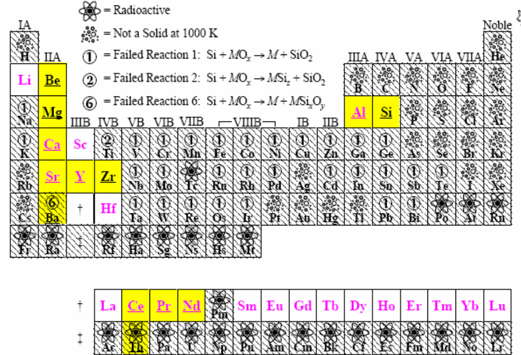


Fig. 12 Drain current characteristics of transistor with <2nm (EOT) of RTCVD silicon nitride as gate dielectric: (a) NMOSFET, (b) OMOSFET [12].

Song, et al., IEDM Technical Digest, Dec. 1998

Oxides Thermodynamically Stable in Contact with Silicon



K.J. Hubbard and D.G. Schlom, "Thermodynamic Stability of Binary Oxides in Contact with Silicon," *Journal of Materials Research* **11** (1996) 2757-2776.

Oxide heats of formation

(Adapted from E. Garfunkel)

- Relative oxide stability (oxygen affinity)
- Do the phases mix ???
- Suboxide existance and stability ???

Heats of formation of oxide (ΔH_f^0 in kJ per mole O) [a]	Metal
>0	Au
0 - −50	Ag, Pt
−50 - −100	Pd
−100 - −150	Rh
−150 - −200	Ru, Cu
−200 - −250	Re, Co, Ni, Pb
−250 - −300	Fe, Mo, Sn, Ge, W
−300 - −350	Rb, Cs, Zn
−350 - −400	K, Cr, Nb, Mn
−400 - −450	Na, V
−450 - −500	Si ←
−500 - −550	Ti, U, Ba, Zr
−550 - −600	Al, Sr, Hf, La, Ce
−600 - −650	Sm, Mg, Th, Ca, Sc, Y

for the most stable oxide of the metal.

Mobility measurement

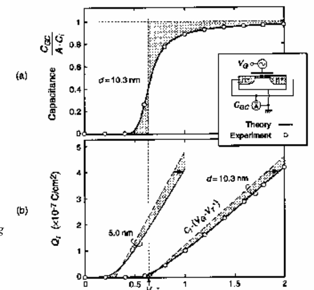
Effective mobility:

$$\mu_{eff} = \frac{L}{w} \cdot \frac{I_d(V_g)}{V_d Q_{inv}(V_g)}$$

Inversion charge density:

Conventional $Q_{inv} = C_{ox}(V_g - V_T)$

Split CV: $$Q_{inv} = \int_{-\infty}^{Vg} C_{gc}(V_g) dV_g$$

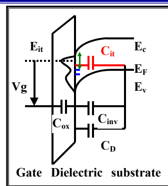


- **C_{gc} is not step function of V_g at V_T => need split CV**

Standard split CV method is inadequate for high-k dielectrics with high N_{it}

Problem 1. N_{it} can respond to ac signal

$$C_{gc} = \frac{C_{ox}(C_{inv} + C_{it})}{C_{ox} + C_{inv} + C_D + C_{it}}$$

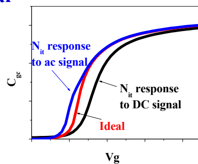


Solution: Higher frequency for split CV

Problem 2. N_{it} can respond to dc signal

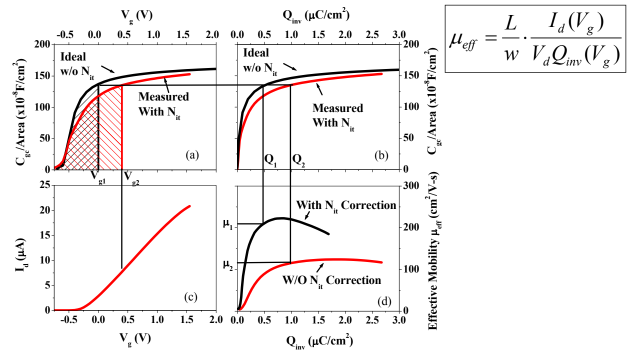
$$dV_g = -(dQ_{inv} + dQ_{trap}) / C_{ox}$$

Solution ?



Mobility from Split CV

-Interface trap correction for mobility extraction



$$\mu_{eff} = \frac{L}{w} \cdot \frac{I_d(V_g)}{V_d Q_{inv}(V_g)}$$

- **Q_1, not Q_2, should be used for mobility extraction**

Mobility from Split CV (cont'd)

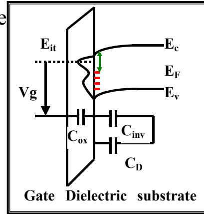
-Interface trap correction for mobility measurement

At high frequencies, gate-channel capacitance

$$C_{gc} = \frac{C_{ox}C_{inv}}{C_{ox} + C_{inv} + C_D}$$

where $C_{inv} = \frac{dQ_{inv}}{d\psi_s}$

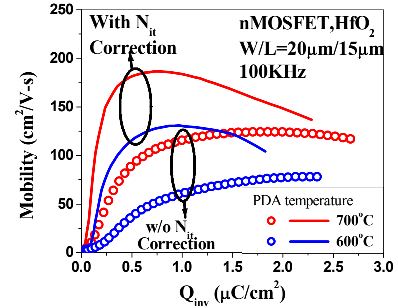
is the same with or w/o interface traps for the same Q_{inv}



At same C_{gc}, Q_1 extracted from ideal C_{gc} and Q_2 from measured C_{gc} contain the same amount of mobile inversion charge, while Q_2 contains extra interface trapped charge

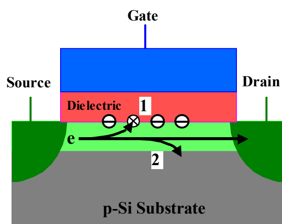
Mobility of HfO_2-Gated MOSFET

-Effect of Interface Traps



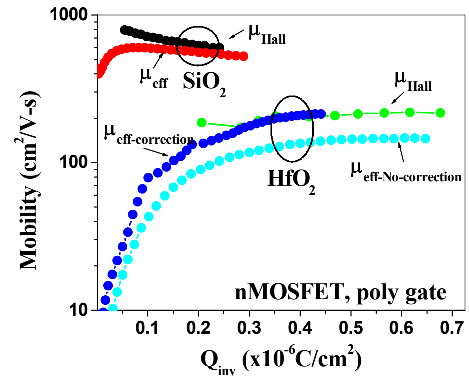
- **Corrected curves are higher**
- **Both show a peak, as predicted by scattering theory**

Difference between interface traps causes mobility "underestimation" and mobility "degradation"

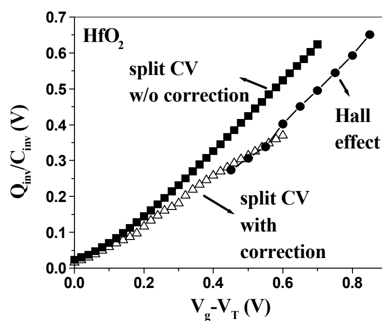


- 1: Charge trapping causes carrier loss and mobility underestimation
- 2: Trapped charge causes Coulomb scattering and mobility degradation

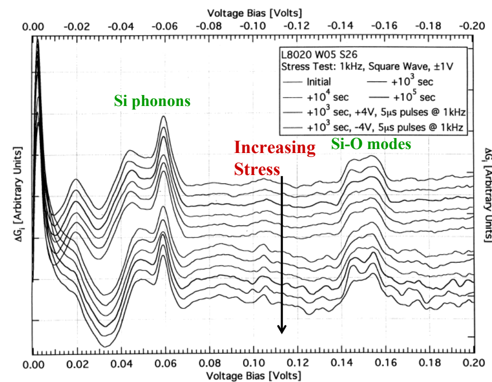
Hall Mobility *vs* Effective Mobility from split CV



Normalized Inversion Charge Density

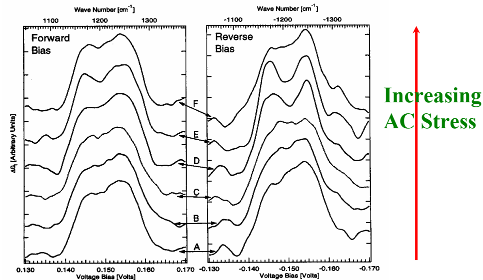


Electrical Stress Alters the Si-O Modes But Leaves the Si Phonons Unchanged



IETS can detect changes caused by elctrical stress

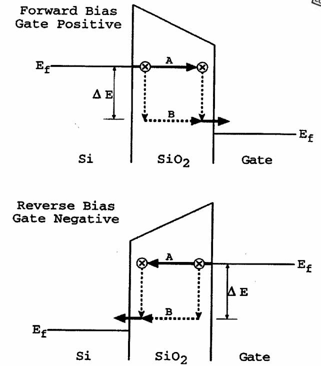
IETS reveals changes in SiO_2/Si interface after AC stress.
Possible explanation is that AC stress breaks weak bonds and cause positive charges at the interface. The positive charges will modify the bonding structure for SiO2 near the interface.



A:Initial; B-D:After 10^3,10^4,10^5 sec $\pm$0.5V 1kHz square wave stress;
E:After 10^3 sec +2V 1us 1kHz pulses;
F: After 10^3 sec -2V 1us 1kHz pulses.

Bias Polarity Dependence

Electrons have higher probability to interact with a vibration located near the positively biased electrode.



Bias Polarity Dependence of IETS for Al/HfO_2/Si

- **Results suggest significantly different microstructures near Al-HfO_2 interface and Si-HfO_2 interface.**
- **HfO_2/Si interface is more SiO_2-like.**
- **HfO_2/Al interface is more HfO_2-like.**