Sub-20nm Novel Silicon based transistors

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Aggressive MOSFET scaling faces the challenges of limited Ion/Ioff ratio and severe short channel effects. To overcome these problems, new device configurations made feasible by small dimensions and new materials need to be explored. In this paper, novel devices incorporating silicon and germanium are presented. These silicon and germanium based asymmetric source injection devices with superior performance have the potential to alleviate the scaling challenges for sub-25nm nodes.

1. Schottky Barrier MOSFET

Schottky barrier MOSFETs which use fully silicided source/drain junctions have been proposed for future very-short-channel devices 0. The major advantage is the formation of ultra shallow junctions with very low resistively. In this abstract, a novel asymmetric Schottky Tunneling Source MOSFET is introduced. The operating principle of the STS MOSFET utilizes the concept of gate controlled Schottky barrier tunneling between a metal and a semiconductor. Fig. 1 shows the band diagram along the surface of the channel region at different gate voltages for a Schottky source with a barrier height (φ_b) of 0.45eV. When the gate voltage is sufficiently low the tunneling distance of the Schottky junction is high as well as the number of states that electrons can tunnel into is small. Hence the current injection is limited by the tunneling resistance only. As the gate voltage increases, the tunneling distance reduces and the number of states the electrons in the metal source can tunnel into increases thereby reducing the tunneling resistance. Fig 2a shows that as gate oxide thickness reduces, there is a marked improvement in STS MOSFET sub-threshold characteristics as well as I_{ON}. A sub-threshold swing of ~130mV/dec is obtained for EOT = 20Å and ~70mV/dec is obtained for EOT = 5Å. This suggests that the sub-threshold swing is a strong function of t_{OX} as opposed to diffusion barrier transport. However, the sub-threshold swing obtained due to gate controlled tunneling is always degraded as compared to best possible diffusion limited sub-threshold swing (~60mV/dec at room temperature); even though STS has excellent DIBL and V_{TH} roll-off characteristics. To further improve the performance of STS transistor, Schottky FETs with asymmetric source/drain pocket is proposed. Fig 2b shows that as the source pocket is made n-type with increasing dopant density, the tunneling distance (and therefore tunneling resistance) reduces for a given gate voltage and the threshold voltage also reduces. But, the sub-surface conduction goes up thereby increasing the off current. However, when the pocket is made p-type, a region of high threshold is created near the source. This reduces the subsurface conduction considerably resulting in low I_{OFF}. I_{ON} on the other hand is not degraded since the band-bending increases due to the p-pocket. Therefore, the tunneling width remains about the same as conventional STS transistor. The n^+ pocket on the drain side forms a low resistance contact between the channel and the drain, eliminating the potential drop at the drain side due to the presence of a Schottky barrier.

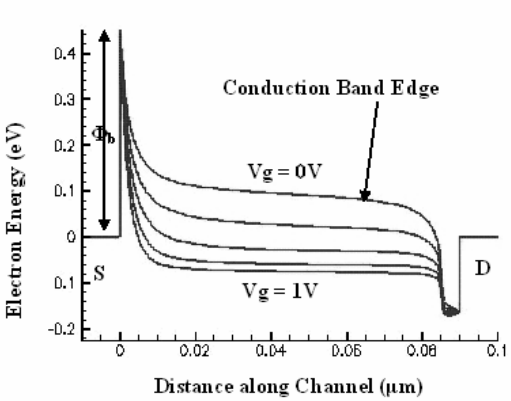

Figure 1 Conduction Band Edge profile along the channel for different gate voltages. φ_b=0.45eV.

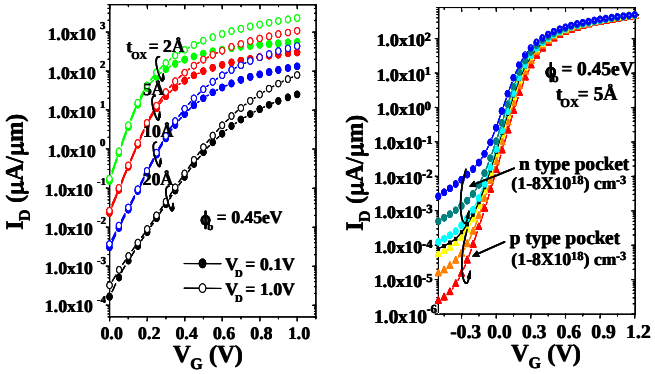

Figure 2 (a) I_D-V_G characteristics of devices with different gate oxide thicknesses for a given φ_b of 0.45eV. N_{BULK} = $1X10^{17}cm^{-3}$. (b) I_D-V_G characteristics with different pocket doping. N_{BULK} = $1X10^{17}cm^{-3}$, t_{SI} = 60nm and V_D = 0.1V.

2. Tunnel Source MOSFET

To further improve the I_{ON}/I_{OFF} ratio, we propose the Tunnel Source (P^+N^+ tunnel diode) MOSFET [3]. The device structure of the novel asymmetric MOSFET is shown in Fig. 3. The gate electrode controls the source-to-channel tunneling current by modulating the band-alignment between the valence band of the P^+ tunneling source and the conduction band of the channel (thus modulating the availability of density of states for tunneling) and modulating the tunneling width (Fig 4).

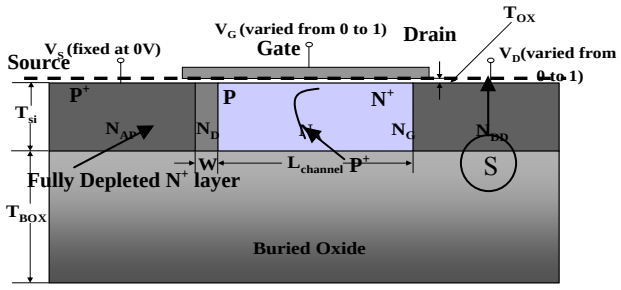

Figure 3 Device structure of the novel PNPN MOSFET

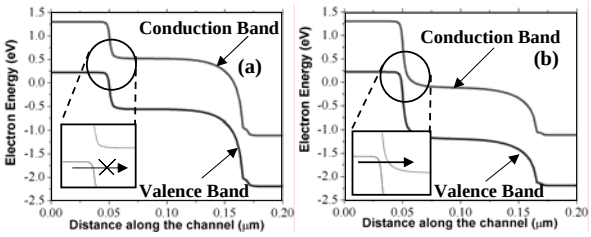

Figure 4. Band Diagram along the channel along section S in Fig. 3. (a) $V_G < V_{TH}$ (b) $V_G > V_{TH}$.

Detailed simulations show that the optimized novel PNPN MOSFET exhibits a steep sub-threshold slope (<<60mv/dec) (Fig 5a) with negligible DIBL. This is due to the fact that the overlap of the available density of states changes abruptly from zero to a finite value along with a reduction in tunneling width as the gate voltage increases from 0 to V_{TH}. Since the subthreshold behavior is determined by the tunneling source junction, DIBL is significantly reduced. Fig. 5b shows the I_D-V_D characteristics for the tunnel source MOSFET and a conventional SOI MOSFET. In the above threshold regime, the resistance of the tunneling junction is negligible for the PNPN MOSFET resulting in a current characteristic similar to a conventional SOI transistor. The threshold voltage (V_{TH}) is defined as the gate voltage at which the channel conduction band overlaps with the source valence band. Therefore, for the same V_G-V_{TH}, the drive current is larger (band bending > 2 φ_b) for the PNPN MOSFET.

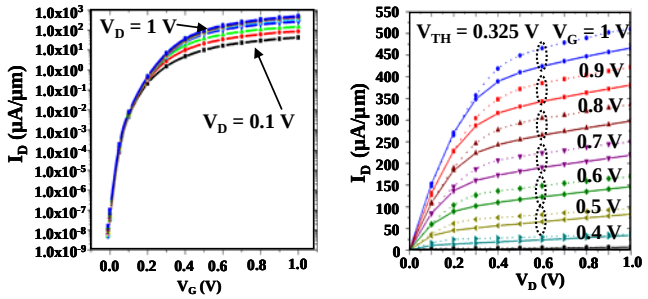

Figure 5 (a) Subthreshold Characteristics of a Tunnel Source FET. (b) I_D-V_D characteristics for different V_G for the Tunnel Source FET (dotted) and conventional MOSFET (solid)

3. Tunneling transistors on GeOI

Germanium has regained attention for its low field high electron and hole mobilities which are beneficial for carrier transport in nanoscale devices. In addition, due to its smaller bandgap and therefore smaller tunneling width, Ge is the material of choice for both the Schottky FET and the Tunnel Source FET. To better control short channel effects and junction leakage current and to make germanium acceptable in current silicon production line, germanium-on-insulator (GeOI) is preferred. GeOI substrates can be obtained by wafer bonding and Smart-Cut™ techniques. A successfully transferred germanium on oxidized silicon wafer is shown in Fig. 6. The fabricated GeOI substrate has large amounts of vacancies which are the major diffusion vehicles in germanium. The electrical concentrations in bulk germanium and GeOI are then determined by the Fermi level dependency of dopants (Fig. 7a). Boron yields identical active concentration in two substrates, whereas phosphorous shows lower active level in GeOI due to faster diffusion assisted by charged vacancies, and this may affect scalability of germanium nMOSFETs. Another challenge of Ge devices is the quality of gate stack. A stable metal gate electrode against the selection of gate dielectrics is essential. In our study, Mo/germanium oxynitride gate stack is found to be thermally stable up to 400°C with interface charge density in the orders of 10^{12} /cm^2, as shown in Fig. 7b. A further reduction of the charge density is still needed.

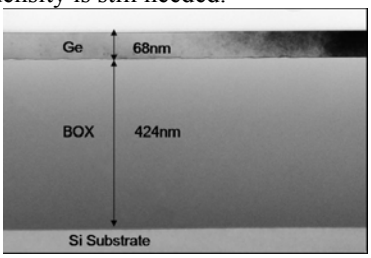

Figure 6 XTEM of a GOI sample

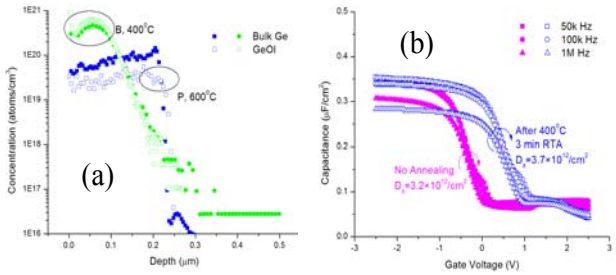

Figure 7 (a) Electrical concentrations of n- and p-type dopants in bulk Ge and GeOI (b) C-V curves of Mo/germanium oxynitride gate stack before and after annealing.

4. References

[1] Moongyu Jang et al, IEEE Transactions on Nanotechnology, Vol.2, No. 4, pp 205-209, 2003.

[2] Kazuya Matsuzawa et al, IEEE Transactions on Electron Devices, Vol. 47, No. 1, pp 103-108, 2000.

[3] N. V. Girish, Ritesh Jhaveri and Jason C. S. Woo, IEEE 2004 Silicon Nanoelectronics Workshop, 2004, pp. 33-34.

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Outline

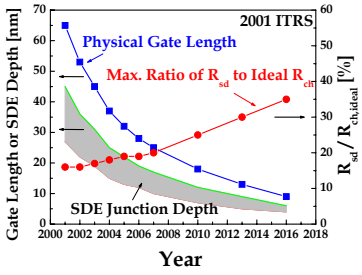
- **Motivation for sub-25nm novel device concepts**
- **GeOI Devices**
- **Schottky Transistors**
- **Tunnel Source (PNPN)MOSFET**

Scaling Challenges

Challenges arising due to scaling in the sub-nm regime

- **Source/Drain-to Channel Electrostatic Coupling**
- **Channel Transport Limitation (Mobility Reduction, Velocity saturation)**
- **Parasitic Effects (Source/Drain Resistance/Capacitanc, Gate Leakage)**

SDE & Series Resistance Scaling Trends

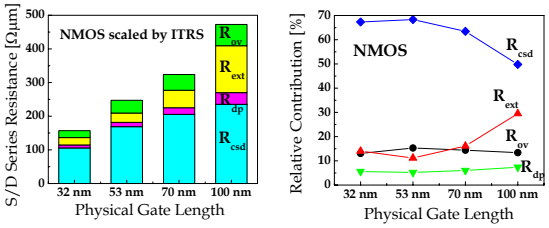


$R_{ch} \propto \frac{L_{ch} t_{ox}}{(V_{gs} - V_{th})}$ ⇒ Scaled with L_g ($L_{ch}\downarrow$, $t_{ox}\downarrow$)

$R_{sd} \propto R_{sh} \propto \frac{1}{N_{sd} X_j}$ ⇒ Difficult to scale R_{sh} ⇒ $R_{sd}/R_{ch}\uparrow$ ($N_{sd}\uparrow$, $X_j\downarrow$)

Relative Contributions of Resistance Components

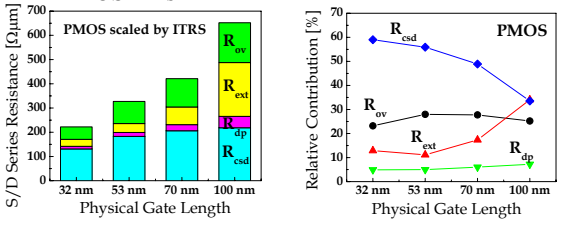
❑ NMOSFETs



- Assumptions : Scaled according to ITRS projection
  Gradual doping & midgap silicide material
- R_{csd} will be a dominant component for highly scaled nanometer transistor
  (R_{csd}/R_{series} is rising up to >> ~ 60 % for L_G < 53 nm)

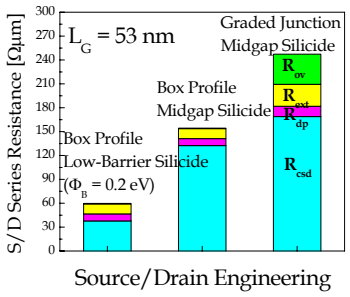
Relative Contributions of Resistance Components

❑ PMOSFETs



- **Relatively large R_{ov} contribution, but still largest in R_{csd}**
  (R_{csd}/R_{series} : ~ 60 % , R_{ov}/R_{series} : 20 ~ 30 % for L_G < 53 nm)

Advanced S/D Engineering

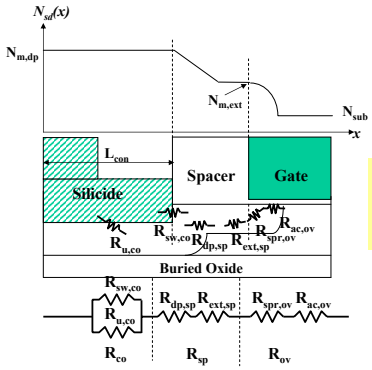


- **Potential solutions for advanced S/D Engineering:**

⇒ **Box-shaped highly-doped ultrashallow SDE junction (i.e., laser annealing)**

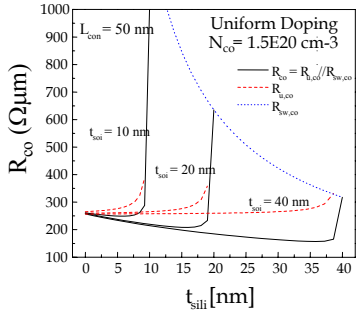
⇒ **Schottky Barrier lowering (i.e., ErSi for NMOS, $PtSi_2$ for PMOS, and lower bandgap $Si_{1-x}Ge_x$ layer)**

SOI MOSFET

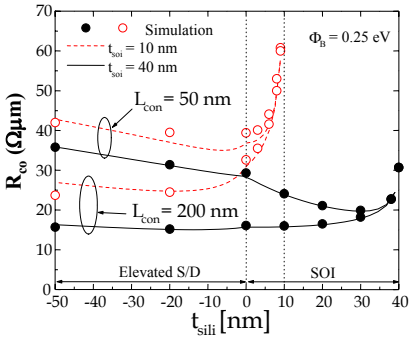


$$R_{extrinsic} = 2R_{sd}$$
$$= 2(R_{co} + R_{sp} + R_{ov})$$

Contact resistance in SOI MOSFETs



Need Contacts with Low Φ_B



Low SBH (Φ_B = 0.25 eV) (ρ_c = 1.27X10^{-8} Ωcm^2 for uniform doping)

Scaling Challenges

Challenges arising due to scaling in the sub-subnm regime

- **Source/Drain-to Channel Electrostatic Coupling**
- **Channel Transport Limitation (Mobility Reduction, Velocity saturation)**
- **Parasitic Effects (Source/Drain Resistance/Capacitanc, Gate Leakage)**

Potential Solutions

- **Improved Device Architecture (Double/Tri-gate MOSFETS)**
- **New materials to enhance transport (SiGe or Ge channel)**
- **New Gate Dielectrics to reduce gate leakage (High-K)**
- **Small ϕ_B contacts --- Small E_G Source/Drain Junctions**

Potential Solutions

- New Materials with Higher Mobilities
- New Gate Stack to Reduce Tunneling
- New Contact Materials (Metal and Semiconductor) to reduce R_{co}
- New S/D Structures (e.g. Raised S/D) for Small $R_{S/D}$
- SOI, DG, … to improve SCE

Essentially, Try to Make Scaled MOSFETs Follow Scaling Behavior of "Long Channel Device Miniaturization"

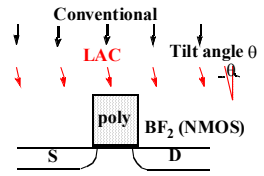
Alternatives?

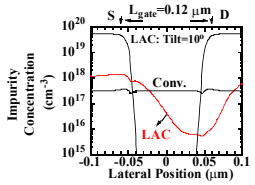
New Device Architectures
- Novel Transports
- Incorporate QM Effects

New Materials
- High Mobilities
- Bnadgap Engineering

Others

Lateral Asymmetric Channel (LAC) MOSFET





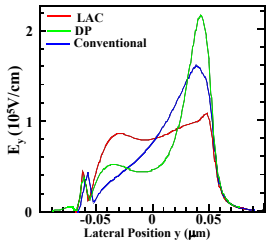
- Formation of Channels in the LAC and conventional structures. Usual tilt angle: 10°-15°
- Simulated channel profiles for devices with same Vth from source to drain 1.5 nm away from the SiO2/Si interface.

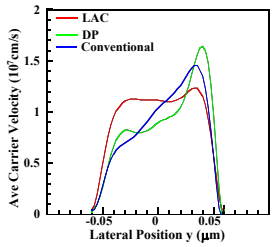
Lateral Asymmetric Channel MOSFETs

What are the advantages?

- Suppression of Short Channel Effects similar to the Double Halo (DH) structures in bulk devices
- Higher Current Drive than DH for both Bulk and SOI devices
- Higher Transconductance than DH and conventional devices for bulk devices
- Improved Early Voltage compared to DH in bulk devices
- Improved low frequency Flicker Noise compared to conventional devices

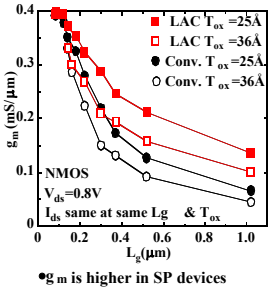
LAC Transistor

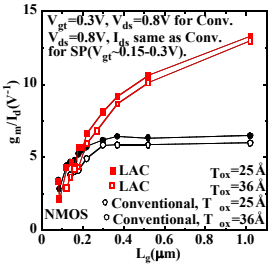




LAC Devices: Higher doping near the source end ⇒
- High lateral electric field near the source end in channel region
- High average carrier drift velocity near the source end in channel region
- High current drive, $I_{ds} = W C_{ox}(V_{gs}-V_{th}(y)-V(y))v(y)$

LAC DEVICES: ANALOG PERFORMANCE



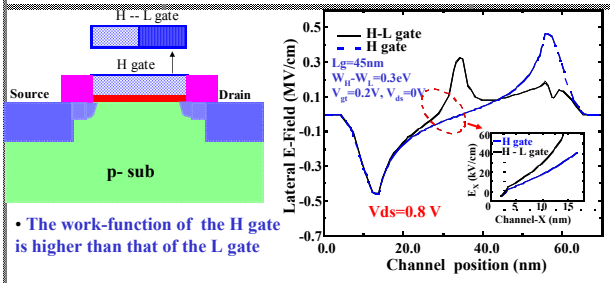


- g_m is higher in SP devices
- g_m/I_d ratio is very high compared to conventional devices when biased at same current density :
  - due to high current drive, small Vgt is needed. Also high g_m

Issues with LAC Transistors

- High doping near the source – Lower Mobility
- Sharp doping profile in sub45 nm transistors – Difficult

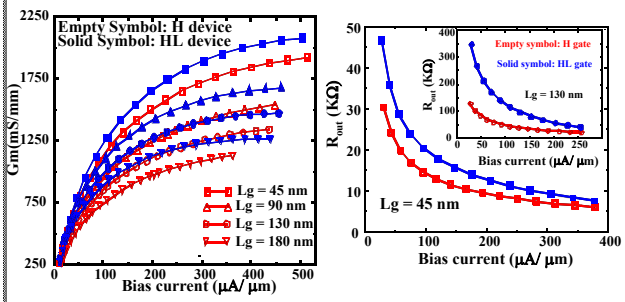
Proposed Split Gate Design



• The work-function of the H gate is higher than that of the L gate

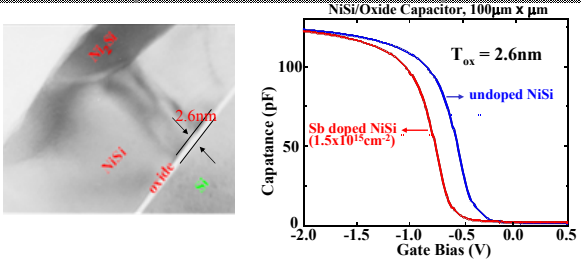
•An electric field peak is generated in the channel close to the source side which enhances source carrier injection into the channel (g_m ↑).
• R_{out} can be increased due to the reduced channel-length-modulation.

Simulation: G_m and R_{out} in scaled MOSFETs



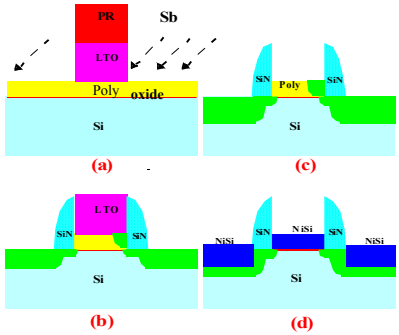
• Both g_m and r_{out} can be improved by using this split gate design for different channel length considered.

S_b-induced Work Function Shift in the NiSi Gate



• NiSi Gate: Gate full silicidation and no oxide degradation.
• Antimony implantation in the polysilicon gate reduces the NiSi gate work function (~0.25eV) due to the dopant segregation effect at the NiSi/oxide interface.

Process Flow



• Oxide/Poly/LTO: 4.5nm/50nm/200nm

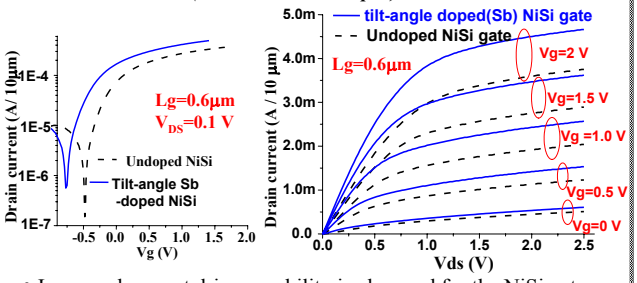
• Sb implant energy, dose and angle: 25KeV, $1.5x10^{15}$ cm^{-2}, 30°

• Nitride spacer width : ~ 80nm

• Silicide conditions: 10mins @ 450 °C

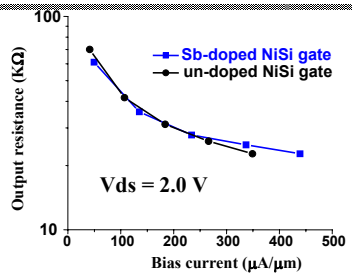
Id-Vg and Id-Vds curves

(Substrates are undoped)



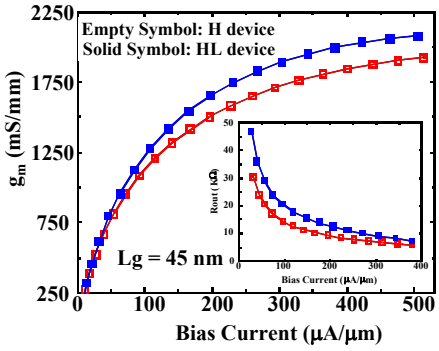
• Improved current drive capability is observed for the NiSi gate device with tilt angle S_b implantation from the drain side, i.e, the split-gate device.

Output Resistance

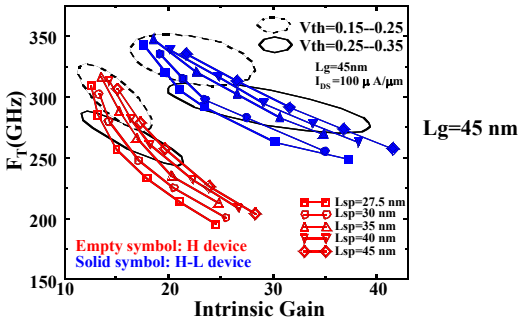


- At lower bias current, both devices have similar r_{out} due to their large DIBL as a result of un-doped substrates.
- At higher bias current, the split-gate device has higher r_{out} due to its less channel-length-modulation at the drain side.

Scalable?



Improved speed-gain performance



- Split-gate HL MOSFETs have improved gain- frequency performance compared with conventional MOSFETs

Novel Materials

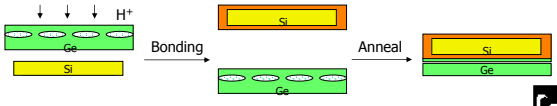
CMOS Research Laboratory

GOI MOSFET

- Advantages of germanium
  - Large low field mobilities
  - Reduced $R_{S/D}$
  - Large Tunneling Probilities
  - Possibility of optoelectronic integration

Gemanium-on-Insulators Wafers

- Why Germanium-on-Insulators?
  - Germanium is expensive ($$$) and brittle.
  - Germanium has high dielectric constant, so worse SCE.
  - Help our industry peers incorporate Ge into existing Si production lines.
- How to make it?
  Wafer bonding and Smart-Cut™ technologies are employed to fabricate GeOI substrates.

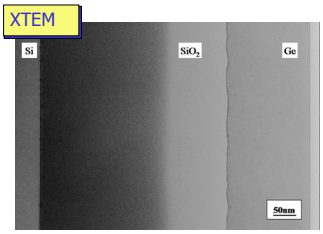


Gemanium-on-Insulators Wafers

- Germanium film remains single crystalline known from TEM diffraction pattern.

As-split

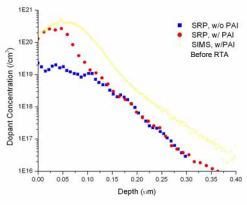
XTEM



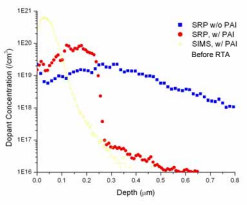
Dopant Activation in Ge/GeOI

- **Bulk Ge**
  - The difficulty of dopant activation arises from the limited solid solubilities and fast diffusion of dopants in Ge.
  - Rapid thermal annealing and pre-amorphization implantation (PAI) are combined to address the issues.

B, 650° C

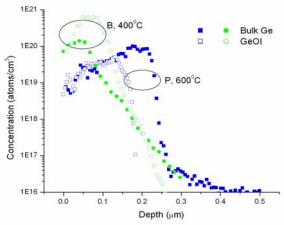


P, 600° C



Dopant Activation in Ge/GeOI

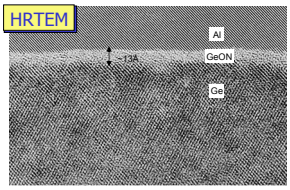
- **GeOI**
  - The lower level of P activation in GeOI is due to enhanced diffusion by vacancies created by hydrogen implantation.
  - The cause for the high level of boron concentration in GeOI is still under investigation.

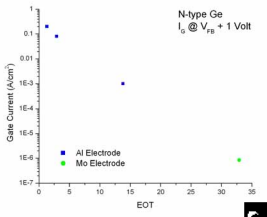


Gate Dielectric/Electrode in Ge

- Germanium oxynitride is used as gate dielectric film in our study.
- This film seems to exhibit low gate leakage current, but the reliability remains a concern, and more study is on going.

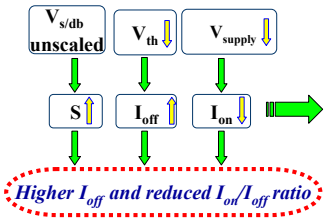
HRTEM





Novel QM-Injection Transistos

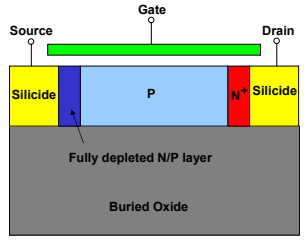
Motivation



Exploit novel device physics concepts made possible by nano-dimensions to achieve steep subthreshold swing and ballistic carrier transport to give high I_{on}.

$V_{s/db}$ – Source/Drain-Substrate Junction Potential
V_{th} – Threshold Voltage
S – Subthreshold Swing

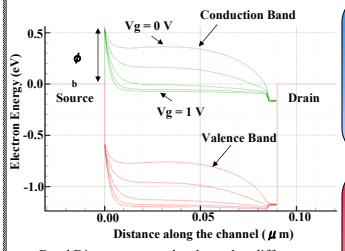
Assymetric Schottky Tunneling Source MOSFET



- Schottky Barrier between Fully Depleted pocket and the source silicided junction
- Fully Silicided Source/ Drain Junctions
- N^+ Region on the drain side to form an ohmic contact between drain and substrate

The gate controls the tunneling through the schottky barrier on the source side by changing the tunneling width as well as the available density of states on the semiconductor side

Device Concept

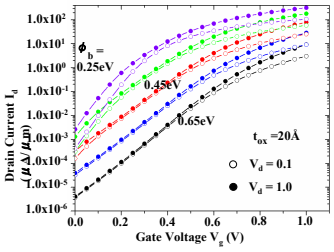


Band Diagram across the channel at different gate voltages (V_g) for V_{drain} = 0.1 V and ϕ_b = 0.55 eV

a) $V_{gate} < V_{threshold}$
- Tunneling Distance of the schottky junction is large
- Number of available states on the semiconductor side is limited
- Subthreshold current is limited by schottky tunneling resistance

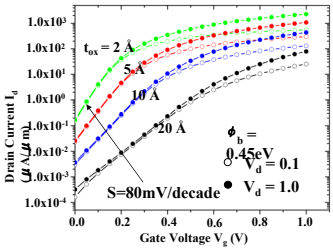
b) $V_{gate} > V_{threshold}$
- Tunneling Distance decreases
- Number of available states on the semiconductor side increases
- Tunneling Resistance decreases and current gets limited by channel and tunneling resistance depending on certain parameters at the schottky junction

Barrier Height (ϕ b)

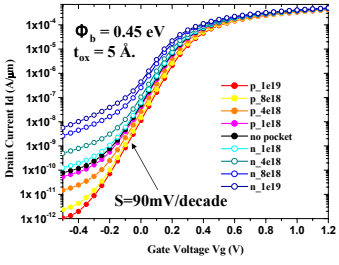


$N_{bulk} = 1x10^{17}cm^{-3}$ $N_{pocket} = 1x10^{17}cm^{-3}$

Gate Oxide thickness (t_{ox})

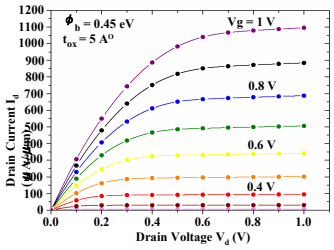


Pocket Doping (N_{pocket}) to improve I_{ON}/I_{OFF}



- As n-type pocket doping ↑ tunneling distance ↓ (whereby reducing threshold voltage)
- n-type pocket doping ↑; subsurface conduction increases
- p-type doping ↑ a region with high threshold is obtained near the source
- This reduces subsurface conduction and I_{on}/I_{off} ratio considerably.

I_d-V_d curves



- Due to much better control of SCEs the R_{out} at a given I_D is much higher than for a conventional device.
- However, I_{on} is always smaller than conventional MOSFET at same $(V_g - V_{th})$ at a given t_{ox} which degrades the gm/I_{DS} ratio
- This is due to a drop at the schottky junction which reduces effective drain-source voltage (V_{DS})

The Tunnel Source MOSFET

"A novel device structure incorporating gate controlled source injection by band-to-band tunneling"

Tunneling Source Transistors

Device Physics Enabled by small-dimensions: **Quantum Mechanical Tunneling (Band-to-Band)**

governed by

governed by

Tunneling Probability(T_t) dependent on the Tunneling width

Fermi Selection Rule

$F_V(E)*[1-F_C(E)]*u(E)$

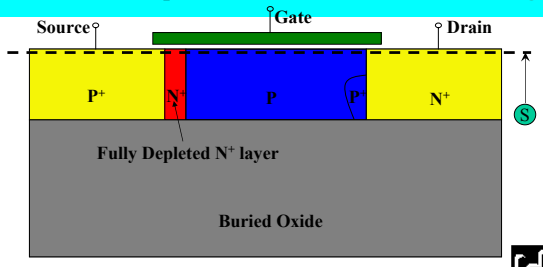
Where u(E) =1 if there is availability of states to tunnel to; 0 otherwise. $F_V(E)$ and $F_C(E)$ are Fermi-Dirac distribution functions for the initial (valence band) and final (conduction band) energy states.

Basic Equation used for the tunneling current: Esaki Diode integral

$$I_{V\text{-}C}=A \int F_V(E)*n_V(E)*T_t*[1-F_C(E)]*n_C(E)*u(E)dE$$

The Tunnel Source (PNPN) MOSFET

- **Gate controlled P^+-N^+ tunneling junction is used as a source of electrons (Tunneling width is reduced by the fully depleted N^+ layer)**
- **Novel device concept based on Band-to-Band Tunneling**



The Tunnel Source (PNPN) MOSFET

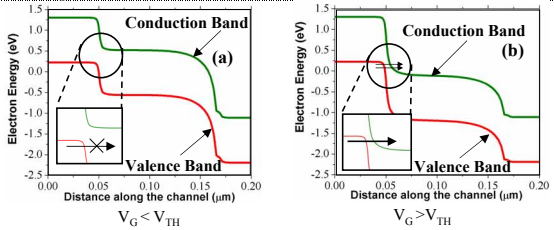
Gate controls the source-to-channel tunneling current by

- **modulating the band-alignment between the valence band of the tunneling-source junction and the conduction band of the channel, thus modulating the availability of density of states for tunneling**
- **modulating the tunneling width (which is already made small because of the narrow and fully depleted n-pocket)**

Important condition for successful device operation:

- **The n-pocket of the PNPN device needs to be narrow (<10nm)**
- **The doping of the pocket should be such that it is fully depleted**

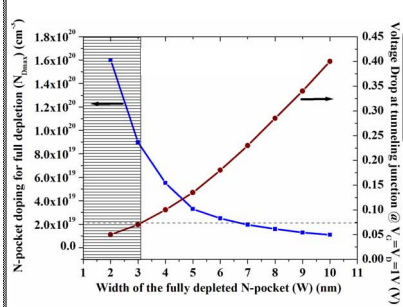
The Tunnel Source MOSFET



$V_G < V_{TH}$ $V_G > V_{TH}$

- When $V_G < V_{TH}$, current level is small since the electrons from the P^+ valence band can **tunnel** only to the **trap states**
- When $V_G > V_{TH}$, electrons from the P^+ source valence band **tunnel** to **empty states in the conduction band** of the channel

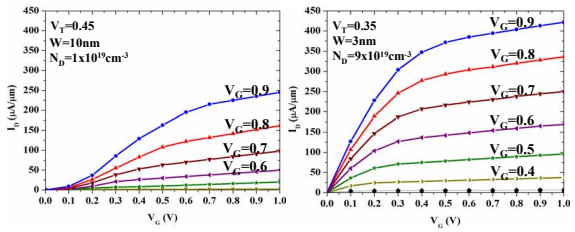
Tunneling Width Minimization



For any given width W, doping needs to be less than N_{dmax} to maintain full depletion. As W decreases, N_{dmax} ↓ as shown.

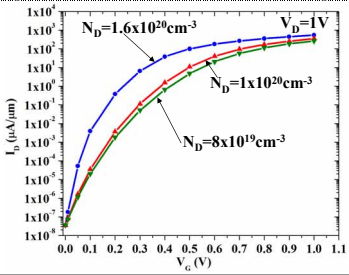
As the width W of the N-pocket decreases, the voltage drop across the tunneling junction reduces. A width of 3nm or less is needed for negligible voltage drop.

Small Pocket Width (W)



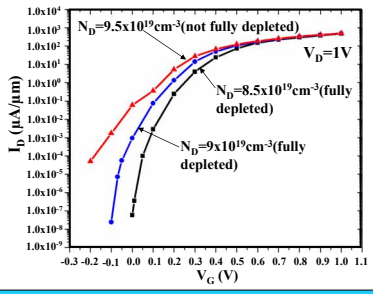
A narrow width (W≤3nm) with a doping close to N_{dmax} gives high I_{DS}

Pocket Doping (N_D)



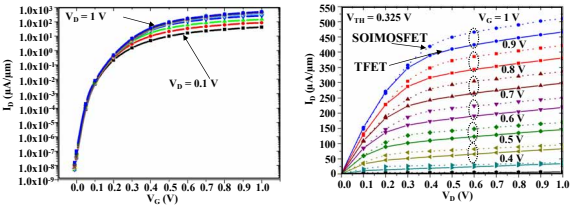
$N_D \leq N_{dmax}$ for good subthreshold characteristics by minimizing tunneling width.

Pocket Doping (N_D):

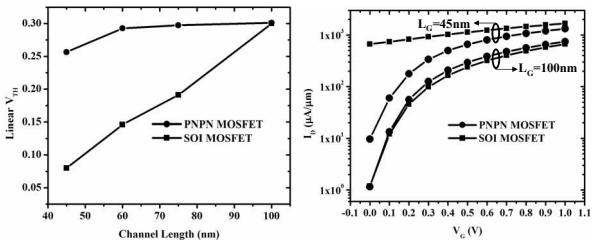


$N_D >$ N_{dmax} results in degraded sub-threshold slope. Device is no longer tunneling limited

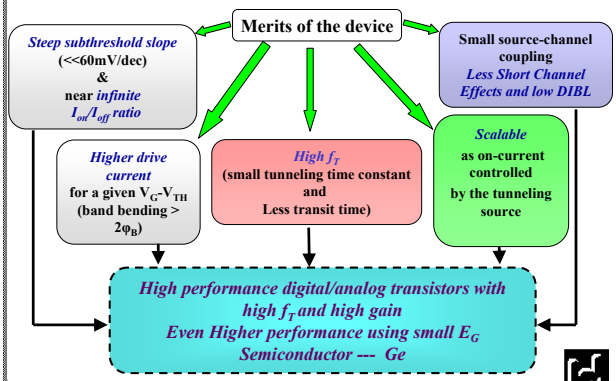
Device Performance



Scaling behavior



Summary



Conclusion

- New Device Structures Exploiting Physical Mechanisms Made Feasible by Nano-dimensions
- Ge has Small E_G not just High mobilities
- Tunnel-Source Transistors Promosing
- Parasitics Still Need Special Attention