Conventional Bulk and "Bulk+" Architectures for 45nm Node

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Abstract

We discuss the possibility of using bulk architecture for 45nm node by a proper device design and the use of technological boosters. We also propose an alternative solution allowing the use of single metal gate with thin films, co-integrated with conventional bulk devices on bulk substrate. This solution defines a "Bulk+" technology.

Introduction

Power management appears as an important issue for 45nm node. Indeed, following the 0.7 scaling rule for the MOSFET device parameter leads to a SiON gate oxide thickness hardly compatible with the leakage requirements of General Purpose Low Operation Power (GP) and Low Standby Power (LP) applications (*Figure 1*). This issue is well known, and the first solution looked at by industry was the use of High-K dielectric (such as HfO_2 or HfSiON). Unfortunately, these oxides suffers from several issues, such as mobility degradation and Fermi pinning [1]. Recently, the use of Si-rich HfSiON/Poly-Si gate together with buried conduction channel (counter doped) was proposed [2,3] in order to compensate the threshold voltage shift due to Fermi Pinning. Nevertheless, this leads to a strong DIBL making the control of nanometric devices difficult. Another solution is the use of metallic gate on High-K, where Fermi pinning phenomenon is negligible [4] . Nevertheless, in order to be able to correctly adjust devices threshold voltage for all kind of applications, workfunctions of metallic gates should be identical to those of n^+ and p^+ doped poly-Si. This makes necessary the use of two different metallic gates [5] for nMOS and pMOS devices, leading to complex integration scheme and reliability issues. In order to design devices for 45nm we propose a different strategy consisting in minimizing the scaling of gate oxide as proposed in [6,7] by keeping either Poly-Si gate or Single Metal Gate. In the first case, the subsequent loss on device speed performance is evaluated to 20%. Therefore, smart optimisation of device must be performed in order to compensate this speed degradation due to the static leakage reduction. This conventional Bulk approach is compatible with consumer electronics applications where a very low-cost is a major driver.

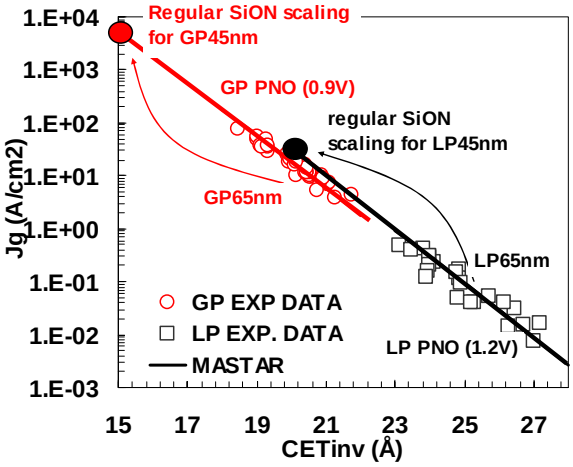

Figure 1 :Gate leakage trend as a function of CETinv for Plasma Nitrided oxides. A regular scaling of the 65nm node CET to 45nm using poly-Si gate electrode lead to an excessive leakage current.

In the second case, a single mid-gap gate electrode (or close to mid-gap) is used in combination with a fully depleted thin-film channel. This ensures the adjustment of threshold voltage for both GP and LP applications and allows a better scaling of total gate capacitance, by suppression of poly-depletion effects. A major point in this approach is the co-integration of regular bulk devices, in order to ensure a full compatibility of the analog and I/O platform. The "Silicon On Nothing" (SON) architecture is a promising candidate in this perspective, defining a "Bulk+" architecture. In this paper we show examples of conventional "Bulk" optimisation using Strain-Silicon, advanced USJ and "Bulk+" integration for 45nm node (*Figure 2*.)

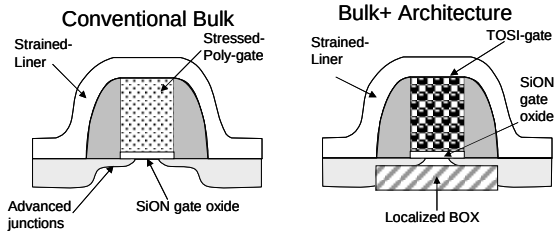

Figure 2 : Schematic view of bulk and bulk+ architectures

Bulk optimisation for 45nm node

In order to compensate performance reduction due to gate stack limited scaling, the use of cumulated strained-silicon options is mandatory. For electrons, uni-axial tensile stress is known to allow performance improvement. This stress can be induced by a tensile nitride liner, used as Contact Etch Stop Layer (CESL) [8] as shown in *Figure 3*. This layer creates tensile zones near the gate edge and a compressive zone in the center of the MOSFET channel. For short devices, the tensile zones on the edge are overlapping, leading to a device with a complete tensile channel. As a result nMOS performance is improved by 10~15%.

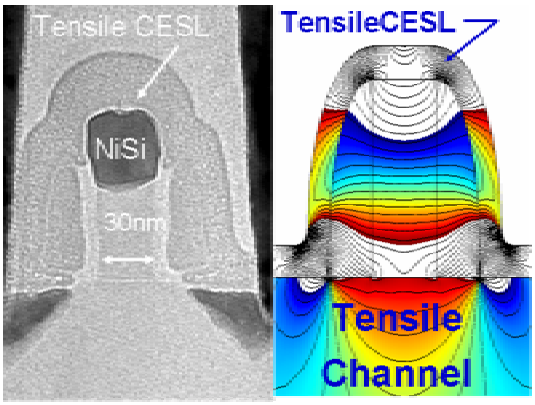

Figure 3 : Tensile strained-channel MOSFET (Lg=30nm) created using stressed-nitride layer as Contact Etch Stop Layer

The use of this techniques can lead to a hole mobility degradation, and may require an additional Ge implantation in the CESL layer on pMOS [9] to relax channel stress. Other techniques can be used to induce stress in MOSFET channel by process, such as Stress Memory Technique. This technique consist in a gate poly-Si re-crystallization under a stressed capping layer by using S/D anneal [10], and leads to an improved nMOS performance (6~10%). Depending on used materials, it can be necessary to remove the capping layer on the pMOS before performing the S/D anneal. An interesting point is that CESL and SMT layers effects are additive. In *Figure 5*, 20% improvement on nMOS performance is obtained by the combination of SMT and CESL.

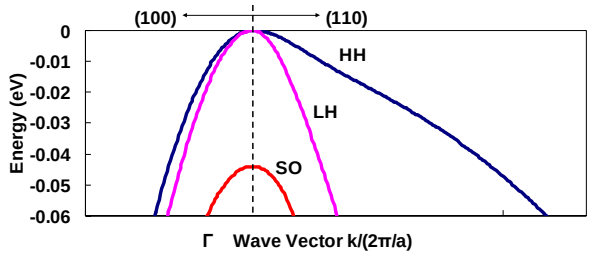

Figure 4 : Valence band structure of Si computed using a 6x6 Lutinger Hamiltonian.

For holes mobility improvement, compressive liner can be used and co-integrated with tensile liner [11]. Nevertheless, a lower cost solution can be used for GP/LP application. Indeed, a closer look on the band structure of holes reveals anisotropy of the Heavy-Holes (HH) sub-band (*Figure 4*). In particular, HH are 'lighter' in the (100) direction. As a result, using (100) channel for pMOS devices leads to 15% improvement on the drive current (*Figure 5*).

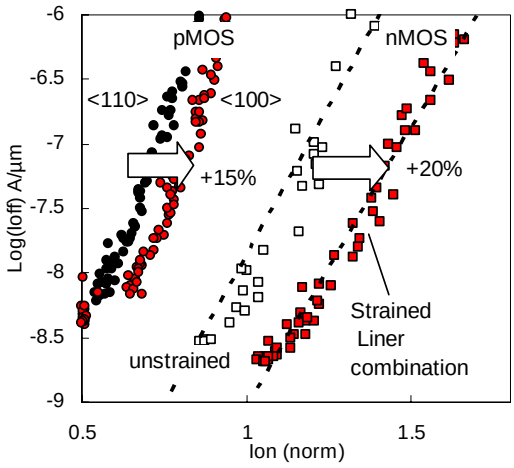

Figure 5 : nMOS and pMOS performance improvement using low-cost mobility boosters. 15% drive current improvement is obtained on pMOS by using (100) channel. 20% improvement on nMOS drive current is obtained by using a combination of strained liners.

Integration of these conventional strained bulk devices with Lg=30nm (*Figure 6*) has been successfully demonstrated into a 0.334µm² SRAM bit-cells representative of 45nm node design rules [12].Besides mobility improvement, a performant junction scaling is also mandatory in order to achieve good control of the Short Channel Effects.

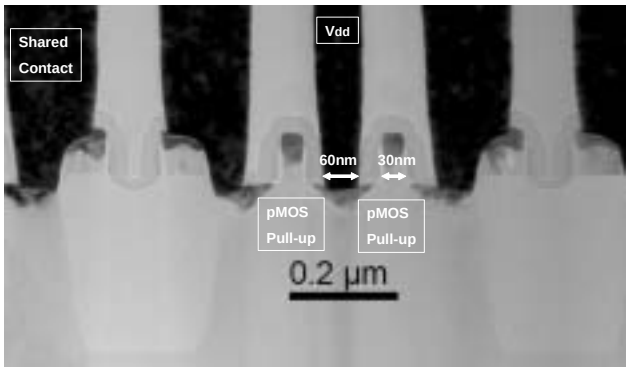

Figure 6 : TEM Cross section of a 0.334µm² SRAM bit-cell for 45nm node

Ultra short non-diffusing anneals are a promising candidates to realize both improvement of SCE control

and dopant activation enhancement. As shown on *Figure 7*, the combination of these new techniques (LSA or Flash Annealing) with spike annealing allows improving the nMOS (pMOS) performance by 11% (6%) respectively. Without spike annealing the DIBL effect can be significantly reduced for both nMOS and pMOS [13].

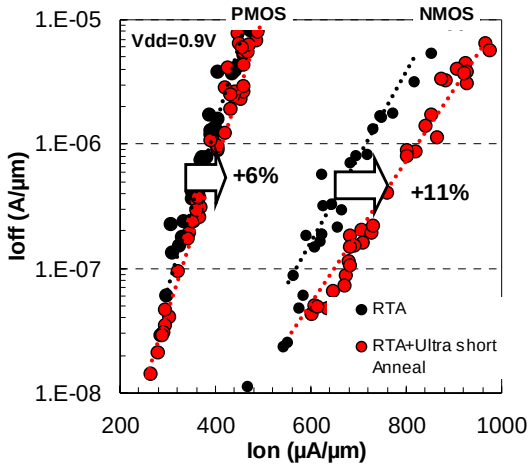

Figure 7 : Performance improvement is obtained by using ultra-fast S/D anneal in combination with regular spike RTA.

Bulk+ for 45nm node

Using of a modulated mid-gap metal gate in combination with fully depleted thin film is a way to obtain a regular gate capacitance scaling (though poly-depletion suppression) without static leakage degradation (i.e. by keeping the same gate oxide thickness than in 65nm node), and adjusted threshold voltages for both GP and LP applications. First, mid-gap metal gates can be achieved by the use of the Totally Silicided (ToSi) gate process [14] using either CoSi2 or NiSi (*Figure 8*). If CoSi2-ToSi gates are mid-gap, NiSi-ToSi gate workfunction can be modulated through the use of ion-implantation. Depending on the dopdant type and dose, it has been shown that workfunction could be adjusted toward n^+ type or p^+ type [15].As a result, workfunction can be modulated by +/- 300meV around the mid-gap, allowing threshold voltage adjustement for LP and GP devices on FD films. Next, the realisation of FD device on bulk substrates has been successfully demonstrated by using the Silicon On Nothing (SON) technique [16-17]. Main device process-steps are described in *Figure 9*. After STI patterning, a SiGe Selective Epitaxial Growth (SEG) is performed followed by a Si SEG. This last layer defines the future conduction channel of the SON device. After gate patterning, a junction recess is performed in order to access to the SiGe buried layer. Then, a selective removal of the SiGe is performed, leading to an empty tunnel under the gate. At this stage, the channel stands above "nothing". The tunnel is then filled with dielectric, allowing the creation of a local Burried Oxide (BOX).

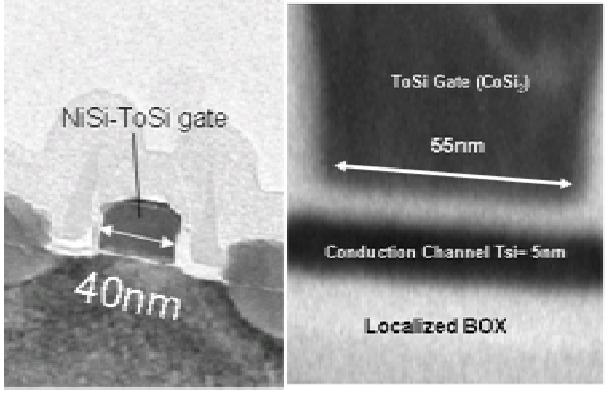

Figure 8 : Example of different ToSi gates : NiSi/Bulk (right) – CoSi2/Bulk+ (left)

Finally, junctions are re-filled using a Si SEG. As a result, the device morphology reveals a fully depeled channel with a local BOX. *Figure 10* show the comparison of Lg=45nm poly-gate/SiON devices integrated with bulk and SON process. Using thin films allows improving DIBL and SS and also using lightly doped channel. Moreover, using thin films allows a lower channel implantation, leading to a reduction of the junction leakage by 1 decade. This makes the SON suitable for LP options.

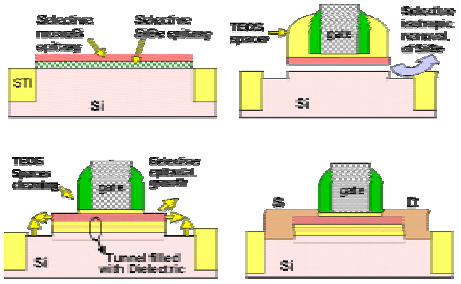

Figure 9 : main process steps of SON module

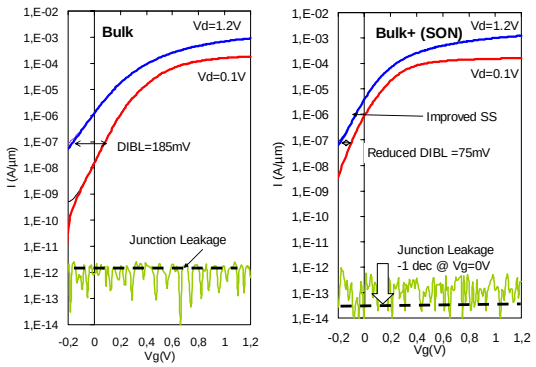

Figure 10 : Bulk versus Bulk+ (SON) sub-threshold characteristics. Subthreshold slope and DIBL are improved by using thin films.

In addition, an important point of the Bulk^{+} platform is the easy co-integration with standard bulk devices, mainly for analog and I/O application where thin film are not desired. Indeed, this allows the re-use of existing libraries and participates to the low cost of the technology. In order to achieve this co-integration, a hardmask is deposited on the bulk zone prior to the SEG to avoid the SiGe growth. Then no local BOX is created on these devices leading to regular bulk devices fabrication (*Figure 11*).

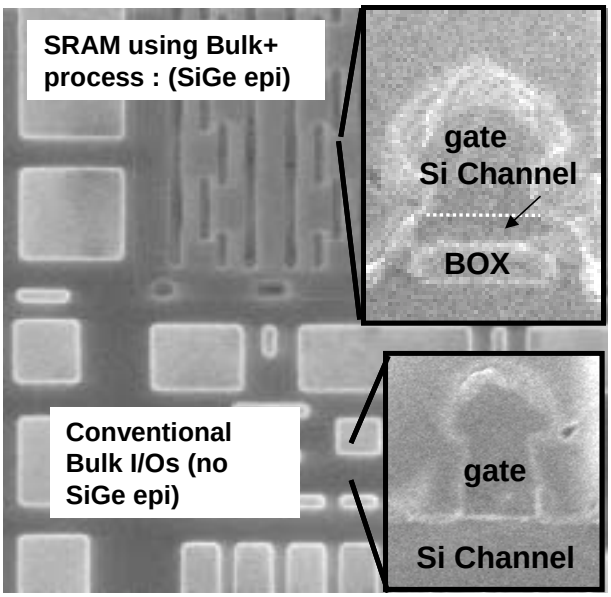

Figure 11 : Co-integration of bulk and bulk+ on the same chip is possible with SON module, by using a simple hardmask before SiGe SEG.

Finally, the combination of the ToSi process with the SON process allows fabricating Bulk+ devices with adjusted threshold, scaled inversion capacitance, and improved subthreshold characteristics

Conclusion

Using technological boosters, Bulk architecture is still a good candidate for low-cost consumer electronics products. Performance improved Bulk+ platform can be achieved by using combination of mid gap metal gate by ToSi process and Silicon On Noting technology.

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[5] S. Samavedam *et al,* IEDM 2002, pp 433
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[7] F. Boeuf *et al.*,IEDM 2004, pp 425-428
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[10] K. Ota *et al.* , IEDM 2002, p 27
[11] H.S. Yang *et al.,* IEDM 2004, p1075
[12] F. Boeuf *et al.,* VLSI 2005, p130
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[15] D. Aime *et al.,* IEDM 2004, p 87-90
[16] S. Monfray *et al.,* IEDM 2001, p645
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Crolles2 Alliance

45nm Conventional Bulk and "Bulk+" Architectures

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Outline

- **Introduction**
- **Conventional Bulk Definition for 45nm node**
  - **Device Optimization Strategy**
  - **Electrical Results**
  - **45nm node 6T-SRAM demonstration**
    - **E-beam processing**
    - **Electrical results**
- **Bulk+ Definition for 45nm node**
  - **ToSi gate process**
  - **Silicon On Nothing (SON) Process for Bulk+**
  - **Co-Integration of Bulk with Bulk+**
- **Conclusion**

Introduction

- Different targets for different products

- **High Performance applications** (MPU,CPU,VPU…)
  - •Optimization strategy → speed
    - •i.e. small Lg and high Ion
    - •Leakage is relaxed

- **Low Power applications** (mobile, cell-phone ….)
  - •Optimization strategy → Power dissipation
    - •i.e. small Ioff and high integration density (low cost products)
    - •Ion is relaxed

Introduction

- Boosters for **High Performance applications**
  - Strain-Silicon for enhanced mobility
  - Dual Metal Gate for low Vth nMOS and pMOS
  - High-K with small EOT <1nm ? (Sugii et al. SSDM 2005)
  - FD-Double gate architecture for SCE control

- Boosters for **Low Power applications**
  - Strain-Silicon for enhanced mobility
  - Single Mid gap Metal Gate for high Vth in nMOS and pMOS
  - High-K with small EOT >1.4nm
  - FD-Single gate architecture for SCE control

Introduction

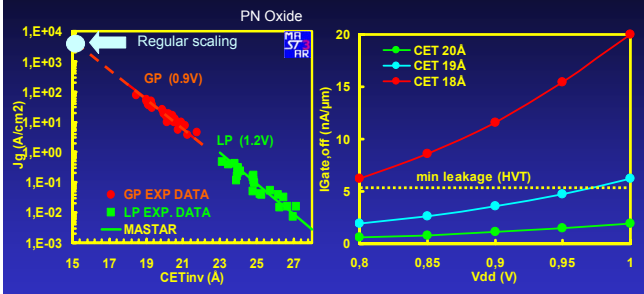
- At 45nm node, Performance Boosters for Low Power needs to be choosen
  - Hypothesis : keep SiON gate oxide

- **This work**

1. **Conventional approach : Optimization strategy for 45nm Bulk platform**
2. **Advanced Approach : Definition of a Bulk+ platform based on thin-film/MG devices**

Conventional Bulk for 45nm Node

Gate Oxide Shrink Limitation



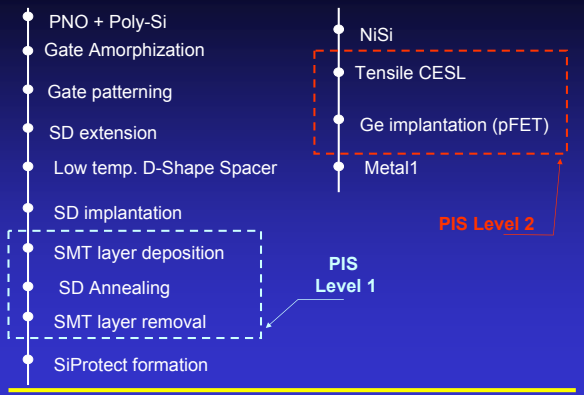
GP : CET 19 Å V_{dd}=0.85V (low leakage) and V_{dd}=1-1.2V (high speed)

LP : CET 25Å V_{dd}=1.2V

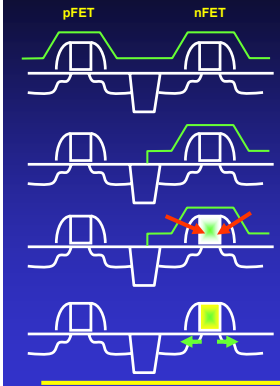
Strain-Si Technique compatibility with LP ?

Substrate-based		Process-based	
SRBs - Si_xGe_{1-x}	Rotated Sub.	Liners	SiGe SEG
no	yes	yes	yes
Junction leakage • SiGe band Gap • Default density	20-25% Gain on pFET	20-25% Gain on nFET	Junction leakage ? Cost ?

Process Induced Strain Flow



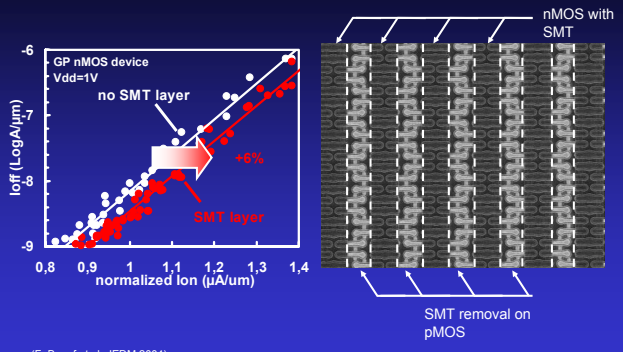
Level 1 : Stress Memory Technique



- Stressed liner deposition (oxide+nitride) [1,2]
- Selective etch on pMOS (see next slide)
- SD Anneal (RTA). Modification of poly-recrystalisation
- SMT removal. Tensile stress created in the nMOS channel

[1]Ota *et al.*, IEDM 2002
[2] Chen *et al.*, VLSI 2004

Level 1 (SMT) : Electrical Impact



(F. Boeuf et al., IEDM 2004)

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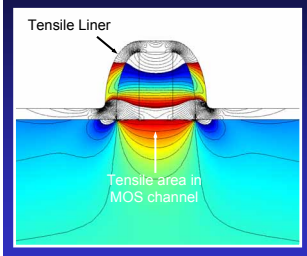
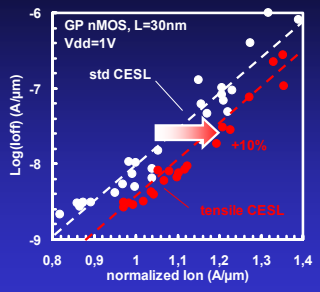
Level 2 : Contact Etch Stop Layer





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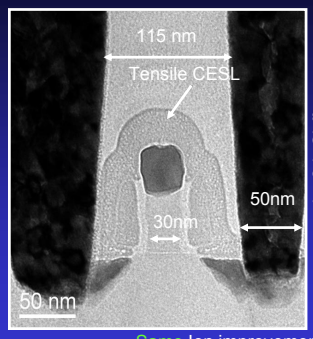
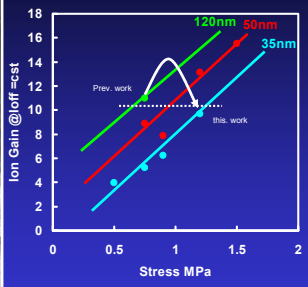
Tensile CESL optimization



Liner optimisation for SRAM integration



Same Ion improvement with reduced Thickness

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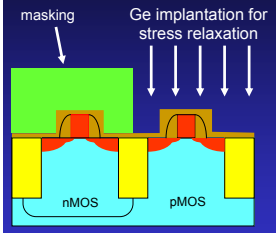
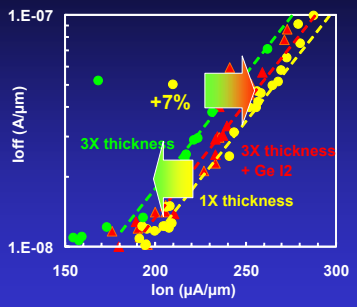
Impact of CESL on (110) channel pMOS





(F. Boeuf et al., SSDM 2004)

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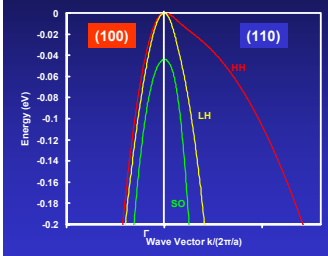
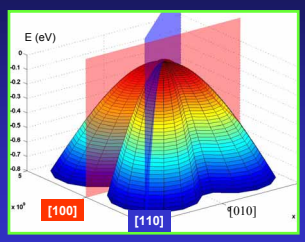
(100) Channel improves Hole mobility …

Heavy hole effective mass is lighter in (100) than in (110)
→ 25% increase of mobility





Si valence band computed by k.p hamiltonian

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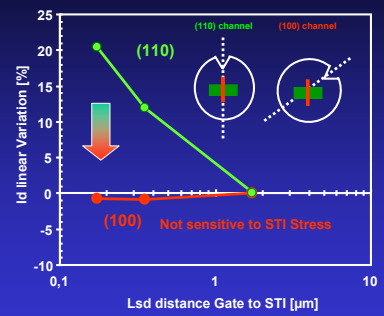
… and supress longitudinal stress effect !



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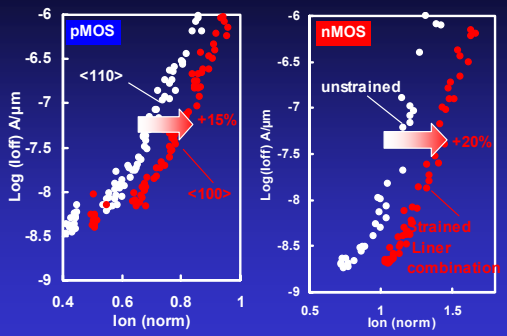
Strained-Si CMOS integration



Junction Optmization

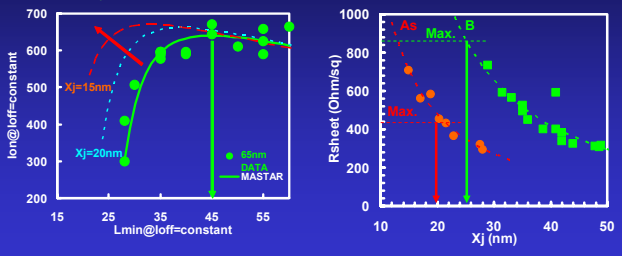
Gate Length shrink efficiency shows an optimum on I_{on} at a given I_{off}

Depending on Xj channel doping needed to keep good SCE will degrade channel mobility

Low temperature spike anneal allows shallow junction for As

→ Poly-depletion issues ?

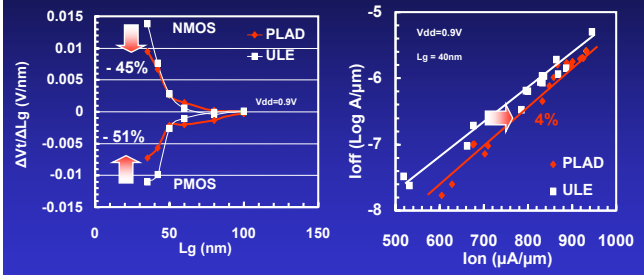
→ Lower Rs achiveable ?



Plasma Doping (PLAD)

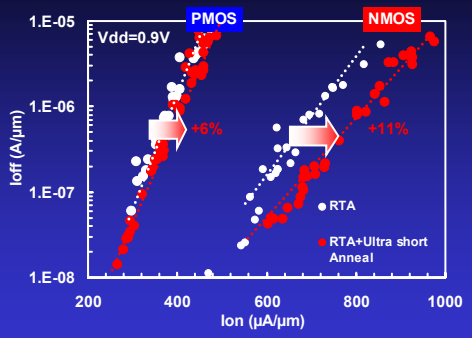
Improved SCE control on nMOS and pMOS

Lower pocket dose allows performance 4% improvement on nMOS

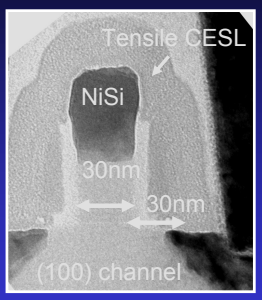


(B. Dumont et al., ESSDERC 2005)

Ultra Short Anneal Integration

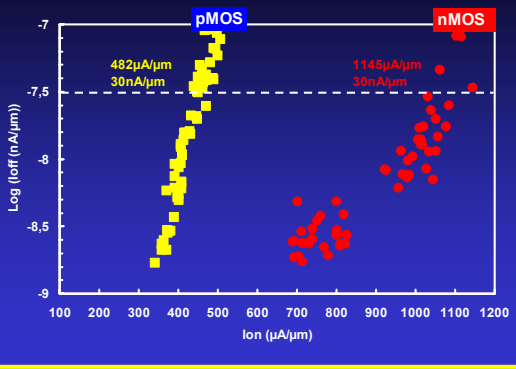


45nm Bulk Device Morphology

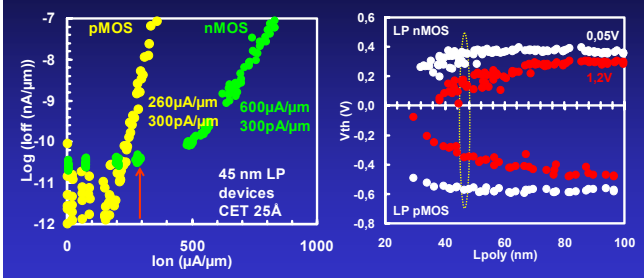


- TEM cross-section of device
  - 30nm gate length
  - 30nm D-Shape spacer
  - 50nm contacts
- Boosters
  - 100 channel for pMOS drive current enchancement
  - Highly tensile CESL for nMOS drive current enchancement

GP MOS : Electrical Results



Low Power Devices (L=45nm)



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Conventional Platform Definiton

Design	Pitch (nm)	
	65nm [1]	45nm
OD	190	130 ~140
PO	165	115~130
CO	200	140~150
M1	180	125~135
PO-CO	45	30~35
N^+/P^+	135	95~105
Density	800 kG/cm²	1600 kG/cm²

2X

- Platform needs to be compatible with 45nm design
- Linear scaling factor 0.7-0.75
- Surfacic density 2X
- 6T-SRAM bit-cells for 65nm node
  - 0.69µm² - 0.499µm²
- 6T-SRAM bit-cells for 45nm node
  - 0.35µm² - 0.25µm²

[1] Arnaud *et al.*, VLSI 04

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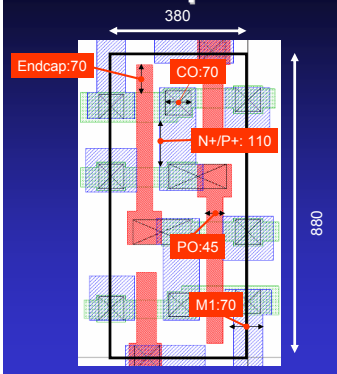
HD 0.334µm² SRAM bit-cell Design



Main Design Rules		
	Pitch	Line/space
OD	135	55/80
PO	125	45/80
CO	160	70/90
M1	140	70/70
PO-CO	35	
n+/p+	110	

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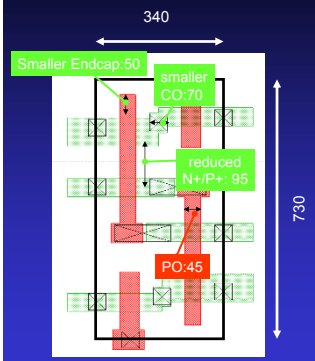
UHD 0.248µm² SRAM bit-cell Design



Main Design Rules		
	Pitch	Line/space
OD	135	55/80
PO	125	45/80
CO	140	50/90
M1	130	70/60
PO-CO	35	
n+/p+	95	

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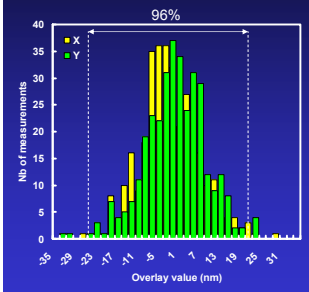
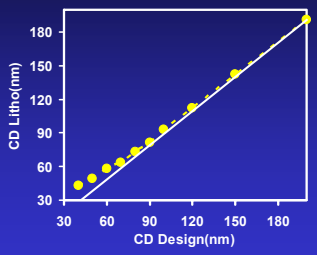
E-beam Lithography Capability for R&D Validation

96% of values with overlay with [-23,+23nm]

Linearity Control must be corrected for SRAM patterning





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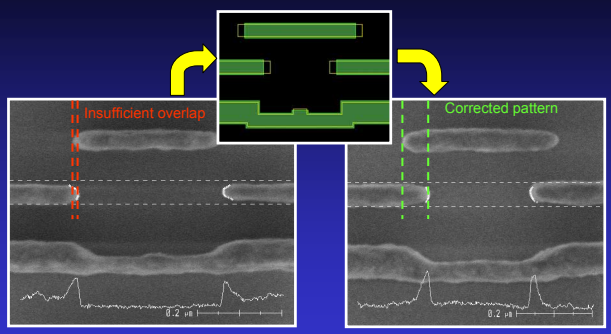
E-beam Proximity Correction (EBPC)



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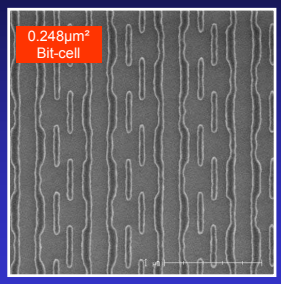
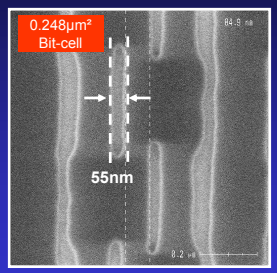
OD Patterning

Top view after e-beam lithography



Top view after STI Module



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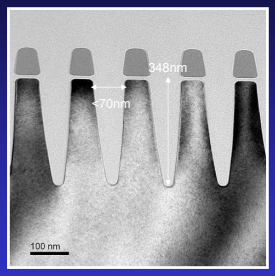
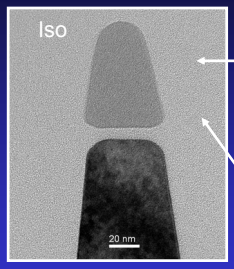
Advanced Gapfill Process





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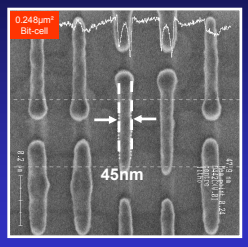
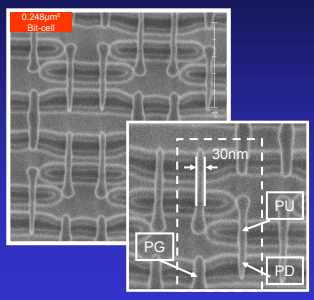
Gate level patterning

Top view after e-beam lithography



Top view after Gate Etch



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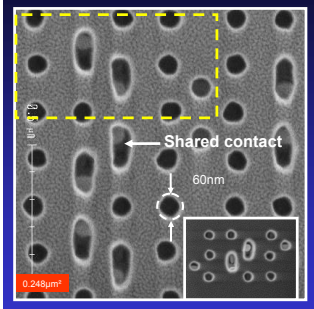
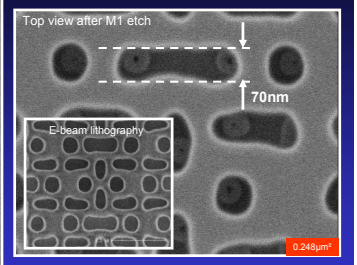
Contact and M1 Patterning





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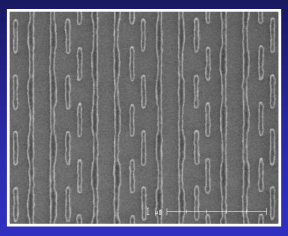
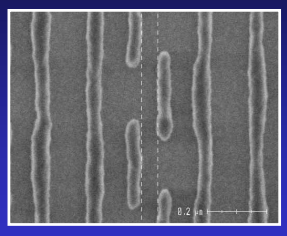
Going towards 32nm with e-beam

OD of 0.178µm² 6T SRAM Bit-cell



OD of 0.124µm² 6T SRAM Bit-cell



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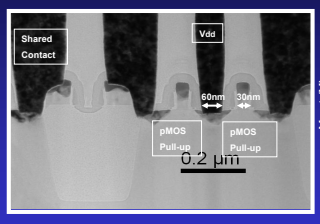
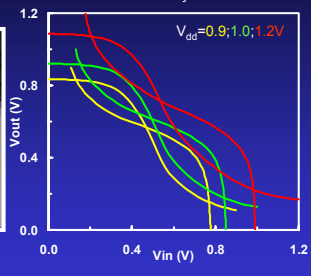
0.334µm² SRAM functionnality

TEM cross section of a 0.334µm² SRAM bit-cell



Measured butterfly caracteristic



(F. Boeuf et al., VLSI 2005)

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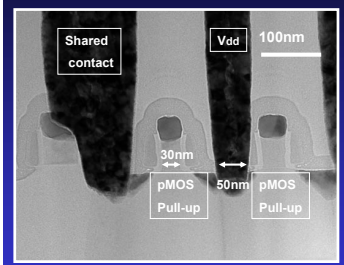
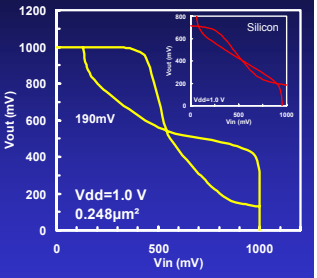
0.248µm² SRAM bit-cell

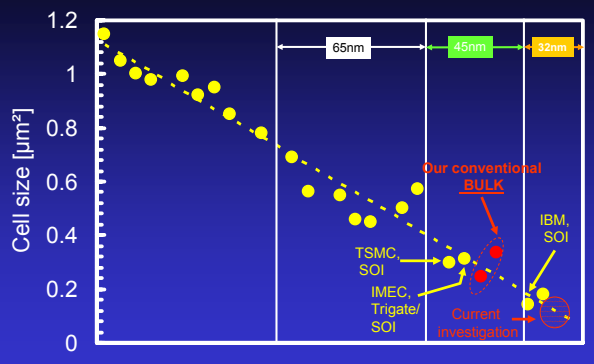


TEM cross section of a 0.248µm² SRAM bit-cell



(F. Boeuf et al., VLSI 2005)

Historical Trend of SRAM bit-cells size

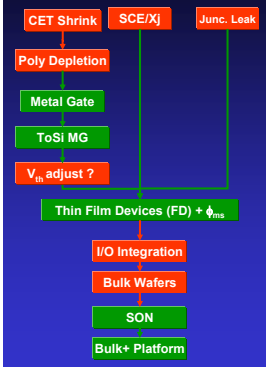


Intermediate Summary

- Conventional 45nm compatible bulk platform achieved
  - Gate oxide scaling limited
  - Dual mobility enhancement technique used
    - Strained-liner combination for nMOS (SMT/CESL)
    - (100) conduction channem for pMOS
  - Integration in 45nm node 6T-SRAM cell achieved
    - e-beam lihography is cost effective
- Remaining issues
  - Improving performance while keeping reasonnable static leakage for Low Power application
  - Reducing junction leakage for LSTP

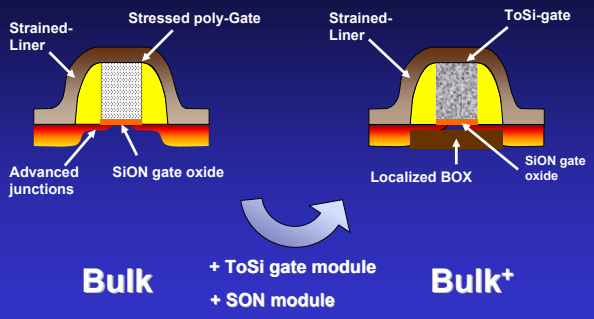
Bulk+ for 45nm node

Objectives



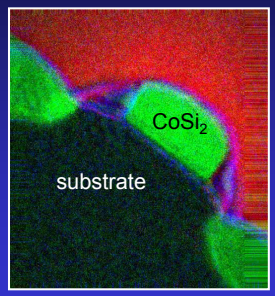
- Correction of Conventional Bulk weakness:
  - Improving CET scaling of conventionnal bulk
  - Improving SCE control
  - Improving Junction leakage
- Integration of Thin-film devices with a single metal gate on bulk substrate
  - Mid-gap gate + thin-film = adjusted Vth for Low Power application
  - Improved SCE (lower DIBL)
  - Low doped channel (better mobility)

From Bulk to Bulk+

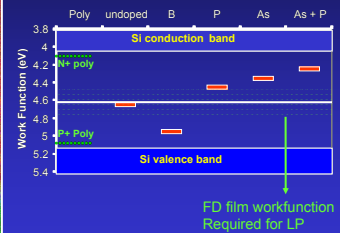


Totally Silicided Gate (ToSi)

CoSi2-ToSi (mid-gap) MOSFET integration
Tavel et al., IEDM 2001



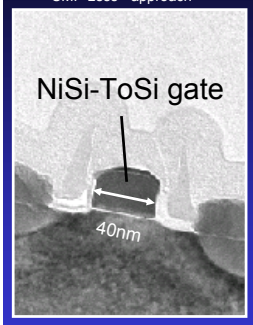
NiSi-ToSi workfunction modulation
Aime et al., IEDM 2004



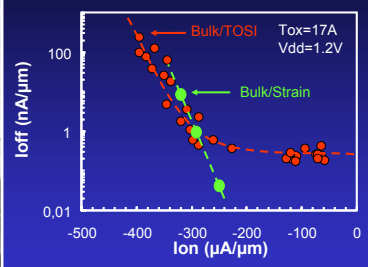
FD film workfunction
Required for LP

ToSi Gate Module

CMP Less - approach

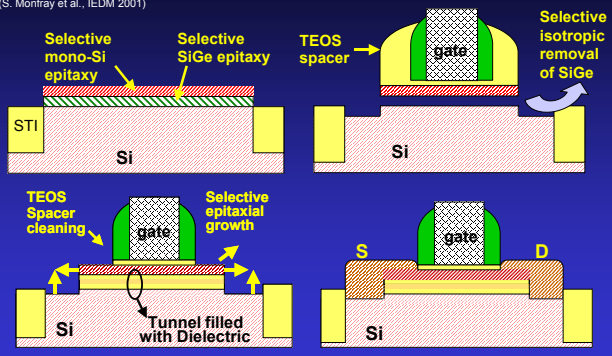


Functionnal Bulk LP Devices

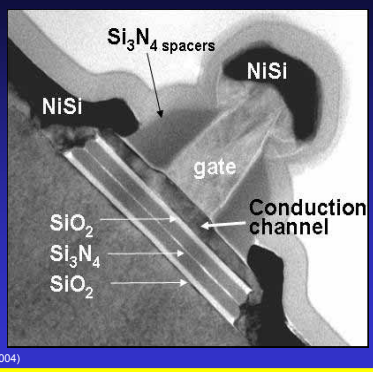


The « Silicon On Nothing » (SON) Technology

(S. Monfray et al., IEDM 2001)

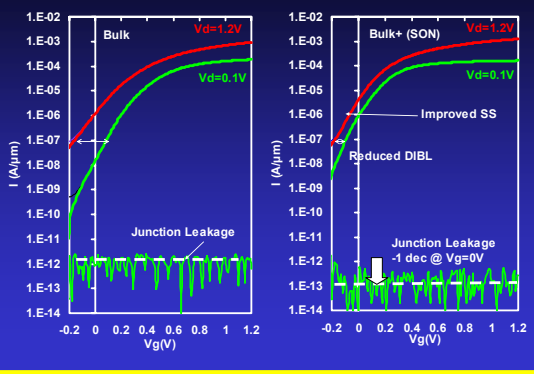


Device Morphology

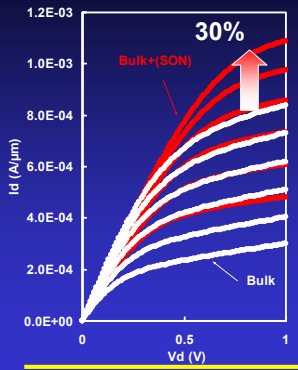


(S. Monfray et al., IEDM 2004)

SON subthreshold behavior

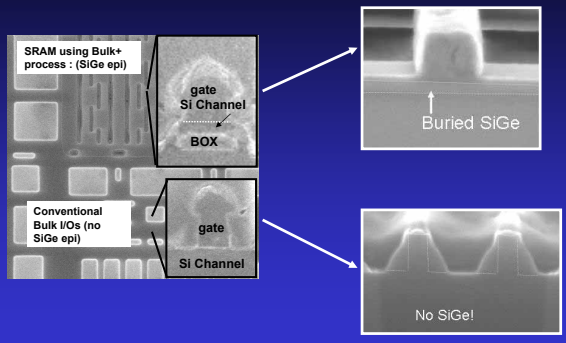


Benefic effect on IDsat

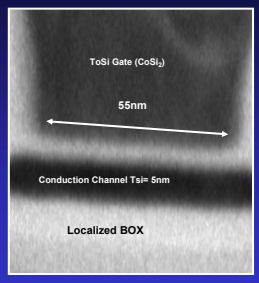


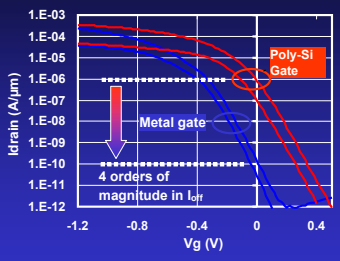
- Bulk+/SON allows a better drivebility due to better subthreshold slope
- Reduced doping allows reduced effective field → improved mobility

Co-Integration of Bulk and Bulk+



Combination of ToSi with SON





Conclusion

- Bulk architecture can be scaled down to 45nm node for Low Cost application
  - Gate oxide scaling is slow down
  - Strain-Si can compensate performance loss
  - Junction can be scaled using ultra-fast anneal
  - Issue : junction leakage ?
- Bulk+ architecture is proposed to solve bulk issue while keeping substrates and co-integration of bulk I/O (IP reuse)
  - Single Metal mid-gap gate with Thin Film devices = Good Vth adjustement for Low Power applications and regular 45nm CET scaling
  - Junction leakage and scaling issues are solved
  - Co-integration with bulk I/O is demonstrated