Current status of PVD Hf-based high-k gate stack
- Process improvement on drive current

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Abstract

The electrical characteristics of high-k transistors using HfO\textsubscript{2} and its silicate gate dielectrics are investigated. These dielectrics are formed by an oxidation of co-sputtered Hf (and Si), followed by nitridation in NH\textsubscript{3} gas. In case of HfSiON gate dielectrics, due to its thermal robustness, lower gate leakage with good uniformity was achieved even after higher thermal treatment. Capacitance reduction due to its lower permittivity compared to HfO\textsubscript{2} is compensated by introducing of Ni-FUSI electrode to reveal high on-state drive current.\cite{1} More highlighted is the effects of SiN capping between Ni-FUSI gate and PVD-high-k dielectric, and post deposition annealing(PDA) to suppress the reaction during FUSI process. The SiN cap was found to increase the yield of transistors, however, it could not suppress the instability of drive current characteristic. The reason for this is considered to be due to an interfacial reaction between high-k and electrode during the NiSi formation.\cite{2} Also, it is noteworthy to arouse that the replacement of poly Si with FUSI gate causes not only the elimination of poly-depletion but also the reduction of EOT.\cite{3} Hereof, by optimizing the PDA condition, as an example, stable decent electrical characteristics were obtained for the Ni-FUSI/SiN/HfO\textsubscript{2} stack, i.e., $I_{on}(n/p) = 600/180$ uA/um at $V_{dd}=20$ pA/um at $V_{dd}=1.1V$. This excellent drivability meets low standby power specification of the MOSFET for 45nm node.

Results and Discussion

Poly Si, Ni-FUSI gated MOS FETs down to $L_g=50nm$ with (SiN)/HfO\textsubscript{2}/HfSiON/SiO\textsubscript{2} were fabricated by a conventional self-aligned process. The SiN capping on HfO\textsubscript{2} can act as a protective layer leading higher transistor yield, however, as shown in Fig.1, it cannot suppress a scatter in the $I_{on}$-$I_{off}$ characteristics. Compared with Poly Si gated FETs, this trend is remarkable for the FUSI/SiN/HfO\textsubscript{2}/SiO\textsubscript{2}-FETs. However, this problematic scattering has been found to be drastically reduced when an elevated PDA temperature treatment is mainly introduced(Fig.2). This implies reaction-related phenomena, i.e., roughness or defects at upper interface between Ni-FUSI and HfO\textsubscript{2} are main causes of the electrical degradation. This is also confirmed by other experiments including $V_{d}-I_{g}$, $I_{g}$-$V_{g}$. In this respect, control of the upper interfacial reaction is a key issue for FUSI/high-k stacks.

By these treatments, excellent performance was obtained for the Ni-FUSI/SiN/HfO\textsubscript{2}/SiO\textsubscript{2}/Si system, i.e., $I_{on}(n/p) = 600/180$ uA/um at $I_{off}=20$ pA/um at $V_{dd}=1.1V$. Meanwhile, different from the HfO\textsubscript{2}, NH\textsubscript{3} treatment plays a role of the SiN capping for Hf-silicate, since Si-N bonds rather than Hf-N can easily be formed in the HfSiO\textsubscript{2}. In case of the FUSI/HfSiON stacks with optimized NH\textsubscript{3} annealing, the scatter in the electrical characteristics was confirmed to be improved. This means the nitrided surface on the HfSiO\textsubscript{2} is capable of protecting from the interfacial reaction. In addition, different from HfO\textsubscript{2}, Hf-silicate stays amorphous with less reaction with Si in the gate even after high temperature annealing(\textgreek{g}1000C).\cite{4} In spite of its lower k value than HfO\textsubscript{2}, the use of HfSiON with Ni-FUSI gate is worthwhile due to its EOT scalability and less gate leakage. Concerning FUSI potentiality, from process controllability point of view, variety of silicide phases can be produced in the gate due to narrowing effect of the gate.\cite{8} Darker contrast in the XTEM image in Fig. 3 indicates a Ni-rich regime, conversely brighter contrast for a less Ni regime. Since each phase has respective work function, the phase control is primary important. Due to the work function

Introduction

For LSTP application, it has been a serious challenge to compromise higher $I_{on}$ with lower $I_{off}$ with a suitable $V_{t}$ value for high-k gate stacks.\cite{4-7} Owing to its high $C_{ox}$ and low EOT, Hf based gate stack with Ni-FUSI has become one of the promising candidate for LSTP application. Ni-FUSI is intensively investigated recently.\cite{8,9} However, it is reported that FUSI/high-k gate stacks have worse uniformity and lower yield of transistors.\cite{10} A systematic approach based on PVD has been employed in this work to enable optimized bi-layered gate stack by engineering the interface. In this talk, we investigate a formation of Hf-based high-k gate dielectric formed by PVD method and demonstrate that the instability of FUSI/high-k system is caused by interfacial reaction between NiSi gate electrode and the high-k gate dielectric.
difference, as shown for the pMOS case in Fig.3, Ni-rich gate can provide lower $V_t$, hence high drivability, while NiSi gate provides higher $V_t$ with poor drivability as indicated by (b) and (a) respectively. We recently confirmed this occasional phase separation could be controllable. This presents a rosy picture. CMOS integration with wide process window is needed in addition to further material research towards potential band-edge (FUSI) gate.

Conclusion

As far as performances are concerned, by suppressing the interfacial reaction between high-k and gate electrode and controlling the phase in the Ni silicide gate, Ni-FUSI/HfSiON gate stack can be promising candidate for LSTP MOSFETs. There are pressing needs for its CMOS integration and reliability confirmation.

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References

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Motivation / Current status
- Platform techniques
  - PVD-Hf based Hi-k dielectric
  - (Ni-)FUSI gate process
- Ni-FUSI/Hf-based High-k
  - Ni-FUSI (NiSi, Ni-rich)
  - Hf-based Hi-k (ex. PVD-HfO2, HfSiON)
- Recent topics
- Conclusion

Current status
Vt control of high-k Tr.

Ch. i/i + Well i/i ➔ impurity conc. is high; Vt ↑ low; SCE

In case of Hi-k Tr ; Vt is fixed due to FLP

Ch. i/i : low or non, counter dope

Reformation of " halo, extension i/i "
+ Immature gate processing (Dry etch etc.)

Performance degradation!

Motivation
In order to introduce to industry, most problematic issues are

Gate electrode: Pure dual metal gates seem to be the best, but ..., 
- FUSI seems to have realistic capabilities at present for its
  - Reusability of Poly Si deposition infrastructure,
  - but complex processing, phase control, ...

Gate dielectric: Among variety of materials and formations, 
- Hf-based high-k seems to have a potential capability
  - intensively investigated, i.e., HfSiOx, HfO2
  - but still problematic, i.e., interfacial reaction related to FLP

Along with CVD, ALD, PVD method has potential capability for its
- simple deposition
- less water content
- less impurity & higher density

Specific PVD formation; “Hf-metal_sputter + RPO”

Starting Surface

Hf-metal_sputter: pure Hf-metal can be deposited uniformly onto any surfaces with high density, less water content.

RPO:
- Hf-metal can be oxidized uniformly by oxygen radicals where Hf takes on blocking layer to suppress Si oxidation at specific low temp.
- Oxidation by RPO leads to a wider process window

Systematic approach (interface/hik)
**Motivation / Current status**

**Platform techniques**
- PVD-Hf based Hi-k dielectric
- (Ni-)FUSI gate process
- Ni-FUSI/Hf-based High-k
  - Ni-FUSI (NiSi, Ni-rich)
  - Hf-based Hi-k (ex. PVD-HfO₂, HfSiON)

**Recent topics**

**Conclusion**

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**PVD-HfO₂ formation**

Why wider process window?

- Oxidation Rate (a.u.)
- Treatment temperature
- Interface preparation (RTO)
- Oxidation (RPO, RTO)
- NH₃ Nitridation for HfSiOₓ
- SiN capping for HfO₂
- Sinter 520°C FGA

**Process flow for Ni-FUSI gated Hi-k Tr.**

1. STI formation
2. Cleaning
3. Interface preparation (RTO)
4. Hf/HfSi co-sputter
5. Oxidation (RPO, RTO)
6. NH₃ Nitridation for HfSiOₓ
7. SiN capping for HfO₂
8. Sinter 520°C FGA
9. Activation anneal
10. Ni S/D silicidation
11. S/D implantation
12. Sidewall formation
13. Halo&Ex. implantation
14. Gate etch
15. High-k removal

**FUSI process**

- Conventional process up to S/D silicidation
- Oxide coating and CMP (stopping on oxide)
- Oxide etch back to expose gate poly and Ni deposition
- RTP silicidation and selective Ni etch
- Oxide clear-out from active area pads

**FUSI CMOS process**

1. Oxide HM
2. CMP of whole area
3. Polysilicon formation
4. Poly etch back

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**Conclusion**
Ni-FUSI gate effect

**Ni-FUSI(NiSi), Poly Si / SiON (Recent results)**

Fixed Vth of PMOS due to FLP has been confirmed to be reduced effectively by means of Ni-rich FUSI gate.

Possible reasons of the EOT reduction

1) Interfacial reaction at FUSI / Hi-k?

2) Extra C caused by band bending due to FLP for Poly Si gate?

3) Interface roughness at FUSI / Hi-k?

4) Other
Ni-FUSI(NiSi), Poly Si / SiN / HfO2
- comparison of FUSI and Poly Si with unoptimized ch. i/i

- Optimization of channel implantation
- maskset problem

Ni-FUSI(NiSi), Poly Si / SiN / HfO2
- comparison of FUSI and Poly Si with optimized ch. i/i

- Optimization of channel implantation
- Vt roll-off; middling performance, but still high Vt for pMOS
- Ni-rich FUSI is Vital for pMOS!

Ni-FUSI(NiSi), Poly Si / SiN / HfO2
- comparison of FUSI and Poly Si with optimized ch. i/i

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• NiSi
• Hf-based Hi-k (ex. PVD-HfO2, HfSiON)
• Recent topics
• Conclusion

PVD-HfSiON

- Crystallized!
- After oxidation without any post annealing

- Hf-silicate remains "amorphous"
- Less [Hf] seems to cause building up of [Hf] at upper part of the film.
CVD-HfSiON remained amorphous even after annealing at 1100°C.

M. Koyama et al., IEDM 2002

**Ex. nMOS**

- **Ni-FUSI** (Ni-rich) / (SIN) / HfO2
- Comparison between with & w/o SiN capping

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- Comparison between with & w/o SiN capping

**Ni-FUSI** (Ni-rich), Poly Si / SIN / HfO2
- Comparison between Poly & FUSI

**Ni-FUSI** (Ni-rich) / Sin / HfO2
- Comparison between with & w/o SiN capping

**Hypothesis:**
Origin of the spread behavior micro holes in the SiNy SIN interface roughness

**PDA optimization:**
(700°C → 1000°C)

**Surface prep. is very important!**
Ni-FUSI(Ni-rich) / SiN / HfO₂ 

Owing to new PDA treatment & SiN capping, 

Ni-rich(excessive Ni silicidation), not interfacial reaction

Ex. nMOS

Mobility decreases a little, however....

The EOT resulted in decreased by 0.1nm. This EOT reduction can compensate the mobility degradation.

Recent topics

- By further optimization (film, process);
  by means of Ni-rich FUSI for pMOS with Vt < 0.4 V
  \[ I_{on} (n/p) = 610/230 \text{ uA/um} \]
  at \( I_{off} = 20 \text{ pA/um} @ V_{dd} = 1.1 \text{ V} \)
  \[ = 650/210 \text{ uA/um} \]
  at \( I_{off} = 20 \text{ pA/um} @ V_{dd} = 1.1 \text{ V} \)
  by PVD-HfO₂
- Ni-FUSI CMOS Integration with revised FUSI process

Conclusions

- Ni-FUSI/ PVD-Hf based high-k gate stack
  - Not only the elimination of poly-depletion but also reduction of EOT is induced by introducing the Ni-FUSI gate (SiON, HfO₂)
  - Amorphous state leads to thermally robust (HfSiON)
  - Tr performance improvement (HfO₂)
    - SiN cap and PDA optimization leads to coordinate Vt-Lg & higher \( I_{on} \)
    - Ni-FUSI(NiSi) gate leads to higher \( I_{on} \) (nMOS)
    - Ni-rich FUSI gate leads to higher \( I_{on} \) (pMOS)
  - \( I_{on} (n/p) = <650 / <230 \text{ uA/um} @ I_{off} = 20 \text{ pA/um} @ V_{dd} = 1.1 \text{ V} \)
Implementability for LSTP application (on trial)
Poly Si(PS), FUSI(FS), Metal Gate(MG) vs Hi-k and SiON

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<tr>
<th>Gate</th>
<th>Thermal Budget</th>
<th>Poly/Si</th>
<th>FUSI</th>
<th>Metal Gate</th>
<th>45nm?</th>
<th>32nm?</th>
<th>45nm?</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO2</td>
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<td>😛</td>
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<tr>
<td>HfSiON</td>
<td>45nm?</td>
<td>😛</td>
<td>😛</td>
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<td>😛</td>
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<td>SiON</td>
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No solution, room to study, Achievable solution on going

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