# Current status of PVD Hf-based high-k gate stack - Process improvement on drive current

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*[3] IMEC vzw, 75 Kappeldreef, B-3001, Leuven, Belgium*

## Abstract

The electrical characteristics of high-k transistors using $HfO_2$ and its silicate gate dielectrics are investigated. These dielectrics are formed by an oxidation of co-sputtered Hf (and Si), followed by nitridation in $NH_3$ gas. In case of HfSiON gate dielectrics, due to its thermal robustness, lower gate leakage with good uniformity was achieved even after higher thermal treatment. Capacitance reduction due to its lower permittivity compared to $HfO_2$ is compensated by introducing of Ni-FUSI electrode to reveal high on-state drive current.[1] More highlighted is the effects of SiN capping between Ni-FUSI gate and PVD-high-k dielectric, and post deposition annealing(PDA) to suppress the reaction during FUSI process. The SiN cap was found to increase the yield of transistors, however, it could not suppress the instability of drive current characteristic. The reason for this is considered to be due to an interfacial reaction between high-k and electrode during the NiSi formation.[2] Also, it is noteworthy to arouse that the replacement of poly Si with FUSI gate causes not only the elimination of poly-depletion but also the reduction of EOT.[3] Hereof, by optimizing the PDA condition, as an example, stable decent electrical characteristics were obtained for the Ni-FUSI/SiN/$HfO_2$ stack, i.e., *$I_{on}$(n/p) = 600/180 uA/um at $I_{off}$ = 20 pA/um at $V_{dd}$=1.1V*. This excellent drivability meets low stand-by power specification of the MOSFET for 45nm node.

## Introduction

For LSTP application, it has been a serious challenge to compromise higher $I_{on}$ with lower $I_{off}$ with a suitable $V_t$ value for high-k gate stacks.[4-7] Owing to its high $C_{inv}$ and low EOT, Hf based gate stack with Ni-FUSI has become one of the promising candidate for LSTP application. Ni-FUSI is intensively investigated recently.[8,9] However, it is reported that FUSI/high-k gate stacks have worse uniformity and lower yield of transistors.[10] A systematic approach based on PVD has been employed in this work to enable optimized bi-layered gate stack by engineering the interface. In this talk, we investigate a formation of Hf-based high-k gate dielectric formed by PVD method and demonstrate that the instability of FUSI/high-k system is caused by interfacial reaction between NiSi gate electrode and the high-k gate dielectric.

### Results and Discussion

Poly Si, Ni-FUSI gated MOS FETs down to $L_g$ = 50nm with (SiN)/$HfO_2$,HfSiON/$SiO_2$ were fabricated by a conventional self-aligned process. The SiN capping on $HfO_2$ can act as a protective layer leading higher transistor yield, however, as shown in Fig.1, it cannot suppress a scatter in the $I_{on}$-$I_{off}$ characteristics. Compared with Poly Si gated FETs, this trend is remarkable for the FUSI/SiN/$HfO_2$/$SiO_2$-FETs. However, this problematic scattering has been found to be drastically reduced when an elevated PDA temperature treatment is mainly introduced(Fig.2). This implies reaction-related phenomena, i.e., roughness or defects at upper interface between Ni-FUSI and $HfO_2$ are main causes of the electrical degradation. This is also confirmed by other experiments including $V_t$-$L_g$, $J_g$-$V_g$. In this respect, control of the upper interfacial reaction is a key issue for FUSI/high-k stacks.

By these treatments, excellent performance was obtained for the Ni-FUSI/SiN/$HfO_2$/$SiO_2$/Si system, i.e., *$I_{on}$ (n/p) = 600/180 uA/um with $I_{off}$ =20 pA/um at $V_{dd}$=1.1V.*

Meanwhile, different from the $HfO_2$, $NH_3$ treatment plays a role of the SiN capping for Hf-silicate, since Si-N bonds rather than Hf-N can easily be formed in the $HfSiO_x$. In case of the FUSI/HfSiON stacks with optimized $NH_3$ annealing, the scatter in the electrical characteristics was confirmed to be improved. This means the nitrided surface on the $HfSiO_x$ is capable of protecting from the interfacial reaction. In addition, different from $HfO_2$, Hf-silicate stays amorphous with less reaction with Si in the gate even after high temperature annealing(>1000C).[4] In spite of its lower k value than $HfO_2$, the use of HfSiON with Ni-FUSI gate is worthwhile due to its EOT scalability and less gate leakage. Concerning FUSI potentiality, from process controllability point of view, variety of silicide phases can be produced in the gate due to narrowing effect of the gate.[8] Darker contrast in the XTEM image in Fig. 3 indicates a Ni-rich regime, conversely brighter contrast for a less Ni regime. Since each phase has respective work function, the phase control is primary important. Due to the work function

difference, as shown for the pMOS case in Fig.3, Ni-rich gate can provide lower $V_t$, hence high drivability, while NiSi gate provides higher $V_t$ with poor drivability as indicated by (b) and (a) respectively. We recently confirmed this occasional phase separation could be controllable. This presents a rosy picture. CMOS integration with wide process window is needed in addition to further material research towards potential band-edge (FUSI) gate.

## Conclusion

As far as performances are concerned, by suppressing the interfacial reaction between high-k and gate electrode and controlling the phase in the Ni silicide gate, Ni-FUSI/ HfSiON gate stack can be promising candidate for LSTP MOSFETs. There are pressing needs for its CMOS integration and reliability confirmation.


## Acknowledgements

Authors would like to thank Dr. A. Lauwers and Dr. J. A. Kittle at IMEC for their FUSI technology.


## References


[1] K. Yamamoto et al., Proc. of INFOS, p198 (2005).
[2] R. Mitsuhashi et al., Proc. of INFOS, p7 (2005).
[3] M.Niwa et al., NATO Advanced Research Workshop on "Defects in Adcvanced High-k Dielectrics", St. Petersburg, 2005 to be published.
[4] M. Koyama et al., IEDM Tech. Digest, San Francisco, 2002, p.849.
[5] J. Kedzierski et al., IEDM Tech. Digest, Washington DC, 2003, p.315.
[6] Y. Tamura et al., Symp. on VLSI Technology, Honolulu, 2004, p.210.
[7] E. P. Gusevet al., IEDM Tech. Digest, San Francisco, 2004, p.79.
[8] J. A. Kittle et al., Symp. on VLSI Technology, Kyoto, 2005, p.72.
[9] S. Kubicek et al., Symp. on VLSI-TSA, Hsinchu, 2005, p.99.
[10] C. S. Park et al., IEDM Tech. Digest, San Francisco, 2004, p299.


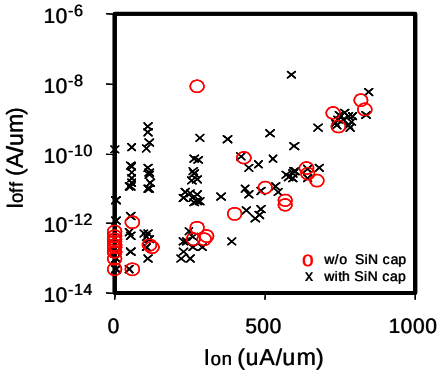


**Fig. 1** SiN capping effect on $I_{on}$-$I_{off}$ characteristics for FUSI/$HfO_2$ (nMOS)

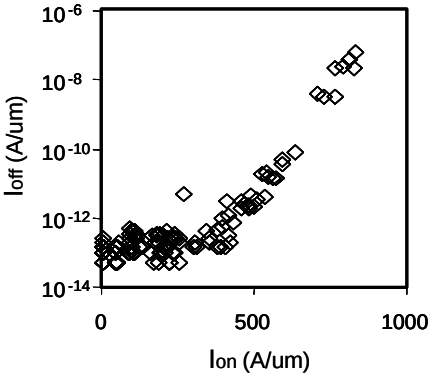


**Fig. 2** $I_{on}$-$I_{off}$ of FUSI/SiN/$HfO_2$ after optimized PDA (nMOS).

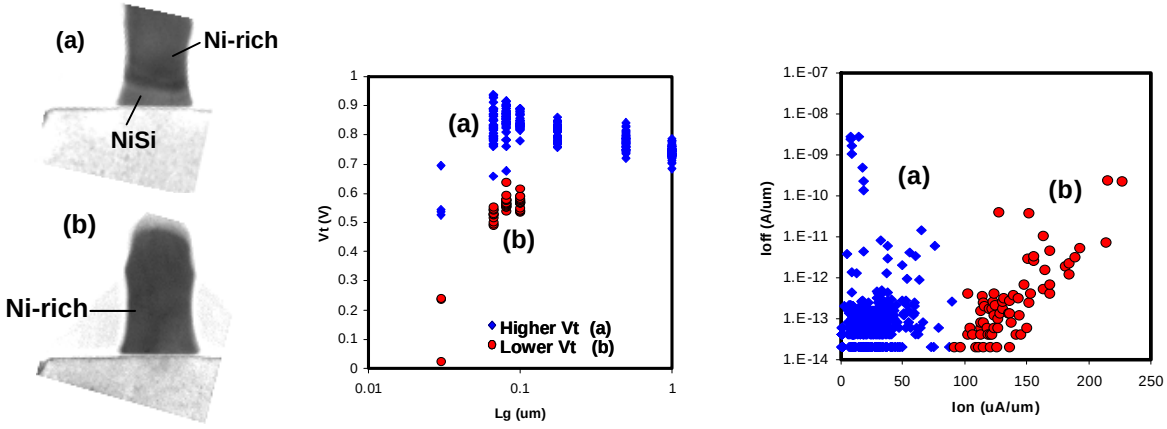


**Fig. 3** XTEM of Ni-FUSI/SiN/$HfO_2$ for pMOS. (a) indicates less Ni(Ni-rich) phase at lower(upper) part of the FUSI gate, and Ni-rich phase in the gate for (b). Darker contrast corresponds to Ni-rich regime. $L_g$ dependence on $V_t$ and $I_{on}$-$I_{off}$ characteristics with respect to (a) and (b) are also shown.

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- Motivation / Current status
- Platform techniques
  - PVD-Hf based Hi-k dielectric
  - (Ni-)FUSI gate process
- *Ni-FUSI/Hf-based High-k*
  - *Ni-FUSI (NiSi, Ni-rich)*
  - *Hf-based Hi-k (ex. PVD-$HfO_2$, HfSiON)*
- Recent topics
- Conclusion





## Current status

**$V_t$ control of high-k Tr.**

Ch. i/i + Well i/i ⇨ impurity conc. is high; $V_t$ ↑
low ; SCE

In case of Hi-k Tr ; $V_t$ is fixed due to FLP

⇨ Ch i/i : low or non , counter dope
⇩
Reformation of " halo, extention i/i "
+ Immature gate processing(Dry etch etc.)
⇩
*Performance degradation !*

Never ending cycle !





## Motivation

*In order to introduce to industry, most problematic issues are*

- ***Gate electrode*; Pure dual metal gates** seem to be the best, but ,,,,
  - FUSI seems to have realistic capabilities at present for its
    - Reusability of Poly Si deposition infrastructure,
    - but complex processing, phase control ,,,,
- ***Gate dielectric*;** Among variety of materials and formations,
  - Hf-based high-k seems to have a potential capability
    - intensively investigated, i.e., HfSiOx, $HfO_2$
    - but still problematic, i.e., **interfacial reaction related to FLP**
  - Along with CVD, ALD, **PVD method** has potential capability for its
    - simple deposition
    - less water content
    - less impurity & higher density





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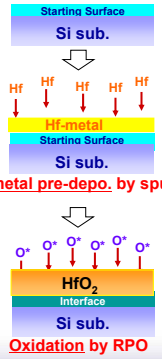
## Specific PVD formation; "Hf-metal_sputter + RPO"




Hf-metal pre-depo. by sputter

Oxidation by RPO
(Remote Plasma Oxidation)

**Hf-metal_sputter:**
pure Hf-metal can be deposited uniformly onto any surfaces with high density, less water content.

+

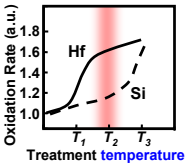
**RPO:**
Hf-metal can be oxidized uniformly by oxygen radicals where Hf takes on blocking layer to suppress Si oxidation at specific low temp.
⇨ **IL thickness control**

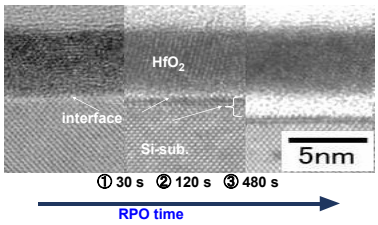
⇩

*Systematic approach (interface/hik) leads to a wider process window*

## PVD-$HfO_2$ formation

**Why wider process window?**





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  - PVD-Hf based Hi-k dielectric
  - **(Ni-)FUSI gate process**
- Ni-FUSI/Hf-based High-k
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## Process flow for Ni-FUSI gated Hi-k Tr.

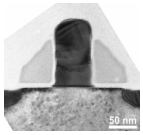
- STI formation
- Cleaning
- Interface preparation (RTO)
- Hf/HfSi co-sputter
- Oxidation (RPO, RTO)
- PDA for $HfO_2$
- $NH_3$ Nitridation for $HfSiO_x$
- SiN capping for $HfO_2$
- Poly-Si
- Gate etch
- High-k removal
- Halo&Ex. implantation
- Sidewall formation
- S/D implantation
- Activation anneal
- Ni S/D silicidation
- Sinter 520°C FGA

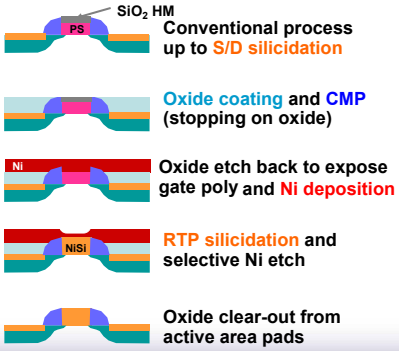
**FUSI process**





## FUSI process

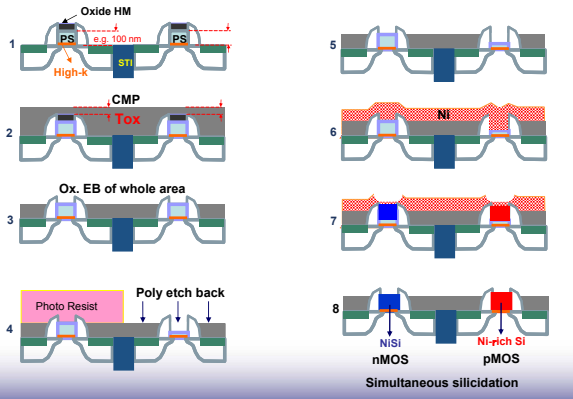







## FUSI CMOS process





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  - PVD-Hf based Hi-k dielectric
  - (Ni-)FUSI gate process
- **Ni-FUSI/Hf-based High-k**
  - **Ni-FUSI (Electrical results wrt NiSi, Ni-rich)**
  - Hf-based Hi-k (ex. PVD-$HfO_2$, HfSiON)
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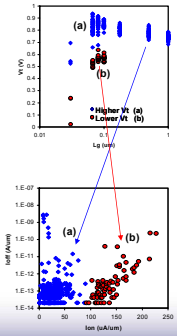
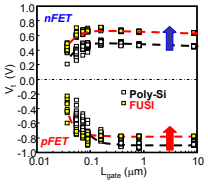
## Ni-FUSI gate effect

**pMOS case** *(in earlier days)*




Influence of Ni-FUSI on Vt



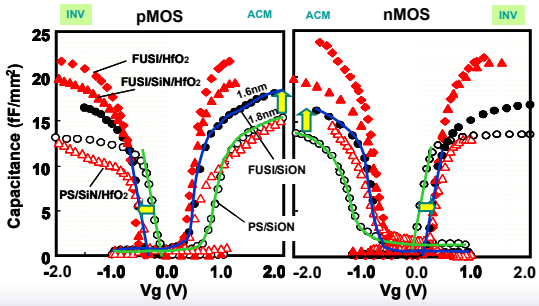

By Ni(-rich) FUSI,
Vt ↑ for nMOS &
↓ for pMOS





## Ni-FUSI(NiSi), Poly Si / SiON

SiON; PS → FUSI ⇒ EOT; 0.2nm ↓, CET; 0.5nm ↓ , |Vt |; ↑

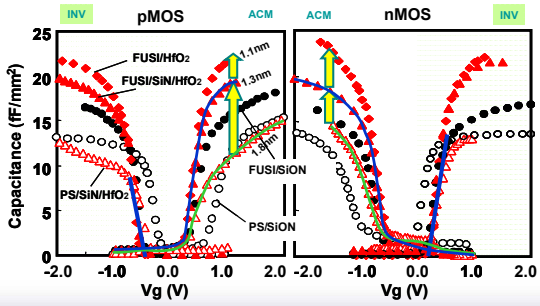







## Ni-FUSI(NiSi), Poly Si / (SiN) / HfO2

~~SiN~~/HfO2 ; PS → FUSI ⇒ EOT; 0.5nm ↓ , |Vt |; ⇒ EOT; 0.7nm ↓




Not only elimination of Poly depletion, but also *REDUCTION of EOT* !
- Reduction; HfO2 > SiON for FUSI gate

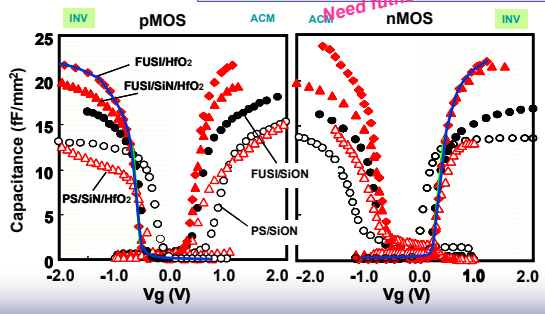




## Ni-FUSI(NiSi) / HfO2

FUSI/HfO2 stack w/o SiN cap ⇒ CET ; 1.6nm (pMOS), 1.4nm (nMOS)
Vt ; - 0.6 V (pMOS), 0.4 V (nMOS w/o ch. i/i)

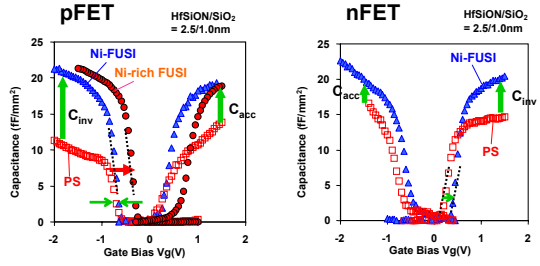
Need futher improvement !








## Ni-FUSI(Ni-rich), Poly Si / HfSiON (Recent results)




Fixed $V_{fb}$ of PMOS due to FLP has been confirmed to be reduced effectively by means of Ni-rich FUSI gate





## Possible reasons of the EOT reduction

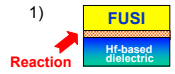
*1) Interfacial reaction at FUSI / Hi-k?*

*2) Extra C caused by band bending due to FLP for Poly Si gate?*

*3) Interface roughness at FUSI / Hi-k?*

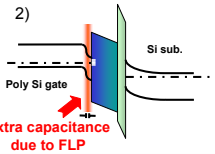
*4) Other*

1)




Due to reaction at the interface, EOT decreases

2)



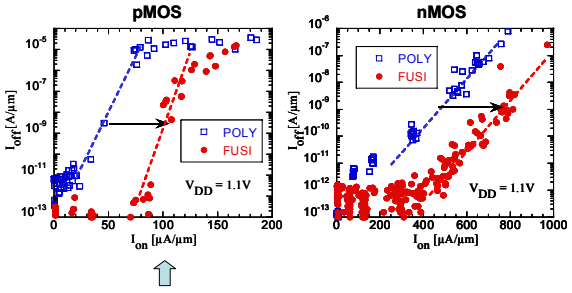

Due to additional C by FLP, total $C_{inv}$ is reduced, hence CET increases

3)


Due to roughness at the interface, C is increased, hence EOT decreases

## Ni-FUSI(NiSi), Poly Si / SiN / $HfO_2$

- comparison of FUSI and Poly Si with unoptimized ch. i/i



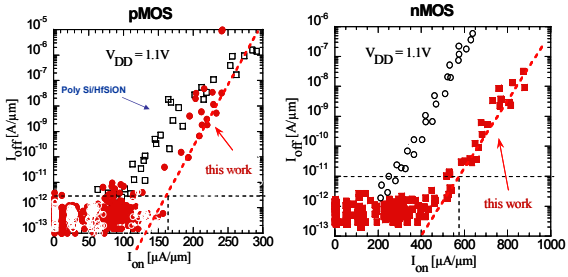

- Optimization of channel implantation
- maskset problem





## Ni-FUSI(NiSi), Poly Si / SiN / $HfO_2$

- comparison of FUSI and Poly Si with optimized ch. i/i




□ ◇ ; Poly Si / HfSiON, the best published data(Y. Tamura et al., IEDM 2004, p.210)





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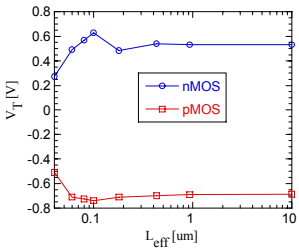
- comparison of FUSI and Poly Si with optimized ch. i/i



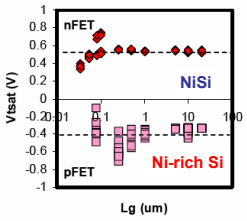

Vt roll-off; middling performance, but still high Vt for pMOS

→ Ni-rich FUSI is Vital for pMOS !



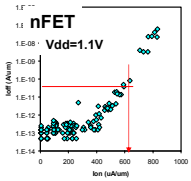


## Tr properties for Ni-FUSI(Ni-rich) gate for pMOS($HfO_2$)

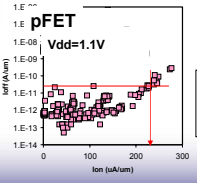



Long channel Vt < 0.4V

$I_{on}$ = 610/230uA/um
($I_{off}$ = 20pA, $V_{dd}$ = 1.1V)




Acceptable $I_{on}$ due to EOT and $T_{inv}$ reduction.




$I_{on}$ has been improved much due to lower Vt.





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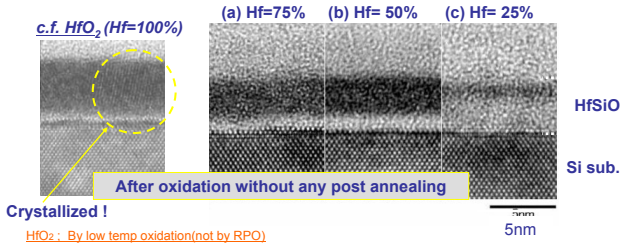
## PVD-HfSiON




- Hf-silicate remains "amorphous"
- Less [Hf] seems to cause building up of [Hf] at upper part of the film.


CVD-HfSiON remained amorphous even after annealing at 1100C.

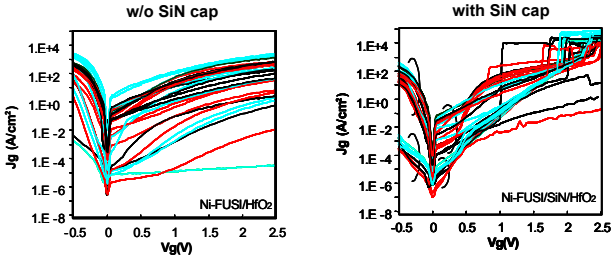
**M. Koyama et al., IEDM 2002**





## Ex. nMOS Ni-FUSI(Ni-rich) / (SiN) / HfO2

**- Comparison between with & w/o SiN capping**





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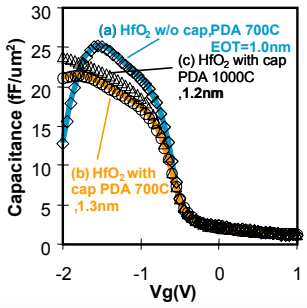


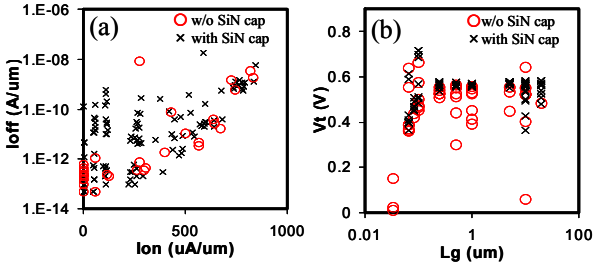

**Due to SiN cap, EOT increases (1.0nm ⟶ 1.3nm)**





## Ex. nMOS Ni-FUSI(Ni-rich) / (SiN) / HfO2

**- Comparison between with & w/o SiN capping**




- Trs w/o SiN cap : low yield
- Trs with SiN cap : spread data

- Trs w/o SiN cap : wide spread Vt
- Trs with SiN cap : coordinated

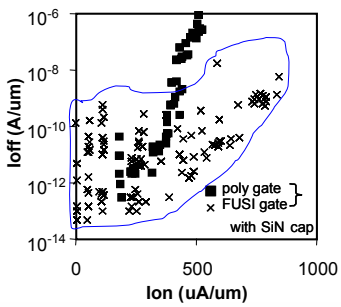
**SiN cap is not always effective !**



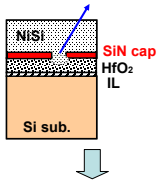


## Ex. nMOS Ni-FUSI(Ni-rich), Poly Si / SiN / HfO2

**- Comparison between Poly & FUSI**




**Hypothesis:**
Origin of the spread behavior
- micro holes in the flimsy SiN
- Interface roughness



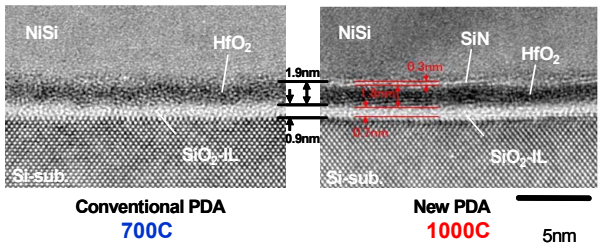

***PDA optimization ! ( 700C ➡ 1000C )***

**Wide spread characteristics for the FUSI/SiN/HfO2**
**Why ??**





## Ex. nMOS Ni-FUSI(Ni-rich) / SiN / HfO2




**Conventional PDA**
**700C**

**New PDA**
**1000C**

- No distinct direct evidence was observed
- SiN disappeared at 700C PDA
- SiN clearly observed at 1000C PDA

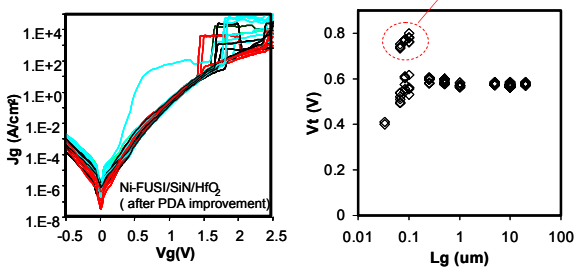
⇨ *Surface prep. is very important !*

## Ni-FUSI(Ni-rich) / SiN / $HfO_2$

imec Ex. nMOS

Owing to
new PDA treatment & SiN capping,

Ni-rich(excessive Ni silicidation),
not interfacial reaction



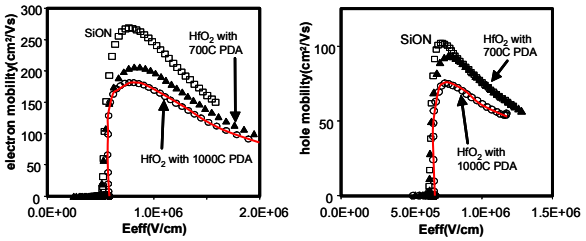

(a) (b)





## Ni-FUSI(Ni-rich) / SiN / $HfO_2$, SiON

imec Ex. nMOS



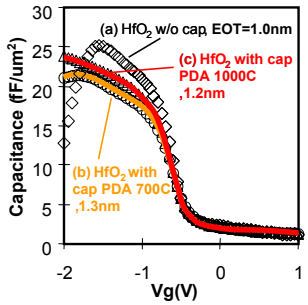

Mobility decreases a little, however,,,,





## Ni-FUSI(Ni-rich) / (SiN) / $HfO_2$

imec Ex. nMOS



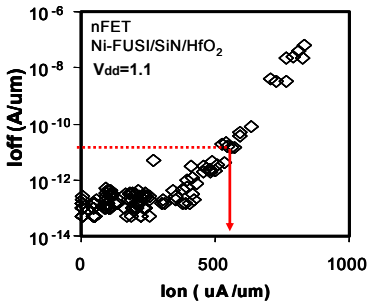

The EOT resulted in decreased by 0.1nm.
This EOT reduction can compensate the mobility degradation.





## Ni-FUSI(Ni-rich) / SiN / $HfO_2$

imec Ex. nMOS




Owing to *SiN capping* combined with *optimized PDA*,

$I_{on}$ (n/p) = 600/180 uA/um at $I_{off}$ =20 pA/um at $V_{dd}$ = 1.1 V





## Recent topics

- By further optimization (film, process);

by means of Ni-rich FUSI for pMOS with $V_t$ < 0.4 V

$I_{on}$ (n/p) = 610/230 uA/um
at $I_{off}$ =20 pA/um @ $V_{dd}$ = 1.1 V
by PVD-$HfO_2$
= 650/210 uA/um
at $I_{off}$ =20 pA/um @ $V_{dd}$ = 1.1 V
by PVD-HfSiON

FUSI CMOS Integration with revised FUSI process





## Conclusions

***Ni-FUSI/ PVD-Hf based high-k gate stack***

- Not only the elimination of poly-depletion but also reduction of EOT is induced by introducing the Ni-FUSI gate (SiON, $HfO_2$)
- Amorphous state leads to thermally robust (HfSiON)
- Tr performance improvement ($HfO_2$)
  - SiN cap and PDA optimization leads to coordinate $V_t$-$L_g$ & higher $I_{on}$
  - Ni-FUSI(NiSi) gate leads to higher $I_{on}$ (nMOS)
  - Ni-rich FUSI gate leads to higher $I_{on}$ (pMOS)

$I_{on}$ (n/p) = <650 / <230 uA/um at $I_{off}$ =20 pA/um at $V_{dd}$= 1.1 V

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## Implementability for LSTP application (on trial)

Poly Si(PS), FUSI(FS), Metal Gate(MG) vs Hi-k and SiON

| | Gate | | | Thermal Budget | $I_{on}/I_{off}$ | EOT | $J_g$ |
|---|---|---|---|---|---|---|---|
| | PS | FS | MG | | | | |
| $HfO_2$ | | | 32nm? | ☹? | ☺ | ☺ | ☺ |
| HfSiON | | 45nm? | 45nm? | ☺ | ☺ | ☺ | ☺ |
| SiON | | 45nm? | | | | ☹ | ☹ |

■ : No solution, ☹ ■: room to study, ■: Achievable ☺ solution on going





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***Thank you !***