A 0.95mW/1.0Gbps Spiral-Inductor Based Wireless Chip-Interconnect with Asynchronous Communication Scheme

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Abstract

This paper presents a reduction method of power consumption and an asynchronous communication scheme for spiral-inductor based wireless chip-interconnect. The power reduction is achieved by utilizing positively resonance phenomena between two spiral inductors. Further, employing dynamic circuits and self pre-charging technique realizes an asynchronous communication without any clocking. The methodology was verified and evaluated by measuring a test chip in 0.18μm 6 metal CMOS technology. The performance of 0.95mW/1.0Gbps/ch was achieved without any clocking.

Introduction

In a 3D-IC fabrication technique, small stacked via-hole technologies are now under development but the processing cost and yield problems are still unresolved [1]. To solve these problems, wireless interconnect using capacitive coupling between small pads [2] and wireless interconnect based on inductive coupling of spiral inductors [3],[4] were proposed. The former requires small pad-to-pad distance of 1-2μm. The latter is not applicable to parallel connections because of its large power consumption, and it requires a complex synchronization scheme. In this manuscript, a reduction method of power consumption and an asynchronous communication scheme without any clocking are proposed for the spiral-inductor based wireless chip-interconnect. The power reduction is very important for parallel interconnects between neighboring chips, which distribute 2D data such as image data in stacked 3D-IC systems [5].

Reduction of Power Consumption

The inductive coupling structure has self-resonance frequencies and it will be utilized for reducing the power consumption in the wireless chip-interconnect. As shown in Fig.1, an nMOS FET excites the spiral inductor pair by pulse. The spiral inductors are modeled as π–type equivalent circuits with magnetic coupling "k". Spice simulation results are shown in Fig.2. Let us consider, first, a case of the wide-width pulse shown at the left hand. Two damping oscillations appear on the output node, at the times when the input pulse rises and falls. However, the amplitude at the later is larger than the former one. The difference has been caused by on-conductance of the nMOS FET. The former one arises, in case that the input inductor has conductive connection to the ground due to the nMOS FET. On the other
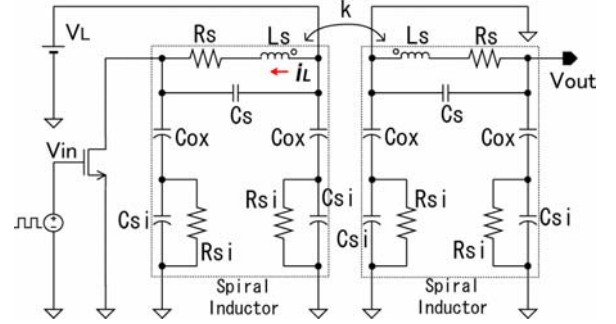

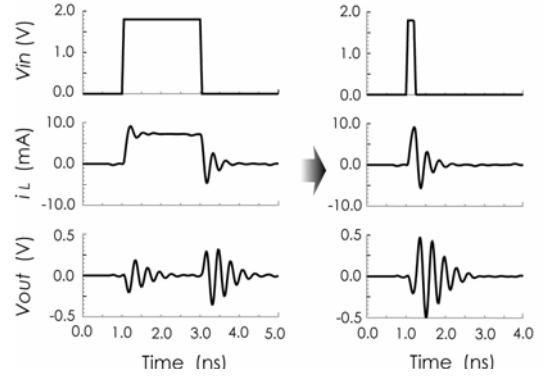Fig.1   Pulse excitation to spiral inductor pair.

Fig.2   Damping oscillations.

hand, two spiral inductors are identical in the later oscillation, because the nMOS FET is off. The identity enlarges the resonance phenomenon and it results in large amplitude. Thus, it is important to generate damping oscillation without on-conductance. Next, let us consider the right hand case in Fig.3. In this case, narrow-width pulse is employed in order to enlarge the amplitude still more, by superposing the two damping oscillations. The pulse width t_{pw} that can superpose the two damping oscillations is :

$$t_{pw} = \frac{1}{2 f_{self}} \tag{1}$$

where f_{self} is the self resonance frequency of the spiral inductor.

Asynchronous Communication Scheme

In order to realize an asynchronous communication, dynamic circuits and self pre-charge technique are employed. Circuit schematics are depicted in Fig.3. The received signal indicated by "V_C" is damping oscillation wave and the center voltage is 0V. First, the signal is level-shifted by C1 and R1

to a bias voltage "Vbn". The shifted signal is indicated by "V_G". The bias voltage "Vbn" can tune the receiving sensitivity by changing the transconductance of M3. The node indicated by "V_D" is dynamically charged up and discharged. M3 discharges the node according to the shifted receiving signal. After discharging, M4 charges up again the node according to the delayed pulse "V_P". This mechanism is called with "self pre-charging". It can regenerate the transmitted pulse V_{TX}" into the received node "V_{RX}", without any clocking scheme. The communication scheme can transmit NRZ signal using "Pulse Generator" (PG) and "Rec. Unit" (RU).
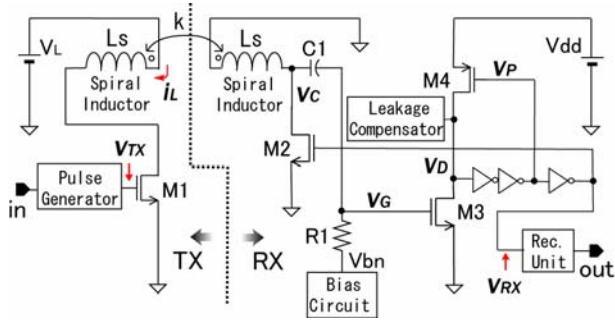
Fig.3   Transmitter and receiver.

Test Chip Fabrication and Measurement

In order to confirm the proposed concept, a test chip was designed and fabricated in 0.18μm 6 metal CMOS technology. Fig.4 shows a micrograph of the test chip and 12 transceivers were integrated. Two chips were set on manipulators in face to face and transfer characteristics were measured. Measured results are shown in Figs.5 and 6. Fig.5 shows transmitted data and received waveforms of the neighboring three channels, where pseudo random data were transmitted at 1.0Gbps. BER (Bit Error Ratio) < 10^{-10} was achieved without cross talk between the neighboring spiral inductors. The delay time was 2.7ns (=1.2ns[transceiver] + 1.0ns[I/O] + 0.5ns[PCB]). Measured power consumption is shown in Fig.6. "Inductor (Tx)" and "Sensing (Rx)" are powers consumed by the spiral inductor in Tx and the dynamic circuits with pre-charging operation in Rx, respectively. The data activities were set to 0.5. The power consumptions were proportional to the data-rate and they were also reduced proportionally by the activity due to the asynchronous scheme. The power consumptions of PG and RU were relatively large. However, they are CMOS logic circuits and it is expected that the power consumptions are reduced in scaled devices.

Conclusions

A reduction method of power consumption and an asynchronous communication scheme without any clocking has been proposed for the spiral-inductor based wireless chip-interconnect. The methodology was verified and evaluated by measuring a test chip in 0.18μm 6 metal CMOS technology. The performance of 0.95mW/1.0Gbps/ch was achieved without any clocking.
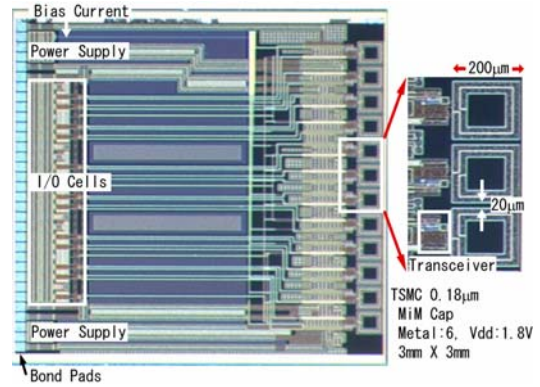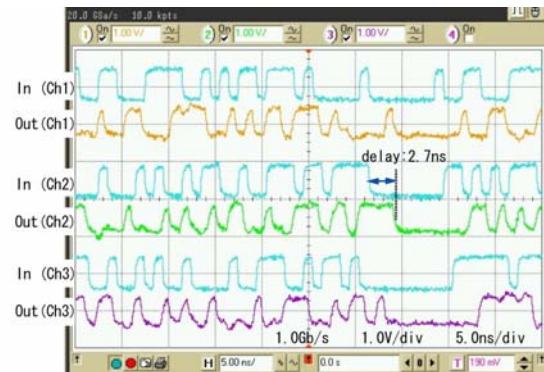

Fig.4   Photomicrograph of test chip.

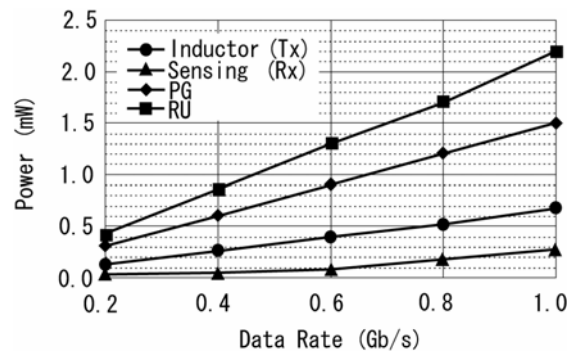Fig.5   Transmitted data and received waveforms.

Fig.6   Measured power consumptions.

References

[1] M. Koyanagi et al., "Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology," *ISSCC Digest of Technical Papers*, pp.270-271, Feb. 2001.

[2] K. Kanda et al., "1.27Gb/s/ch 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Digest of Technical Papers*, pp.186-187, Feb. 2003.

[3] D. Mizoguchi et al. "A 1.2Gb/s/pin Wireless Superconnect Base on Inductive Inter-Chip Signaling (IIS)", *ISSCC Digest of Technical Papers*, pp142-143, 2004.

[4] N. Miura et al. "Analysis and Design of Transceiver Circuit and Inductor Layout for Inductive Inter-Chip Wireless Superconnect", *Dig. of Symp. on VLSI Circuits*, pp.246-249, June, 2004.

[5] A. Iwata et al., "A 3 Dimensional Integration Scheme Utilizing Wireless Interconnections for implementing Hyper Brains," to be published in *ISSCC 2005*.

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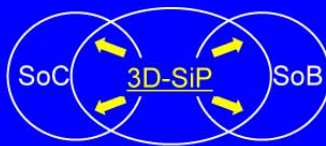
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Outline of Presentation

- Introduction
- Power Reduction Technique
- Asynchronous Communication
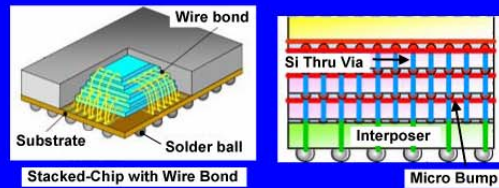- Measurement Results
- Conclusions

Introduction

SoC — 3D-SiP — SoB

SoC : System on Chip
3D-SiP: System in Package
SoB : System on Board

- Short TAT
- Lower cost
- Larger bandwidth
- Different types of functional devices (Memory, Logic, Analog)

3D Interconnect

Wire bond
Substrate
Solder ball
Stacked-Chip with Wire Bond

Si Thru Via
Interposer
Micro Bump

Limited bandwidth   Complicated fabrication

Spiral-Inductor based Interconnect

Instead of "Si Thru Via" and "Micro Bump"

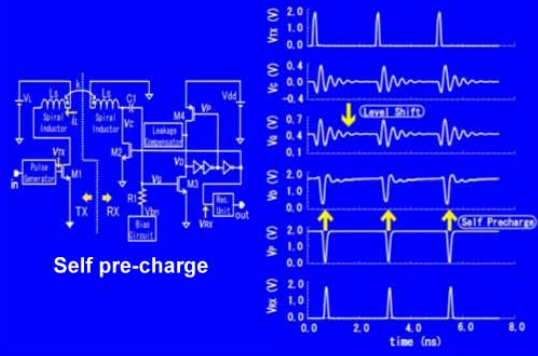| Pros.	Cons.
• No complicated fabrication	• Power consumption
• No ESD protection	• Clocking Scheme
• Large bandwidth	

Key Concept

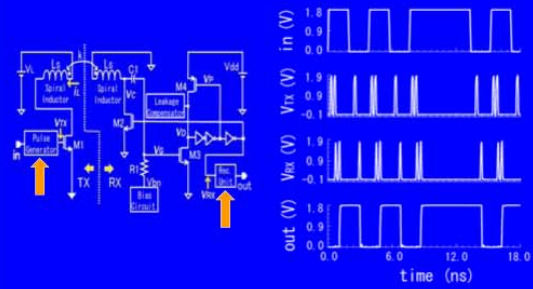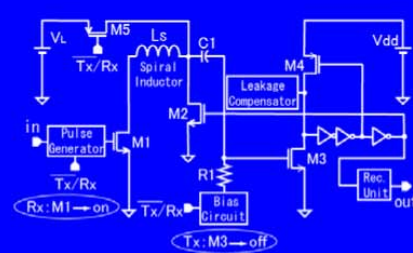$\lambda/2$ Resonance $\lambda/2$

Arbitrary Length   No resonance   Arbitrary Length
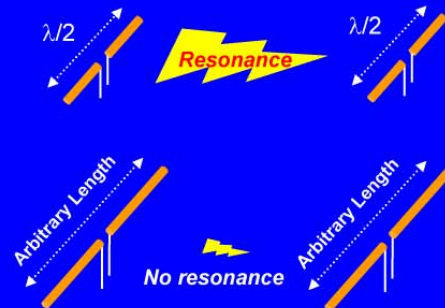
Resonance on Spiral Inductors

$$t_{pw} = \frac{1}{2 f_{self}}$$

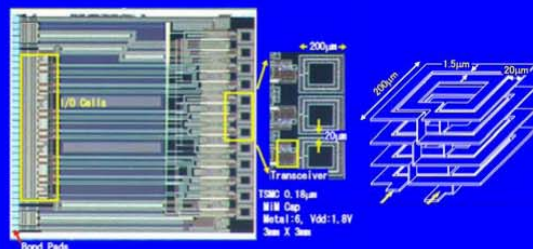## Asynchronous Communication

Self pre-charge
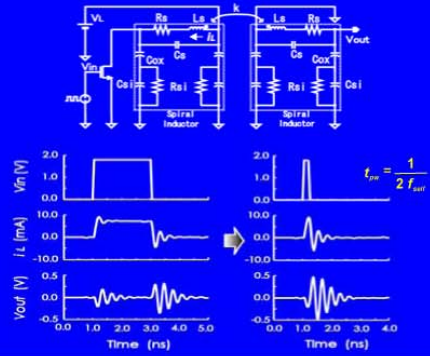
NRZ Communication

Transceiver

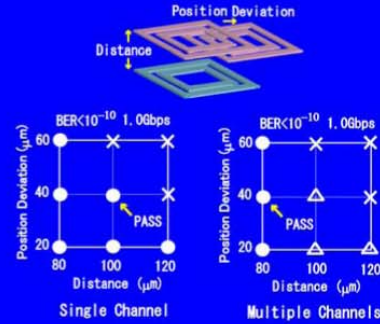## Die Micrograph

Measured Waveforms

In (Ch1)
Out (Ch1)
In (Ch2)
Out (Ch2)
In (Ch3)
Out (Ch3)

Delay:2.7ns

1.0Gb/s   1.0V/div   5.0ns/div
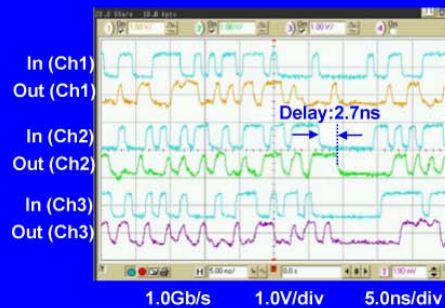
Measured Power Consumptions
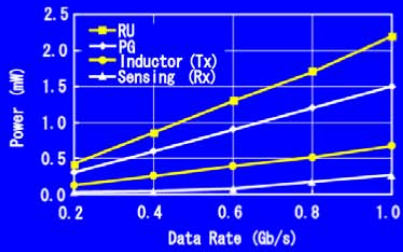
Distance and Position Deviation

Single Channel   Multiple Channels

Performance Comparison

			This work	[1]	[2]
Technology			0.18μm	0.35μm	0.25μm
Communication Distance			100μm	240μm	28μm
Inductor Diameter			200μm	300μm	48μm
Data Rate			1.0Gb/s	1.25Gb/s	1.0Gb/s
Power	Tx	Inductor	0.65mW	43mW	9mW
		PG	1.5mW		
	Rx	Sensing	0.28mW	3mW	2.2mW
		RU	2.2mW		

[1] D.Mizoguchi et al., *ISSCC Dig.* pp.186-187, 2004
[2] N.Miura et al.,   *ISSCC Dig.* pp.264-265, 2005

Conclusions

1. Power reduction by resonation of inductor coupling.
2. Asynchronous Communication with self pre-charging.
3. 0.95mW/1.0Gbps/ch was confirmed by the measurements.
4. It is useful for 3D stacked system.