A Brain-type Vision System using a 3-Dimensional integration with local and global wireless Interconnections

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1. Research Target

The vertebrate visual system processes huge visual information in real-time by massively parallel neural networks arranged hierarchically and adapts to a rapidly changing visual environment by an adaptive mechanism. Inspired by the unique architecture and algorithm of the vertebrate visual system, the neuromorphic vision chips or brain-type vision device, which are novel analog Very Large Scale Integrated (VLSI) circuits, have been fabricated ([1] for outlines). These neuromorphic chips, however, encounter a serious problem, namely, the trade-off between the resolution and the computational complexity of the chip. To solve the problem, multi-chip vision systems have been developed previously [2-3]. In these multi-chip systems, a high resolution and advanced functions are realized by dividing network circuits into separate chips. On the other hand, in our 21st Century COE, a visual processing system using a 3 Dimensional Custom Stack System (3DCSS) has been proposed [4]. In the system, multiple chips fabricated by various technologies and arranged hierarchically are connected by two types of wireless interconnections, which are a local wireless interconnection (LWI) [5] and a global wireless interconnection (GWI) [6]. The LWI can handle huge data, such as 2-dimensional image data, between adjacent chips due to massively parallel structure. The GWI can communicate beyond neighboring chips by microwave. Therefore, the 3DCSS is well-suited for realization of the multi-chip system mimicked the vertebrate visual system. In the present study, we developed a vision system using the 3DCSS configuration.

2. Visual processing chip using the 3DCSS configuration

The visual processing chip was developed to configure the 3DCSS. Fig.1 shows a block diagram of the visual processing chip (3DCSS chip). The chip consists of a cell array, line parallel pulse width modulation (PWM) and demodulation (PWD) circuits, line parallel LWI transmitter and receiver, GWI receivers and a control signal generator.

In the cell array, pixel circuits are arranged in an 80 x 80 matrix. The pixel circuit consists of an analog memory, a resistive network and a sample/hold circuit (S/H). The pixel circuit is the same structure in the prototype visual processing chip [4]. An input image (analog voltage) is smoothed by the resistive network and the extent of the smoothing is controllable by external bias voltages [7]. The S/H is embedded to compensate for circuit offsets [7]. And the output voltage of the S/H varies proportionally to the time-varying input signal; therefore, the S/H can serve as a subtractor circuit.

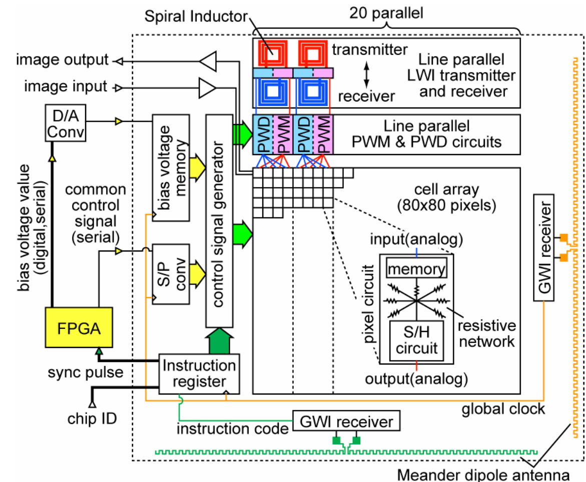

Fig.1 Block diagram of the visual processing chip for the 3DCSS (3DCSS chip).

Note that the analog output image from the cell array must be converted into a digital data in order to use the LWI circuits. Consequently, the PWM and PWD circuits were inserted between the cell array and the LWI circuits. The PWM and PWD circuits are arranged every 4 column of the cell array in a line (1 x 20) to speed up the image transfer, respectively. The PWD circuit consists of switched current sources and an integration capacitor [8]. A pulse width signal from the LWI receiver fed into the switched current source is converted into current pulse and integrated on the capacitor. Accordingly, the output voltage is proportional to the input pulse width. The PWD circuit can serve as a weighted adder-subtractor by controlling the current value and direction. And the PWD circuit was embedded a compensation circuit of the current source mismatches. The PWM circuit consists of a clocked CMOS comparator [8]. The circuit generates a pulse signal until a ramp voltage is equal to the input voltage from the cell array. Thus, the output pulse width is proportional to the pixel output voltage. The ramp voltage is generated from a ramp generator incorporated in the chip. A conversion gain of the PWM is controllable by a gradient of the ramp voltage signals.

The pulse width image data is transferred from the LWI transmitter to the LWI receiver between adjacent chips by using inductive coupling [5]. The LWI transmitter and receiver were the same number as the PWM and PWD, respectively. A maximum transfer rate of the LWI circuits was 250 Mbps/cell and enough for the image data transfer. A distance between chips can be separated up to 150 um.

The LWI circuits are useful for the 2-D image data transfer due to the line parallel structure.

The GWI receiver consists of a meander type dipole antenna and a demodulation circuit. A 2.0 GHz amplitude shift keyed (ASK) signal is received by the dipole antenna and then converted into a 100 MHz pulse signal by the demodulation circuit. The GWI receiver was used to get an instruction code. The instruction code determines operations of each chip, for example, whether the LWI transmitter outputs an image data or not, and processing methods of the cell array and PWD circuit. One GWI receiver generates the instruction code and the other generates a global clock. The instruction code is fed into an instruction register in sync with the global clock. The register of each chip has unique ID number and stored a different instruction for each chip by including the ID number in the instruction code. And then, the control signal generator generates control signals to the cell array, the PWM and the PWD circuits by combining the instruction of each chip and common control signals. The GWI receiver is useful because the instruction code and the global clock must be transferred to every chip.

The 3DCSS chip can be applied to processing mimicked vertebrate visual system due to the resistive network and the PWD circuit, etc. The chip was implemented with a 0.35 um, double-poly, three metals, standard CMOS technology and the die size was 9.8 x 9.8 mm^2. The specifications of the chip are shown in Table I.

Table I Specifications of the 3DCSS chip

Process	CMOS 0.35um 2 Poly 3 Metal
Die size	9.8 x 9.8 [mm^2]
Number of pixels	80(H) x 80(V) [pixel]
Number of LWIs	20 x 2 [cell] (transmitter & receiver)
Power supply	3.3 [V]
GWI receiver circuit	
Antenna length	8010 [um]
Size*1	858.1(H) x 820.0(V) [um^2]
Power consumption	40 [mW]
LWI transmitter & receiver circuit	
Size (Inductor)	1100.0(H) x 400.0(V) [um^2] (300.0(H) x 300.0(V) [um^2])
Number of turns	6 (Top metal: 3, 2nd metal: 3)
Power Consumption*2	5.6 [mW/cell] (transmitter + receiver)
PWM & PWD circuit	
Size	332.4(H) x 344.8(V) [um^2]
Resolution	8 [bit]
Power consumption*2	(PWM) 0.66 [mW/cell] (PWD) 1.70 [mW/cell]
Pixel circuit	
Size	77.1(H) x 86.2(V) [um^2]
Output accuracy*4	6 ~ 8 [bit]
Power consumption	(processing) 64.7 [uW/pixel] (readout) 78.9 [uW/pixel]

*1 Except antenna and wire areas.
*2 Pulse cycle = 2.0 [us], Pulse width = 1.0 [us].
*3 Maximum pulse width = 1.0 [us], Maximum voltage magnitude = 1.0 [V].
*4 Depend on an input image, a smoothing area of the resistive network, and etc.

3. Development of the 3DCSS test module

We developed a 3DCSS test module using the 3DCSS chip. Fig.2 shows a cross-section of the 3DCSS test module.

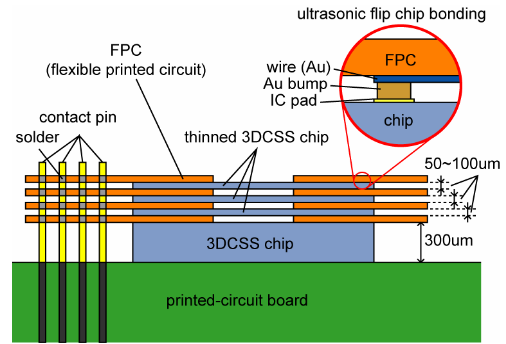

Fig.2 Cross-section of the 3DCSS test module.

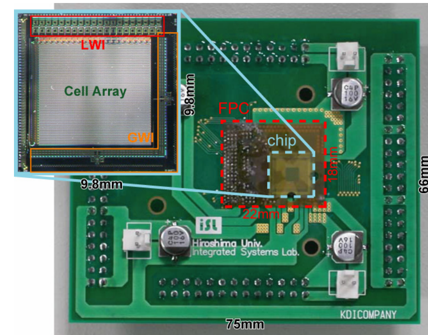

Fig.3 Photo graph of the 3DCSS test module.

We used a flexible printed circuit (FPC) to spacing between chips and wiring of power supplies, input control signals and test outputs since the FPC is very thin and stackable. The 3DCSS chips were thinned to approximate these chips except the lowest chip. The chip was bonded to the FPC by ultrasonic flip chip bonding process. These bonded FPCs were stacked on a printed-circuit board, which was a base board to make the 3DCSS user-friendly, and connected by connect pins. Fig.3 shows the photo graph of the 3DCSS test module.

4. Conclusion and future

We developed the visual processing chip with LWI and GWI. And the chips were developed to the 3DCSS test module. Presently, we conduct verification experiments for the 3DCSS test module.

References–

[1] A. Moini, *Vision Chips* (2000).
[2] C.M. Higgins, *et al.*, Analog Integrated Circuits and Signal Processing. **24** (2000) pp.195-211.
[3] S.-C. Liu, *et al.*, Neural Networks. **14** (2001) pp.629-643.
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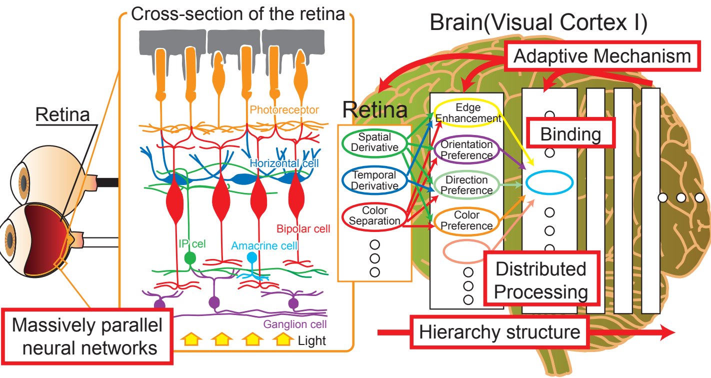
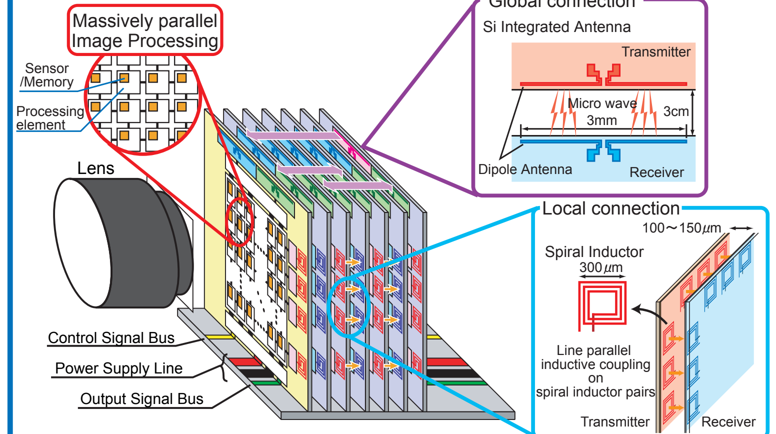
Vertebrate visual system



The vertebrate visual system processes visual information extraction and its binding by massively parallel neural network arranged hierarchically in real-time and adapts to a rapidly changing visual environment by an adaptive mechanism.

Visual processing system using 3-Dimensional Custom-Stack System



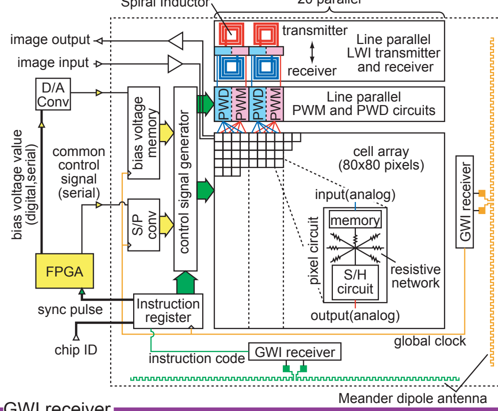
Power of the 3-D integration is demonstrated by engineering realization of the architecture and algorithm of the vertebrate visual system

Visual processing chip using the 3DCSS configuration

A visual processing chip, a 3DCSS chip, was developed to configure the 3DCSS.

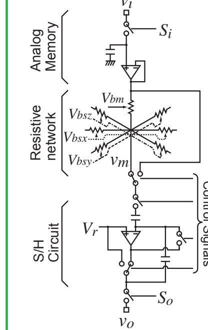
- Cell array : massively parallel image processing
- GWI circuit : global chip control by transmitting instruction code
- LWI circuits, PWM and PWD circuits : high speed data transfer by line parallel arrangement

Block diagram of the 3DCSS chip



The 3DCSS chip can be applied to processing mimicked vertebrate visual system due to the resistive network and the PWD circuit, etc.

Pixel circuit



- Image smoothing by the resistive network
- Pattern-noise compensation & input image subtraction by the S/H circuit

GWI receiver

The GWI receiver is used to get an instruction code, which determines operations of each chip, for example, processing and transmitting methods.

Block diagram of the GWI receiver

Meander dipole antenna
g2 g1 LNA
I2 I1
MIX (Integrator)
m2 m1
Amp
am ap
compalator
cout
out
GWI receiver

Spice simulation

[V]
g1, g2: 1.70 — 20mV
I1, I2: 3.3, 3.2 — 175mV
m2, m1: 1.90, 1.82 — 80mV
ap, am: 1.9, 1.7 — 275mV
cout: 2.0, 1.0 — 1.4V
xout: 3.3, 0.0 — 3.3V
0 delay = 4ns 10 20 [ns]

2GHz ASK signal → 100MHz inverted pulse signal

Another circuits

Instruction register

An instruction code from a GWI receiver is fed into the instruction register in sync with a global clock from another GWI receiver.

The register of each chip has unique ID number, and thus, can store a different instruction code.

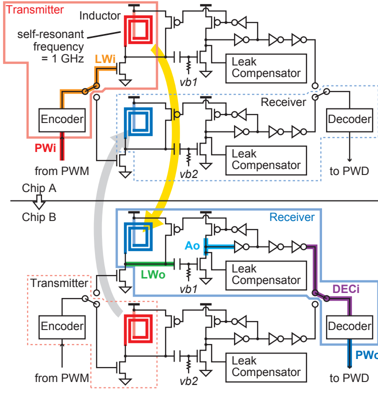
Control signal generator

The generator generates control signals to the cell array, the PWM and the PWD circuits by combining the instruction code of each chip and common control signal, which generates an off-chip FPGA circuit.

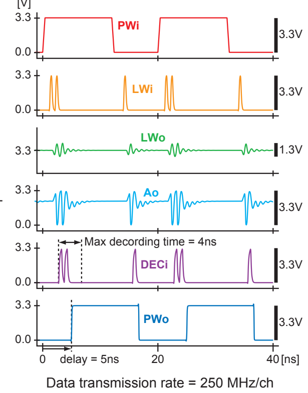
LWI transmitter and receiver

A pulse width signal from the pixel circuit is transferred from the LWI transmitter to the LWI receiver between adjacent chips by using inductive coupling. And then, the received signal is fed into the pixel circuit.

Block diagram of the LWI circuit



Spice simulation

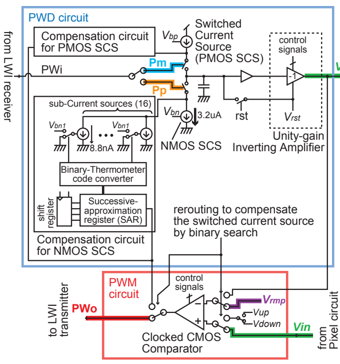


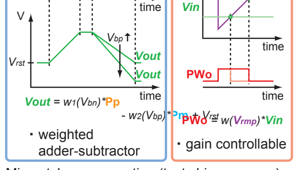
Data transmission rate = 250 MHz/ch

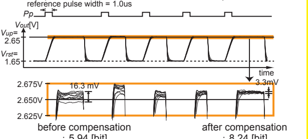
PWM and PWD circuits

An analog output from the cell array must be converted into a digital data in order to use the LWI circuits. The PWM circuit modulates the analog output to a pulse width signal, and the PWD circuit demodurates. The PWM circuit was embedded a compensation circuit of the current source mismatches.

Block diagram of the PWM and PWD circuits







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Power consumption[*2]	5.6 [mW/cell] (transmitter + receiver)

PWM & PWD circuit

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Resolution	8 [bit]
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GWI receiver circuit

Antenna length	8010 [um]
Size[*1]	858.1(H) x 820.0(V) [um^2]
Power consumption	40 [mW]

Pixel circuit

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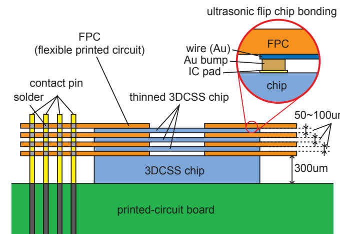
Development of the 3DCSS test module

A 3DCSS test module using 3DCSS chip was developed by ultrasonic flip chip bonding process.



Cross section of the 3DCSS test module

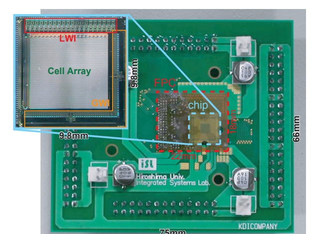


Photo graph of the 3DCSS test module

Presently, we conduct verification experiments for the 3DCSS test module.