A Layout Method of 20GHz Global Clock Distribution

Mitsuru Shiozaki, Atsushi Mori, Atsushi Iwata and Mamoru Sasaki

Integrated Systems Laboratory, Graduate School of Advanced Sciences of Matter
Hiroshima University, Kagamiyama 1-4-1, Higashihiroshima-shi, 739-8527 JAPAN

Introduction

Global clock distribution has become increasingly difficult for multi-GHz microprocessors. Timing uncertainty must reduce with clock period, but skew and jitter are proportional to latency, which does not scale with clock period for conventional H-trees. In addition, clock power consumption affects the total power reduction because the clock signal is most active signal.

Aiming at realization of low-skew, low-jitter, low-power consumption in multi-GHz clocking, we designed the 20GHz global clock distribution in a 0.18um, 1.8V digital CMOS technology. The key of the clock distribution is reducing power consumption by using passive devices and distributed constant transmission lines. On 20GHz operation, parasitic capacitances or parasitic resistances also affect an increasing of power supply consumption. So, the layout that reduces parasitic component is very important. In this paper, we explain 20GHz global clock distribution, and the reduction method of parasitic components.

20GHz Global Clock Distribution

Figure 1 shows a clock distribution architecture. It has the grid structure of differential transmission line, and inductors and cross-coupled oscillators are put on cross sections of the grid lines. Inductors and transmission lines determine the oscillating frequency. The cross-coupled oscillators provide enough gain to compensate for wire losses.

The 20GHz – 6 X 6 grid global clock distribution was designed in a 0.18um, 1.8V digital CMOS technology. Figure 2 shows a layout of the global clock distribution. The size of the clock distribution network is 2mm X 2mm. The clock distribution includes the 36 inductors and cross-coupled oscillators. Differential transmission lines use 6th metal layer, and VDD and GND lines use 2nd and 1st metal layer, respectively. The transmission line length between inductors is 400um. The width and space of differential transmission lines is 5um and 2um, respectively. Figure 3 shows a layout of inductor and cross-coupled oscillators. The inductor uses 4th and 5th metal layer, and the outside diameter and internal diameter is 70um and 50um, respectively. MOSFETs for the cross-coupled oscillator are distributed around inductor.

In circuit simulation at multi-GHz, considering the parasitic resistance and parasitic capacitance is indispensable [1]. Especially, the tradeoff between the gate resistance and the parasitic capacitance of the cross-coupled lines is very important. For example, the width of finger transistor needs to be kept small to lower the gate resistance, while the parasitic capacitance may increase due to more fingers.

Layout Method for 20GHz Operation

First, the following simulations were carried out for 1 to 1 connection. Inductors, differential transmission lines and VDD-GND lines were modeled as 2-port S-parameter models, 4-port S-parameter models and 2-port S-parameter models analyzed by using electromagnetic field solver, respectively. And, RC extraction data were used for cross-coupled oscillators.

Figure 4 (a) and 5 (a) shows layouts of the cross-coupled transistor and the simulation result before layout modification, respectively. Considering the fact that the parasitic capacitance increases when the number of fingers increases more, the finger width of 0.9um is chosen as an adequate value. As compared with target clock-period (42ps), the clock period has been increased to 47ps due to extracted RC components. The main factor is parasitic capacitance (11fF) between the cross-coupled lines, including parallel parasitic capacitance of the spiral inductor. Especially, the parasitic capacitance between the same layers is dominant, as shown in Figure 4 (a). So, it is effective to detach the lines in same layers or to use different layers for closed lines. In the layout modification, the 1st metal layer has been moved to 3rd metal layer in case of closed lines. As a result, the parasitic capacitance has been approximately reduced to half, as shown in Figure 4 (b). The modification can be also carried out with small overhead on chip area. Figure 5 (b) shows the simulation result after the layout modification. The clock-period of 3% and the amplitude of 50mV have been improved. It is difficult to improve this by other methods. For example, in order to improve 50mV amplitude without any layout modification, increment of several milliampere in bias current is required. This means that the power consumption is greatly decreased by the layout modifications.

Conclusions

We designed the 20GHz global clock distribution circuit in a 0.18um, 1.8V digital CMOS technology. The key of the clock distribution is reducing power consumption by using passive devices and distributed constant transmission lines. At 20GHz, the layout with considerations of parasitic component and their tradeoff is important.

References

[1] Changhua Cao and Kenneth K. O “A 90-GHz Voltage-Controlled Oscillator with a 2.2-GHz Tuning Range in a 130-nm CMOS Technology,” Symposium on VLSI Circuits, Digest of Technical Papers, pp. 242-243, June 2005

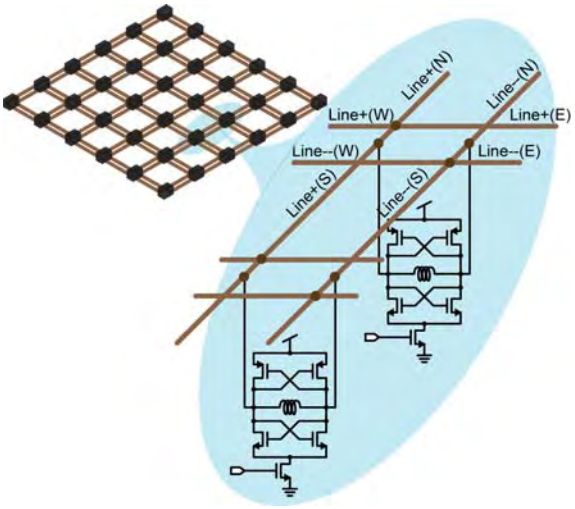

Fig. 1 Basic architecture of global clock distribution.

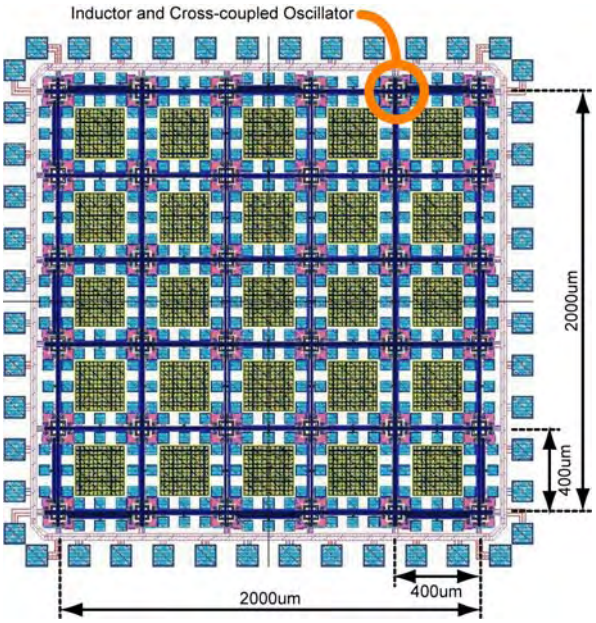

Fig. 2 20GHz – 6 X 6 grid global clock distribution.

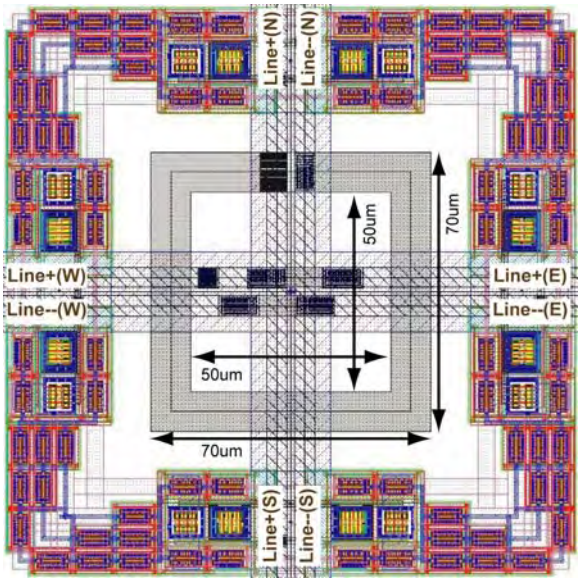

Fig. 3 Inductor and cross-coupled oscillator..

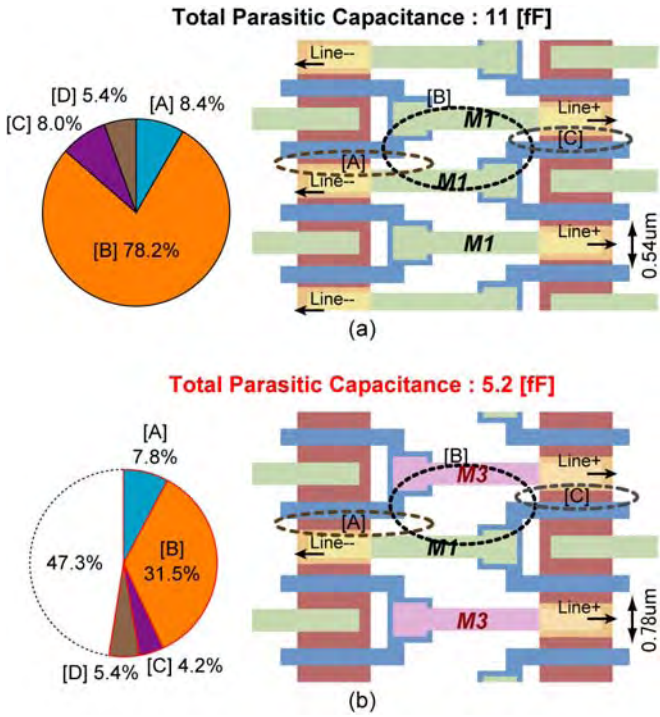

Fig. 4 The proportion of the parasitic capacitance.

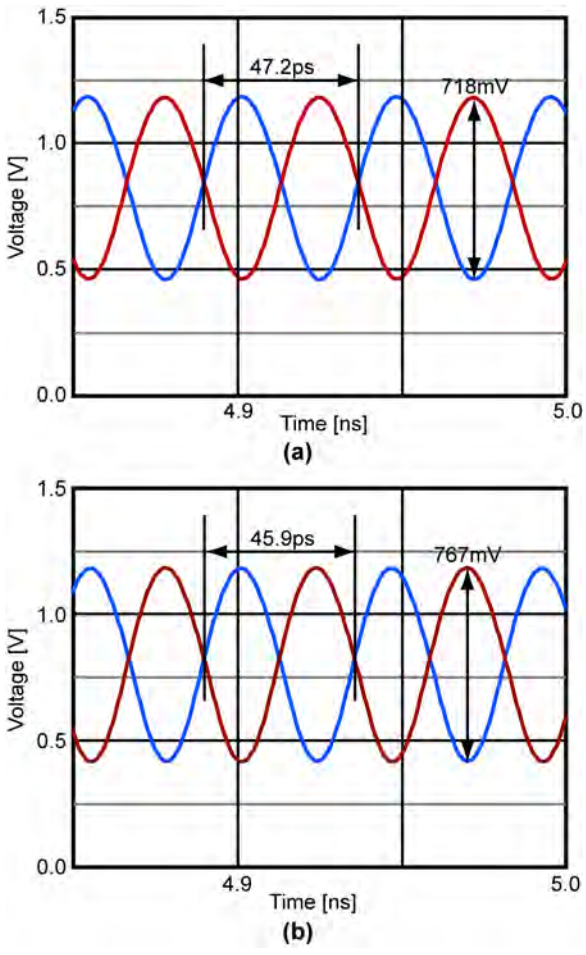

Fig. 5 Simulation results.

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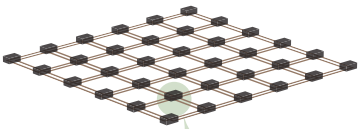
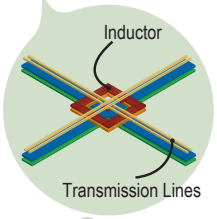
Generate and distribute clock signals to every latch and clocked dynamic gate





[Goals]

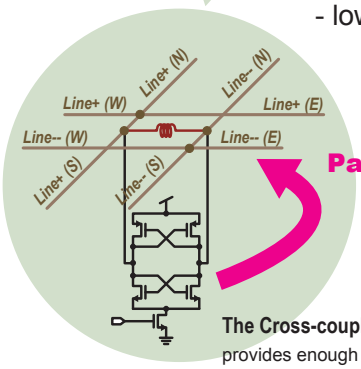
- Simultaneous everywhere (no skew)
- Periodic everywhere (no jitter)
- Use minimum power and resources

[Approachs]

- Using passive devices and distributed constant transmission lines (Inductor + Standing Wave)
- Layout that reduces parasitic component

[Target]

- 20GHz Clocking Network
- mesh size is 400μm
- low-latency

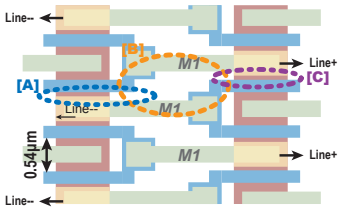


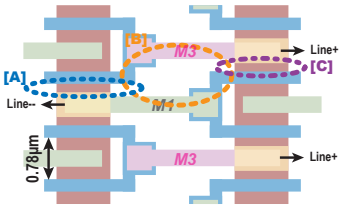
Parasitic Components

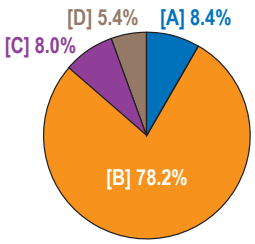
- Inductor Size
- Power Consumption

The Cross-coupled Ocillator
provides enough gain to compensate for wire losses.

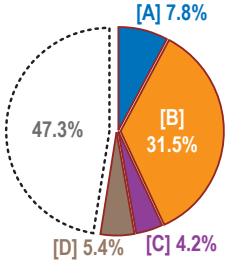
Decreasing of Parasitic Capacitance



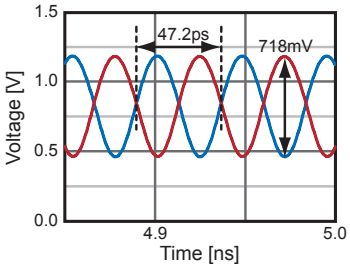




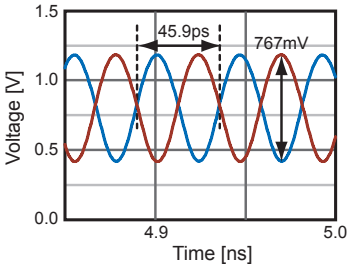
Parasitic Resistance (Contact resistance) increases 5%.



Total Parasitic Capacitance : 11 [fF]



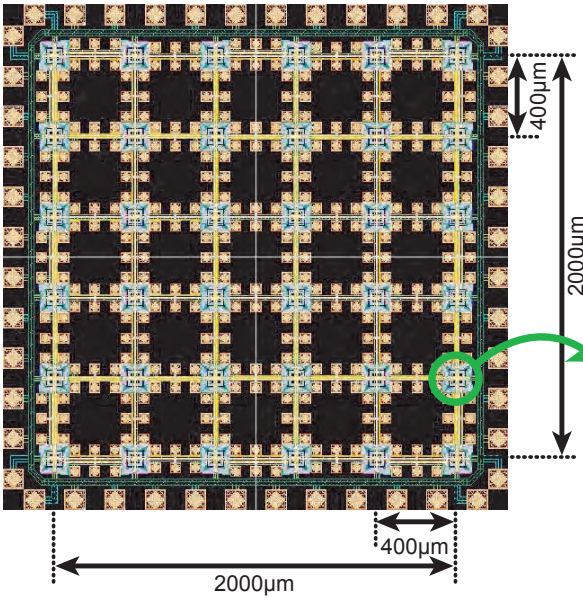
Total Parasitic Capacitance : 5.2 [fF]

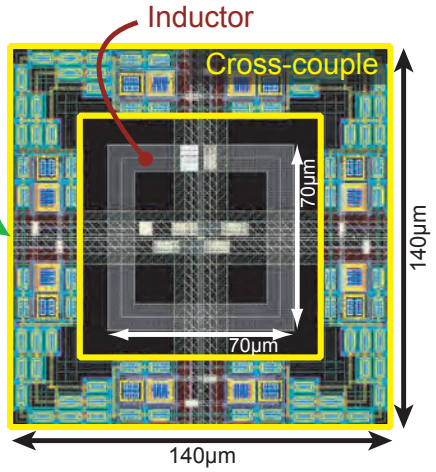


* For example, in order to improve 50mV amplitude without any layout modification, increment of several milliampere in bias current is required.

Tradeoff of Parasitic Components

	Resistance	Capacitance
Increasing of Finger Width	↓	↑
Increasing of Spaces between Lines	↑	↓





【20GHz Global Clock Distribution】 TSMC 0.18μm, 1.8V Digital CMOS

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