A CMOS RF Front-End using Radiation Oscillator for Short-Range Wireless Communication

Toru Mukai, Atsushi Iwata and Mamoru Sasaki
Graduate School of Advanced Sciences of Matter, Hiroshima University
E-Mail: {toru, iwa, sasaki}@dsl.hiroshima-u.ac.jp

Introduction

The recent downsizing of CMOS technology enables monolithic integrated millimeter-wave circuits applicable to sensor and communication systems. The combination of active devices with passive planar structures, including also antenna elements, allows single-chip realizations of complete millimeter-wave front-ends. This paper describes a simple architecture of quasi-millimeter-wave CMOS RF front-end. In the architecture, only one circuit block based on radiation oscillator can carry out whole functions in transceiver. In order to confirm the feasibility of the architecture, the prototype circuit has been designed and fabricated in a 0.18-μm CMOS technology. 100Mbps data rate and 8.11mW power consumption on 20GHz carrier frequency can be achieved.

Architecture

A. Electro-Magnetic Fed Patch Antenna

Fig. 1 shows a structure of the RF front-end. A patch antenna is implemented above IC chip. Fig. 2 shows a relationship between radiation efficiency η and dielectric thickness t of typical patch antenna. λ_0 is the free space wavelength. As shown in Fig. 2, t/λ_0 thicker than 0.1 is required in order to achieve sufficient radiation efficiency. However, it is impossible to fabricate such a thick dielectric layer in conventional CMOS technology. In order to overcome the problem, patch and dielectric layer are stacked in post-process to ensure enough dielectric thickness. Only the ground plane of patch antenna is implemented with top metal layer in the CMOS technology. In order to feed the power from IC chip to the patch with no through-hole-via, an inductive coupling between the patch and a slot in the ground plane is employed.

B. Radiation Oscillator

Fig. 3 shows a circuit diagram of the radiation oscillator. In the oscillator, the antenna is used as both a radiator and a resonator. The cross-coupled MOSFETs M1 and M2 implement a negative resistance.

C. On/Off Keying Modulation

On/Off Keying (OOK) modulation is employed for digital communication. It is realized with switching two states, oscillation and non-oscillation, by MOSFETs M3 and M4. According to transmitting data, the gates of M3 and M4 are controlled and the circuit state is switched into oscillation or non-oscillation.

D. Super-Regeneration

In receiver operation, super-regeneration technique is employed, in order to amplify the received wave and demodulate the OOK signals. The negative resistance value of the cross-coupled MOSFETs M1 and M2 is tuned by the bias voltages Vgate and it is set to the critical point (which means the boundary between oscillation and non-oscillation). In the above condition, the oscillation starts if it receives RF signal having same frequency as the oscillator. A following simple circuit detects the oscillation and demodulates it to digital data

As described above, the front-end circuit has a simple structure that merges many functions of oscillator, modulator, demodulator and radiator. Impedance mismatch and insertion loss in connections of several blocks are serious problems in millimeter-wave systems. The connectionless structure is very effective in millimeter-wave RF circuits.

Circuit Configuration and Simulation

Fig. 4 shows a simplified model of a radiation oscillator, for circuit design. Both the device and the antenna are modeled with Y-parameters because they are connected in parallel. "$Y_a = G_a + jS_a$" and "$Y_d = G_d + jS_d$" are admittances of the antenna and the device, respectively. The oscillation condition can be described as follows.

$$G = G_a + G_d \leq 0$$
$$S = S_d + S_a = 0$$

A test chip was fabricated in a 0.18-μm CMOS technology. The chip micrograph is shown in Fig. 5. The butterfly shape slot in the top metal couples the device and the patch antenna, without any through-hole-via. Y-parameters of the antenna and the device designed in test chip are shown in Fig. 6. It is able to recognize that the oscillation frequency is 19.7 GHz, from the above analysis.

The patch antenna is designed using 3-dimensional electro-magnetic solver. The electro-magnetic solver typically outputs only S-parameters. However, it cannot be used in transient circuit simulation. In the design, 7th order transfer function is calculated from the S-parameters and it is used as a time-domain antenna model.

Fig. 7 shows a result of the SPICE transient simulation of the receiver. A situation is assumed, where the transmission distance and the data rate are 1.5m and 100Mbps, respectively. The digital data can be demodulated as shown in Fig.7. In this condition, power consumption of receiver circuit is 8.11mW. Specification of the test-chip is shown in Table I.

Conclusion

In this paper, we proposed a CMOS RF front-end architecture based on radiation oscillator. With employing OOK modulation and super-regeneration technique, circuits are simplified and power consumption is reduced. Data communication at 100Mbps on 1.5m distance has been confirmed by SPICE simulation. In the next step, we will measure the test chip, and demonstrate the validity of this architecture.

References

[1] P. Russer, "Si and SiGe Millimeter-Wave Integrated Circuits," *IEEE Trans. on Microwave Theory and Techniques*, vol. 46, pp. 590-603, 1998.

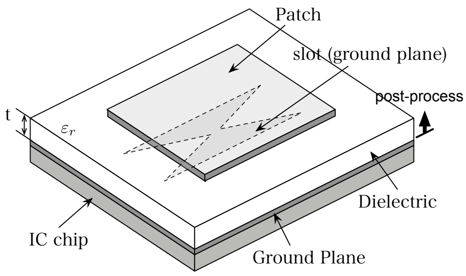


Fig. 1 Structure of the RF Front-end.

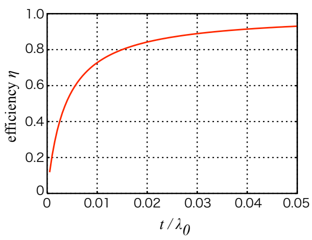


Fig. 2 Radiation efficiency of patch antenna vs. dielectric thickness.

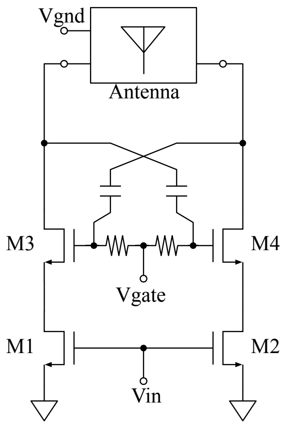


Fig. 3 Radiation oscillator.

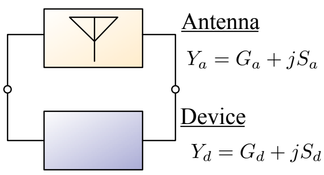


Fig. 4 Simplified circuit model.

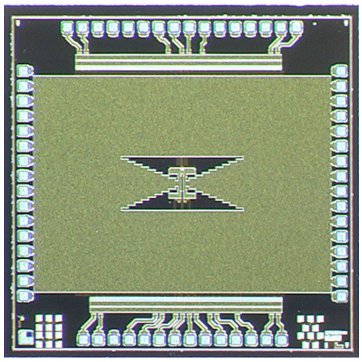


Fig. 5 Chip micrograph

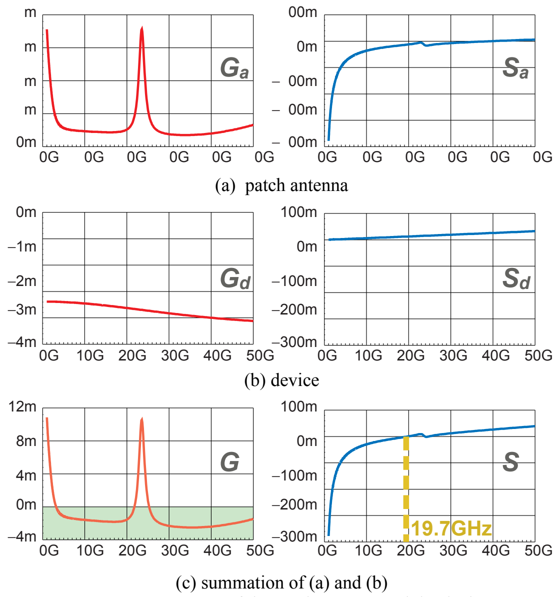


Fig. 6 Y-parameters of the patch antenna and the device.

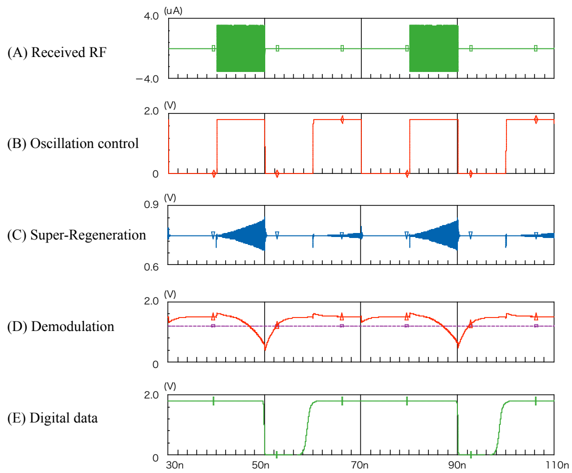


Fig. 7 Simulation result of super-regeneration receiver (100Mbps, 1.5m).

Table. I Specification of the test-chip.

Technology			0.18μm CMOS (5M)
Power consumption	Transmitter (max)		20mW
	Receiver	Super-regeneration	8mW
		Demodulation	110uW
Data rate			100Mbps
Transmission distance (max)			1.5m
Maximum directivity			2.475
Radiation efficiency			0.15

A CMOS Front-End using Radiation Oscillator for Short-Range Wireless Communication

Toru Mukai, Atsushi Iwata and Mamoru Sasaki
Graduate School of Advanced Science of Matter, Hiroshima University

Background

Downsizing of CMOS Technology

→ monolithic integrated millimeter-wave circuits

Millimeter-wave

Capability of wideband Communications

High atmospheric attenuation

Suitable for Short-Range Communication

Single-chip Transceiver Architecture

EM-Fed Patch antenna above IC chip

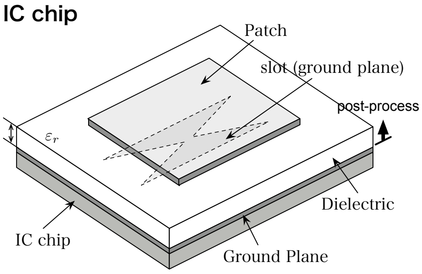
- No-through-hole-via Feeding

Higher Radiation Efficiency

Radiation Oscillator

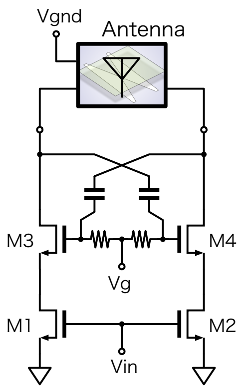
- On/Off Keying
- Super-Regeneration

Small circuit area, Low Power



Single-chip Transceiver

Modeling and Analysis



Radiation Oscillator Circuit

Radiation Oscillator

Using an antenna as a resonator

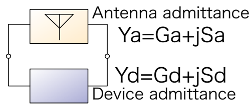
Varying bias voltages
→ enables **On/Off Keying Modulation** and **super-regeneration**

Many Functions in A Single Circuit

Antenna Modeling

7th-order Transmission Function
calculated from the result of Electro-magnetic Simulation (Ansoft HFSS)

Circuit Modeling

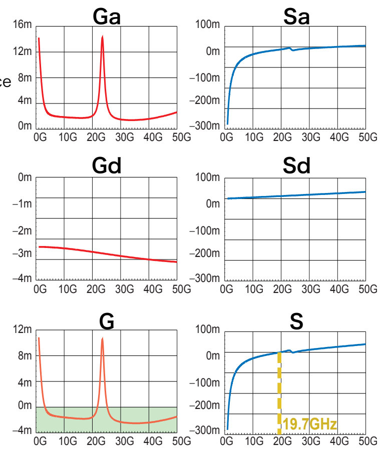


Simplified circuit model

$$G = Ga + Gd$$
$$S = Sa + Sd$$

Oscillating Condition

$$Ga + Gd \leqq 0$$
$$Sa + Sd = 0$$



Circuit Analysis

Transmission Simulation

Simulation Condition

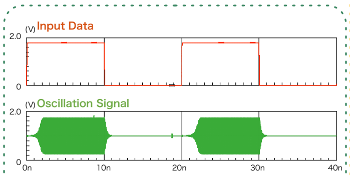
Data Rate: 100Mbps
Distance: 1.5m

Transmitter mode

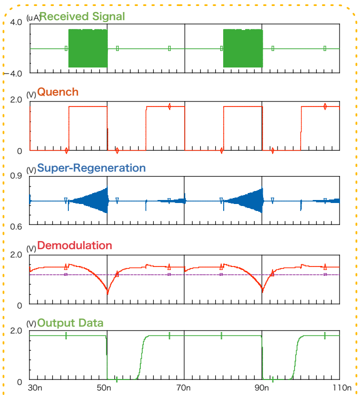
Input Data to Vin (OOK Modulation)

Receiver mode

Set Vgnd to critical point
(between Oscillation and non-Oscillation)
Input Quench to Vin (Super-regeneration)



Transmitting Simulation



Receiving Simulation

Test-Chip

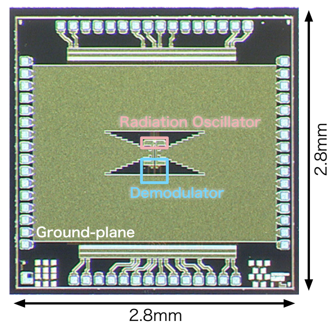
Test-chip Specification

Technology : 0.18μm CMOS(5M)
Power consumption
transmitter : 20mW(max)
super-regeneration : 8mW
Demodulation : 110μW
Data rate : 100Mbps
Transmission distance : 1.5m

Antenna

Patch size : 1800μm × 2400μm
Slot size : 500μm × 1000μm
Dielectric thickness : 300μm

Maximum directivity : 2.475
Radiation efficiency : 0.15



Chip Micrograph

Conclusion and Future plan

A CMOS RF front-end architecture based on radiation oscillator was proposed.
Data communication at 100Mbps on 1.5m distance has been confirmed by simulation.

We will measure the test chip, and demonstrate the validity of this architecture.