A 1V Supply Low Noise CMOS Amplifier Using Noise Reduction Technique of Autozeroing and Chopper Stabilization

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Abstract

A low-noise CMOS amplifier operating at a 1-V supply voltage is developed using the two noise reduction techniques of autozeroing and chopper stabilization. The proposed amplifier utilizes a feedback with virtual grounded input-switches and a multiple-output switched op-amp. The low-noise amplifier fabricated by a 0.18-µm CMOS technology was measured at a 1-V power supply, and achieved low noise performance of 50-nV/√Hz input noise at 1-MHz chopping frequency.

Introduction

Recently, sensor chips using a mixed-signal CMOS technology have been applied for sensing and monitoring biological functions [1-2]. The low-noise amplifier is one of the most significant circuits in the sensor chip because of detecting small level signals. However the increasing of dc offset voltage (Voff) and flicker noise (Vfn) becomes a serious problem in scaled CMOS technologies.

The autozeroing and chopper stabilization technique are used for reducing these noises [3]. The principle of these techniques is illustrated in Fig.1and2. The autozeroing technique samples the dc offset (Voff) and 1/f noise (Vfn), at phase Φ1. And then subtracts the sampled noise from input signal at phase Φ2. The autozeroing technique can reduce the low-frequency noise of amplifier. Although the autozeroing technique increases baseband noise floor caused by aliasing inherent in the sampling process (Fig.3(b)). The chopper stabilization technique converts the frequency range of input signal to a higher corner frequency, and then demodulates it back to the baseband after amplification. Although the large energy is presented at a chopping frequency (fc) due to the low-frequency noise (Fig .3(c)). The chopper stabilization technique equipped with the low pass filter (LPF) can provide the clean output signal. Using both autozeroing and chopper stabilization techniques enable a reduction of the baseband noise floor and the modulated noise at the chopper frequency (Fig .3(d)) [4].

However these noise reduction techniques using floating analog switches are not suitable for operating at a low supply voltage.

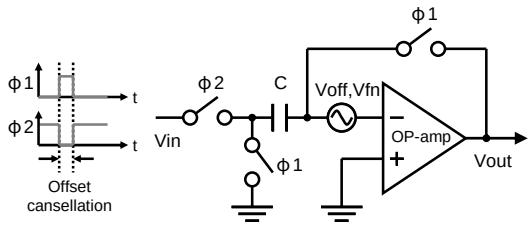


Fig. 1 Principle of Autozeroing technique

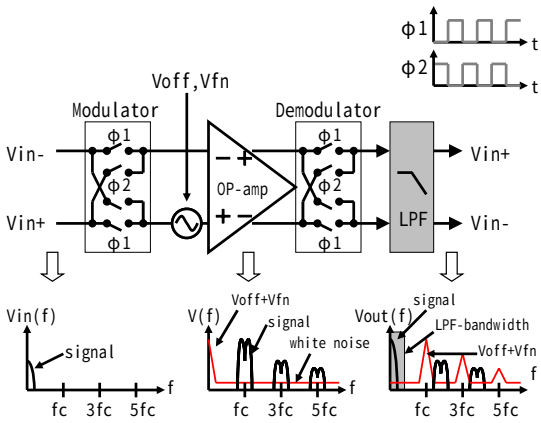


Fig. 2 Principle of Chopper Stabilization technique

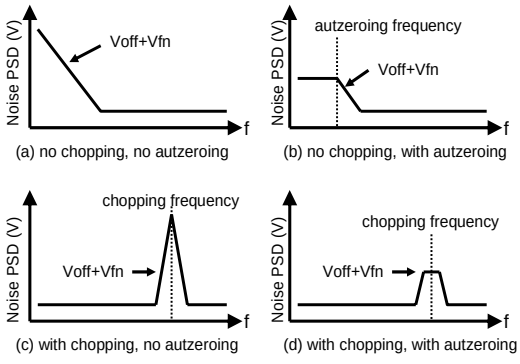


Fig. 3 PSD using noise reduction technique

Circuit Design

Figure 4 shows a equivalent circuit of the low-noise amplifier using autozeroing and chopper stabilization technique operating at a low supply voltage.

The chopper modulators (CHP1, CHP2) placed with the virtual ground are implemented by simple analog switches. Because a voltage level of virtual ground is possible to set to any level and input signal amplitude is small. On the other hand, the demodulator CHP3 placed outside the virtual ground is impossible to constitute analog switches because of large output amplitude. Therefore the CHP3 is implemented by the SWOPA. The CHP1, CHP2 and CHP3 are switched by the complementally clock signals of phase Φ1 and phase Φ2.

The multi-output SWOPA can configure the autozeroing scheme. During the phase Φ0, the output of SWOPA are connected to its input using dotted lines as shown in Fig. 4, so that it forms a voltage follower. The detected dc offset voltage is sampled into the hold capacitor C2; accordingly, the autozeroing operation cancels the dc offset. If the offset sampling is periodically, low-frequency noise also can be reduced.

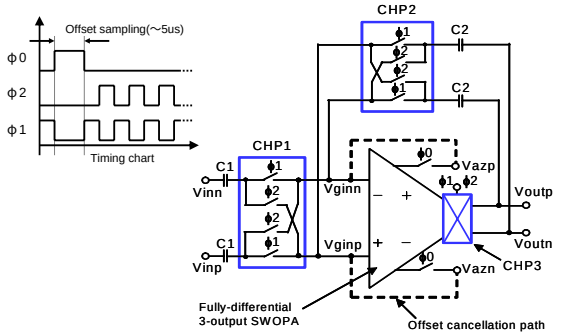
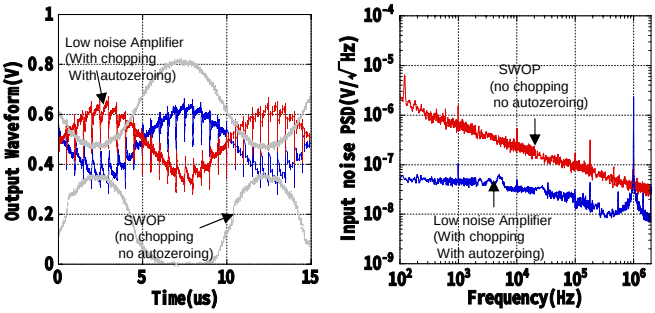


Fig. 4 A equivalent circuit of The low-noise amplifier using autozeroing and chopper stabilization techniques

Experimental Results

A test chip of the low-noise amplifier using chopper stabilization and autozeroing technique is fabricated with a 0.18-μm CMOS process (Vthn = 0.42 V, Vthp = 0.5 V).The measurements are shown in Fig. 5. The low-noise amplifier operated with 1-MHz chopping frequency and 5-μs autozeroing time at a supply voltage of 1 V. The input noise of SWOPA shows a typical 1/f noise spectrum, and the noise PSD is 2.5-μV/√Hz at 100 Hz. The proposed low-noise amplifier suppressed the noise PSD to less than 50 nV / √Hz.



(a) Output Waveform (b) Input noise PSD

Fig. 5 Measurements

Conclusion

In this paper, we presented a 1-V supply low-noise amplifier using autozeroing and chopper stabilization technique. The key technique of noise reduction at a low supply voltage is multi-output switched op-amp and chopper modulator implementation in the virtual ground. The low-noise amplifier fabricated with a 0.18-μm CMOS technology was measured at a 1-V power supply, and achieved low noise performance of 50-nV/√Hz input noise at 1-MHz chopping frequency.

References

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～ Background ～

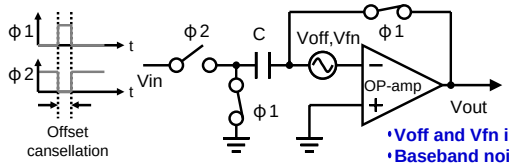
Recently, sensor chips use a mixed-signal CMOS technology. The low-noise amplifier is one of the most significant circuits in the sensor chip. However the increasing of dc offset voltage (Voff) and flicker noise (Vfn) becomes a serious problem in scaled CMOS technologies.

～ Noise Reduction Technique ～

Noise reduction techniques
- Autozeroing technique
- Chopper stabilization technique

<Autozeroing technique>

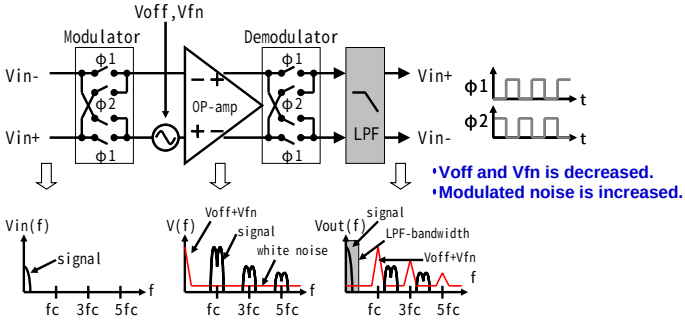
Phase Φ1 ：The dc offset (Voff) and 1/f noise (Vfn) is sampled.
Phase Φ2 ：The sampled noise is subtracted from input signal.



- **Voff and Vfn is decreased.**
- **Baseband noise floor caused by aliasing is increased.**

Principle of Autozeroing technique

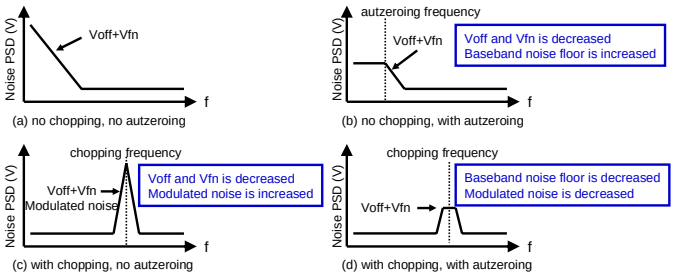
<Chopper stabilization technique>



- **Voff and Vfn is decreased.**
- **Modulated noise is increased.**

Principle of Chopper Stabilization technique

<Using both Autozeroing and Chopper stabilization>

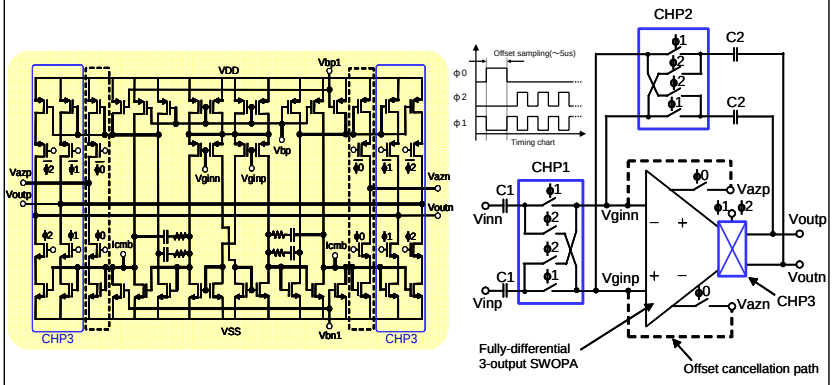


Using both autozeroing and chopper stabilization techniques is effective for noise reduction.

Noise reduction techniques using floating analog switches ⇒Unsuitable for operating at a low supply voltage

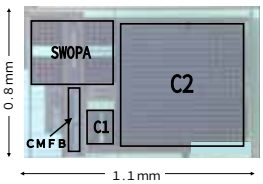
～ Circuit Design ～

Key technique of noise reduction at a low supply voltage
- Multi-output switched op-amp
- Chopper modulator placed in the virtual ground

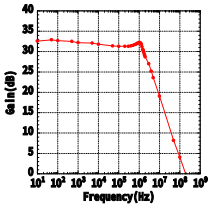


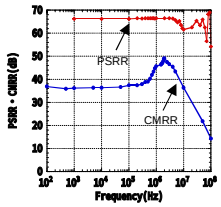
- **Chopper modulators (CHP1, CHP2) placed with the virtual ground**
  ➜By simple analog switches
- **CHP3 is implemented by the SWOPA**
- **The multi-output SWOPA can configure the autozeroing scheme.**

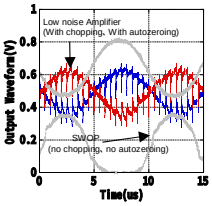
～ Experimental Results ～

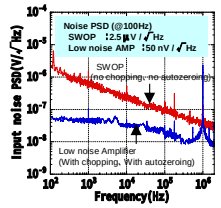


Microphotograph









0.18μm CMOS process
(Vthn = 0.42 V, Vthp = 0.5 V)
Supply voltage 1V
Chopping frequency 1MHz、
Autozeroing time 5μs

～ Conclusion ～

We presented a 1-V supply low-noise amplifier using autozeroing and chopper stabilization technique.

- Key technique
  Multi-output switched op-amp
  Chopper modulator implementation in the virtual ground
- Achievement of the low-noise amplifier
  1-V power supply
  50-nV/√Hz input noise at 1-MHz chopping frequency