Fully-Parallel Associative Memory Architecture Realizing Minimum Euclidean Distance Search

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Abstract

Associative memories are beneficial in intelligent information processing for purposes such as pattern matching for object recognition. In a fully-parallel associative memory, the stored reference data is compared with input data by checking the distance according to a distance measure. The reference data with the minimum distance is called winner. For this pattern matching process the Euclidean distance measure is most desirable, because it correctly represents the distance between two points in an N-dimensional vector space. Here, a fully-parallel associative memory architecture is proposed which searches the winner based on the minimum Euclidean distance between input pattern and previously stored reference patterns.

1. Introduction

An associative memory system with searching capability for the minimum distance is a major part of attention in the field of information processing like image compression and pattern recognition [1]. An associative memory can perform recognition by means of computing the distances between an incoming pattern and stored reference patterns. Architectures for fully-parallel Hamming distance search [2] and winner-search according to the Manhattan distance [3] have been proposed. Both Hamming and Manhattan distance can be represented by,

$$D = \sum_{i=1}^{w} |S_i - R_i|$$

where, $S = \{S_1, S_2, \ldots, S_w\}$ and $R = \{R_1, R_2, \ldots, R_w\}$ are input and reference data, respectively. D is called the Hamming distance, when S_i and R_i are 1-bit binaries. D is called the Manhattan distance, when S_i and R_i are n-bit binaries (n>1). A more desirable distance measure used in many effective algorithms for real applications is however the Euclidean distance, which is represented by,

$$D_e = \sqrt{\sum_{i=1}^{w} (S_i - R_i)^2}$$

Euclidean distance gives the correct distance between two points in vector space and is therefore more accurate than the Manhattan distance. A number of circuits for implementing Euclidean distance in hardware are presented in the literature [4-5]. However a major drawback of most circuits is their limited range of operation and relatively large size. Euclidean distance hardware written in VHDL proposed in [6], is a sequential one. It uses a completely digital circuit consisting of multiplier, adder, register and square root circuits and requires a huge number of transistors making it not suitable for fully-parallel associative memory hardware. Euclidean distance computation circuits generally require the square operation and the complicated square root operation. Therefore, a practical solution for a fully-parallel associative memory, which requires many Euclidean-distance computation circuits for performing the parallel minimum Euclidean-distance search, does not exist. In this paper, a novel fully-parallel associative memory architecture is proposed, which uses a mixed digital-analog Euclidean-distance calculation circuit for searching the winner.

2. Associative Memory Architecture for Minimum Euclidean Distance Search

For solving the problem of finding the pattern with the nearest Euclidean distance it is sufficient to compare square distances only. This is possible, because in pattern matching only comparing of the relative magnitude of the distances is necessary and because the square root does not change this relative magnitude. Therefore, the circuitry for calculating the square roots can be avoided.

The structural blocks of the proposed compact associative memory with fully-parallel match capability according to the Euclidean distance is shown in Fig. 1. The main functional units are search-data storage circuit, row/column decoder and read/write circuit, the memory field, winner-line-up amplifier (WLA) and winner-take-all circuit (WTA). This architecture has been used previously [3] to realize an associative memory with minimum Manhattan-distance search capability. The extension to Euclidean-distance search deals with the analog part from unit-comparison circuit (UC) in the memory field up to the winner-take-all circuit (WTA). This analog part constitutes a multi-stage minimum-distance-search circuit. At the output of the WTA a transformation to digital output signals is carried out, indicating whether the reference pattern of the respective row is the winner or loser.

Architecture of the proposed Euclidean distance search memory field is shown in Fig. 2. Here the digital k-bit subtractor and absolute value calculation units compare the W binaries, each with k-bit, in all rows of the memory field in parallel with the reference data. The digital output of the subtractor is then converted into analog current using a current converter (CC). To realize the CC function the gates of the CC-transistors are connected to the corresponding k-bit output-signal lines of the unit comparator and their drains are connected together to add the analog currents of all CC-transistors. The width of each CC-transistor, $2^{k-1}\times W_0$, varies depending on its bit position in the binary so as to correctly distinguish the weight of each bit. The analog currents from each CC are then squared using analog current squarer circuits (Fig. 3) [7], which exploit the square-law characteristics of the MOS transistor drain current as a function of gate voltage, when operated in the saturation region. Finally, the output currents from all squarer circuits are added to get a Euclidean distance equivalent current.

In the associative memory core, the match lines are processed through analog circuits (WLA) that pre-amplify the match lines and restrict the large variety of possible analog outputs to a small range by self-regulation. The WLA amplifies the differences of current signals between winner and losers and regulates the winner signal to a suitable level for further distance amplification. The results are then fed to a WTA network for recognizing the winner and the losers precisely.

The initial job of the WTA circuit is to amplify winner-loser distances by voltage-current-voltage transformations. In order to reduce the negative effects from fabrication induced miss-match of corresponding transistors in different rows and to improve the reliability for large winner-input distances, 5 stages of the common-source WTA-configuration is used. The final decision circuit in WTA consists of inverters with an adjusted switching threshold. It generates a "1" for the winner row and a "0" for each loser row.

The correct function and the performance of the proposed architecture is confirmed using HSPICE simulation (0.35µm technology) for 128 reference patterns with 16 binaries each 5-bit long. Simulated winner-search time of the proposed architecture as a function of the distance between winner and input-data word for distances of 1, 2 and 5 between winner and nearest-loser row is shown in Fig. 4. The circuit successfully finds the winner for a wide range of input-winner distances.

3. Conclusion

In this paper we have proposed a fully-parallel associative memory architecture realizing minimum Euclidean distance search which uses a mixed digital-analog Euclidean-distance calculation circuit and a fast analog winner search circuit and verified the architecture by circuit simulation. Using an analog squarer circuit for realizing the Euclidean distance function makes the system compact and easy to realize in hardware.

Future work includes the design, measurement and evaluation of a test chip and verification of the usefulness of the fully-parallel associative memory by designing a complete application system.

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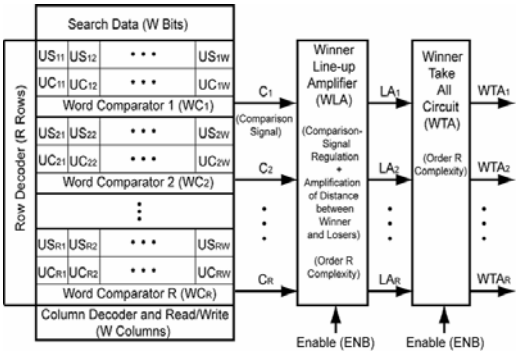

Fig. 1. Construction of the Fully-parallel Associative Memory.

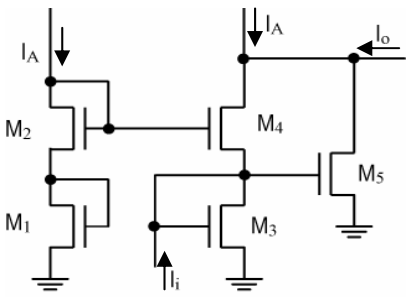

Fig. 3. Analog Current Squarer Circuit

References

[1] D. R. Tveter, "The Pattern Recognition Basis of Artificial Intelligence," Los Alamitos, CA: IEEE computer society, 1998.

[2] H. J. Mattausch, T. Gyohten, Y. Soda, and T. Koide, "Compact Associative-Memory Architecture with Fully-Parallel Search Capability for the Minimum Hamming Distance," IEEE Journal of Solid-State Circuits, Vol. 37, pp. 218-227, 2002.

[3] Y. Yano, T. Koide and H. J. Mattausch, "Fully parrallel nearest Manhattan-distance search memory with large reference-pattern number," Extended abstract of the Int. Conf. on Solid State Devices and Materials (SSDM'2002) pp. 254-255, 2002.

[4] O. Landolt, E. Vittoz and P. Heim, "CMOS Selfbiased Euclidean Distance Computing Circuit with Highdynamic Range," *Electron. Lett.*, vol. 28, pp. 352–354, 1992.

[5] O. Landolt, E. Vittoz and P. Heim, "CMOS Selfbiased Euclidean Distance Computing Circuit with Highdynamic Range," *Electron. Lett.*, vol. 28, pp. 352–354, 1992.

[6] M. Freeman, M. Weeks and J. Austin, "Hardware Implementation of Similarity Functions," IADIS International Conference on Applied Computing, Algarve, Portugal, vol. 2, pp. 329-332, 2005.

[7] B.D.Liu, C.Y.Huang and H.Y.Wu, "Modular current-mode defuzzification circuit for fuzzy logic controllers," Electron. Lett., vol. 30, no. 16, pp. 1287-1288, Aug. 1994.

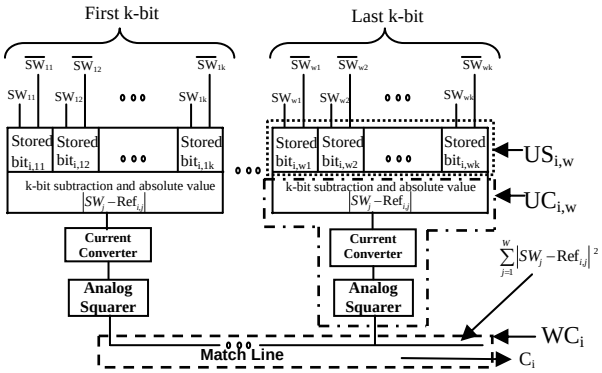

Fig. 2. Euclidean Distance Search Associative Memory Architecture.

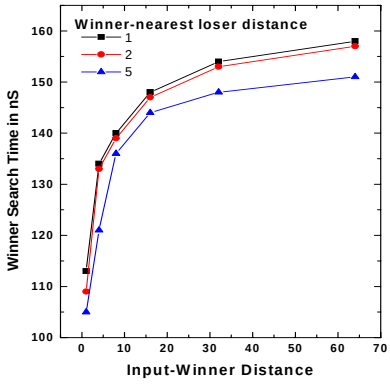

Fig. 4. Winner Search Time

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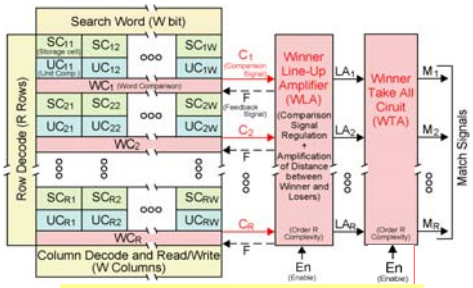
Nanoelectronics for Tera-bit Information Processing

Introduction

Associative Memory Functionality

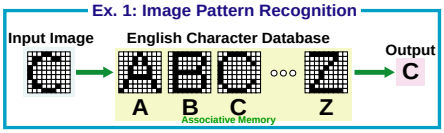
- Find the nearest match for an input-data of W bit length among R reference data words.
- Nearest match (winner) in an Associative Memory operation is determined by the minimum with respect to a distance measure.



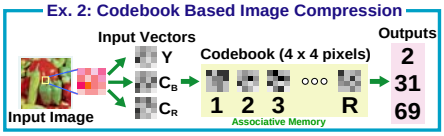
Fully-parallel Associative Memory Architecture

Application Examples:

Ex. 1: Image Pattern Recognition



Ex. 2: Codebook Based Image Compression

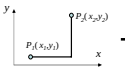


Distance Measures

1. Hamming: The number of positions in two strings of equal length for which the corresponding elements are different.

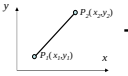
If A = 1 0 1 1 1 0 1 and B = 1 0 0 1 0 0 1 → Hamming distance between A and B is 2

2. Manhattan: Distance between two points measured along axes at right angles.



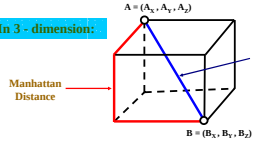
$$D_m = |x_1 - x_2| + |y_1 - y_2|$$

3. Euclidean: The straight line distance between two points.



$$D_e = \sqrt{(x_1 - x_2)^2 + (y_1 - y_2)^2}$$

In 3 - dimension:



$$D_m = |A_x - B_x| + |A_y - B_y| + |A_z - B_z|$$

$$D_e = \sqrt{(A_x - B_x)^2 + (A_y - B_y)^2 + (A_z - B_z)^2}$$

D_1	D_2	D_3	Manhattan Distance $D_m = D_1 + D_2 + D_3$	Euclidean Distance $D_e = \sqrt{D_1^2 + D_2^2 + D_3^2}$	Squared Euclidean Distance $D_{se} = D_1^2 + D_2^2 + D_3^2$
3	2	2	7	4.12	17
1	4	3	8	5.10	26
2	5	1	8	5.48	30
4	2	4	10	6.00	36
1	6	2	9	6.40	41

- Euclidean distance correctly represents the distance between two points and is more accurate than Manhattan distance.
- In content-based image retrieval systems Euclidean distance gives better result to determine the similarities between a pair of images.

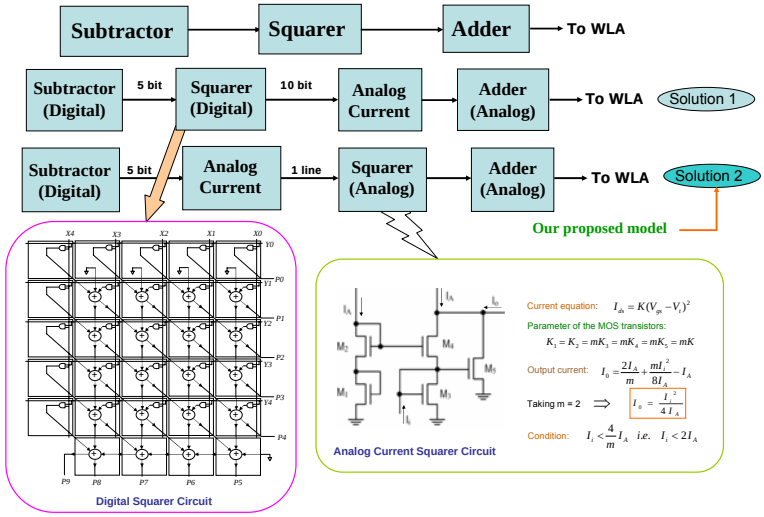
Euclidean Distance Measure Implementation

Distance Measure Manipulation:

- In pattern matching only comparing the relative magnitude of the distances is sufficient.
- The square root does not change this relative magnitude.
- So, the circuitry for calculating the square roots can be avoided.

If $\sqrt{(A^2 + B^2)} > \sqrt{(C^2 + D^2)}$ then $(A^2 + B^2) > (C^2 + D^2)$

Hardware Implementation:



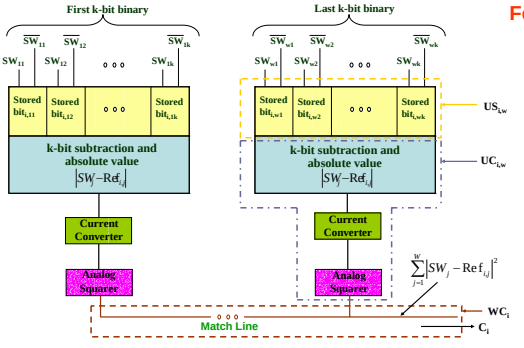
Digital Squarer Circuit

Analog Current Squarer Circuit

Proposed Architecture

Structure of the memory part:

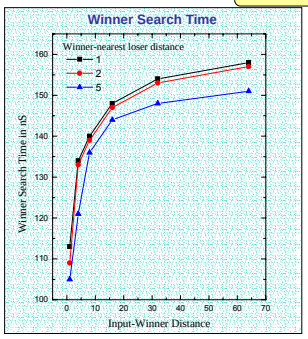
- **Unit storage cells** store the reference patterns data. They are implemented with 6 transistor SRAM cells.
- **Unit comparators** are composed with k-bit subtraction and absolute value calculation unit, digital distance to analog current converter and analog current squarer circuit.
- The output currents from all squarer circuits are added in the **Word comparator** unit to get a Euclidean distance equivalent current.

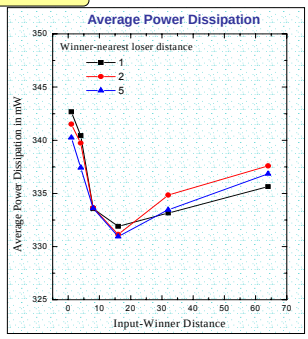


Features:

- All unit comparators and word comparators calculate the distance between input pattern and stored reference patterns in parallel.
- Fast analog word comparison (e.g. comparison result encoded as static current-sink capability.)
- Analog squarer circuit for realizing the Euclidean distance function makes the system compact and easy to realize in hardware.
- Winner search circuitry scales only linear with the number of reference words R (O(R) complexity).

Simulation Results





Distance Measure	Euclidean Distance 16, 5-bit Binaries
Winner-N. Loser Distance	1(One), 2 (Two) and 5(Five)
Reference Patterns	128
Technology	0.35 µm CMOS

- Winner search time is between 105 and 160 nS.
- Average power dissipation of the total circuit is less than 343 mW.

Conclusion and Future works

Conclusion:

- Associative memory architecture with fully-parallel search capability for minimum Euclidean distance is proposed.
- The performance of the associative memory circuit where the Euclidean distance is minimum has been verified by HSPICE circuit simulation using 0.35 µm CMOS technology for 16, 5-bit binaries with 128 reference patterns.
- The circuit successfully finds the winner for a wide range of input-winner distances.

Future works:

- Design, measurement and evaluation of a test chip.
- Verification of the usefulness of the fully-parallel associative memory by designing a complete application system.