The Development of UWB Gaussian Monocycle Pulse Synchronization Circuit based on 0.18-µm CMOS Technology

Nobuo Sasaki, Pran Kanai Saha and Takamaro Kikkawa
Research Center for Nanodevices and Systems, Hiroshima University
Phone: +81-82-424-6265, Fax: +81-82-424-3499
E-mail: { nsasaki, kikkawa }@sxsys.hiroshima-u.ac.jp

1. Introduction

RF wireless clock/data transmission using integrated antenna, capacitor or inductor is the newly developed technology for intra/inter-chip interconnection in future ULSI [1][2]. As for data transmissions among stacked ULSI modules (Fig.1) [3], both high data transmission rate and multi-channel accessibilities are required. UWB (Ultra-Wide-Band) technology is one of the solutions of this problem [4]. The goal of the research is the development of 1Gbps, single-chip, and CMOS UWB transceiver using Gaussian monocycle pulse (GMP) as a transmitted waveform [5]. In the receiver side, amplifier and demodulator, which is based on pulse correlation method, have been already developed, and measurement results will be presented in IWUWBT 2005. However, the synchronization between transmitter and receiver remains as an unsolved problem. In this paper, GMP synchronization scheme is verified using MATLAB/Simulink simulation, and circuit level simulations by HSPICE are also shown.

2. Synchronization Scheme

The block diagram of the proposed synchronization circuit is shown in Fig. 2. The synchronization scheme consists of two steps, *i.e.*, (i) phase synchronization and (ii) frequency synchronization. The circuit receives the following GMP $r(t)$, which is the first derivative of Gaussian.

$$r(t) = -\left(\frac{2\pi t}{\tau}\right) e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2} \tag{1}$$

Here τ denotes the pulse width of GMP. Mixer and integrator circuits give the correlation between the received signal $r(t)$ and template signal $v_1(t)$. Here $v_1(t)$ should have the same waveform as $r(t)$. The phase of $v_1(t)$ is shifted until the value of the correlation exceed the threshold V_{th} .

$$\int_{-T}^{T} r(t)\cdot v_1(t-\Delta t_i)\,dt = \begin{cases} \geq V_{th} \rightarrow \Delta t_{i+1} = \Delta t_i \equiv \Delta t_{locked} \\ < V_{th} \rightarrow \Delta t_{i+1} = \Delta t_i + \delta t \end{cases} \tag{2}$$

Here δt is the unit delay, and Δt_i shows the amount of time shift. After phase synchronization, frequency synchronization is performed. The second derivative of Gaussian is given as another template signal $v_2(t)$.

$$v_2(t) = \left\{\left(\frac{2\pi t}{\tau}\right)^2 - 1\right\} e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2} \tag{3}$$

Another correlation circuit performs the correlation between $r(t)$ and $v_2(t)$. The output voltage ΔV_{LO} is used to control the repetition frequency of the local oscillator f_{LO}.

$$\Delta V_{LO} \propto \int_{-T}^{T} r(t)\cdot v_2(t-\Delta t_{locked})\,dt \begin{cases} > 0 \rightarrow \Delta f_{LO} > 0 \\ = 0 \rightarrow \Delta f_{LO} = 0 \\ < 0 \rightarrow \Delta f_{LO} < 0 \end{cases} \tag{4}$$

Here an orthogonality relation between $r(t)$ and $v_2(t)$ is used.

3. Circuit Design and Simulation

Above synchronization algorithm is verified using MATLAB/Simulink calculation. Figure 3 is the results of Simulink simulation. Where the repetition frequency of synchronization circuit is given as 1GHz, and the difference of the repetition frequency between transmitter and receiver is assumed as 1MHz. The center frequency of GMP is 5GHz. In this condition, the unit delay of DLL should be at least less than the pulse width of GMP (=0.2ns). This time, 1GHz, differential 8 stages VCO, which can generate different 16 phases, is designed and simulated. Corresponding unit delay is about 63ps. This value satisfies above requirement. Whole circuit layout of the phase synchronization circuit, which is developed using TSMC CMOS 0.18-µm process, is given in Fig.4. The schematic diagram of the delay cell of this ring oscillator is given in Fig.5.(a). HSPICE result of the VCO is shown in Fig. 6. (a). Repetition frequency becomes 960MHz. After 8 to 1differential multiplexer, a part of its schematic is shown in Fig. 5. (b), repetition frequency downs to 790MHz.

Figure 5. (c) shows a schematic of the 4 bit counter, which is used as the delay controller. Simulation results are given in Fig. 6. (b).

4. Summary

The new synchronization scheme for Gaussian monocycle pulse was developed. MATLAB/Simulink results indicate that delay cells at least below 200ps are necessary. HSPICE simulation of phase synchronization circuit was demonstrated. The VCO repetition frequency after multiplexer was 790MHz.

References

[1] A. B. M. H. Rashid, S. Watanabe and T. Kikkawa, IEEE Electron Device Letters, 23 (2003) pp.731-733.

[2] N. Miura, D. Mizoguchi, M. Inoue, H. Tsuji, T. Sakurai, and T. Kuroda, ISSCC Dig. Tech. Papers (2005), pp. 264-265.

[3] Atsushi Iwata, Mamoru Sasaki, Takamaro Kikkawa, Seiji Kameda, Hiroshi Ando, Kentaro Kimoto, Daisuke Arizono and Hideo Sunami, ISSCC Dig. Tech. Papers (2005), pp. 262-263.

[4] M. Z. Win and R. Scholtz, IEEE Trans. on Communications. 48 (2000) pp. 679-691.

[5] Pran Kanai Saha, Nobuo Sasaki and Takamaro Kikkawa, Proceedings of ISSSTA 2004, (2003) pp. 962-966

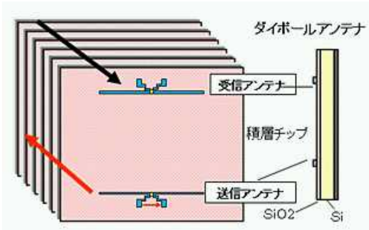


Fig. 1. Conceptual figure of inter-chip wireless interconnections using integrated dipole antennas.

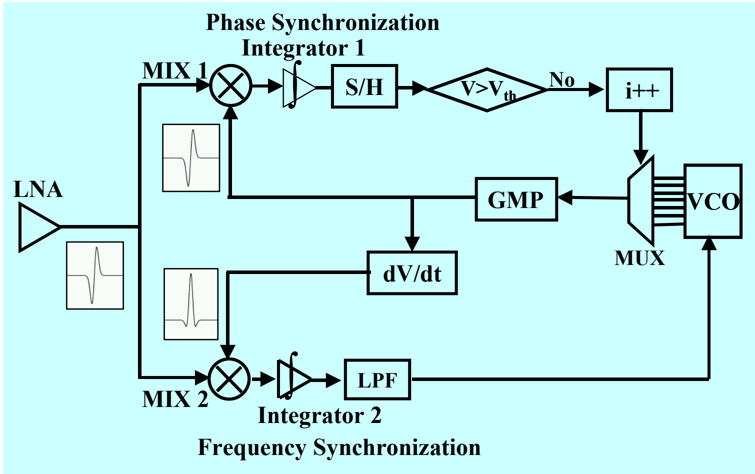


Fig.2. The block diagram of the proposed synchronization circuit.

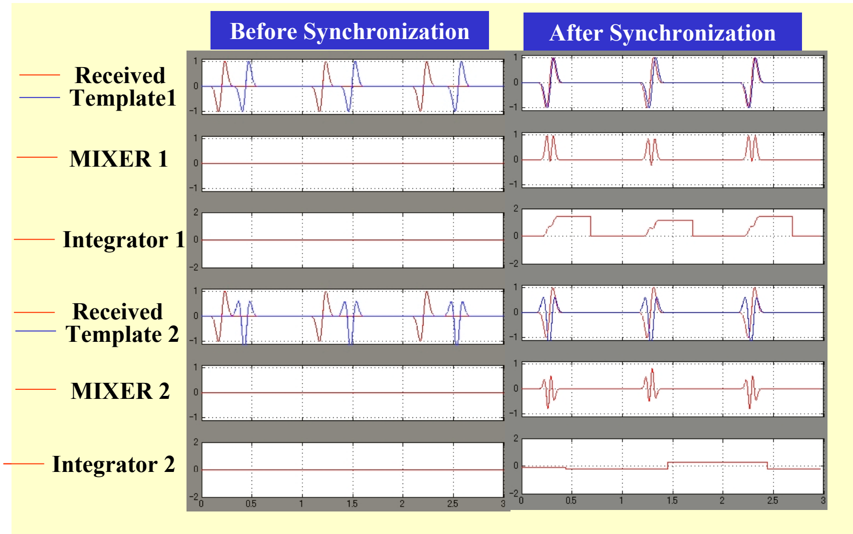


Fig. 3. Simulation results of synchronization scheme using MATLAB/Simulink.

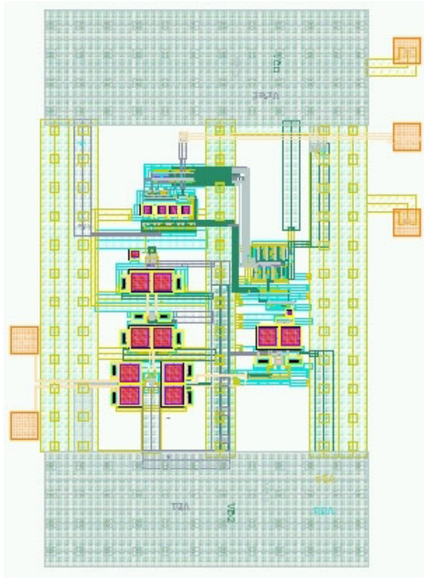


Fig.4. Chip layout of synchronization circuit.

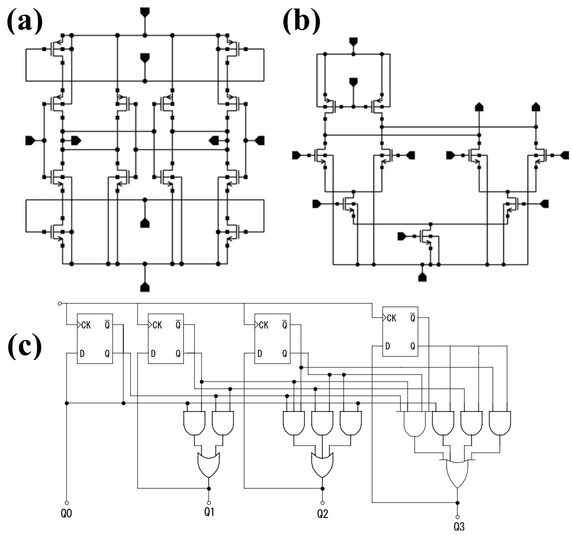


Fig. 5. Schematic diagram of (a) 8 stages VCO delay cell. (b) 2 to 1 multiplexer. (c) 4bit counter.

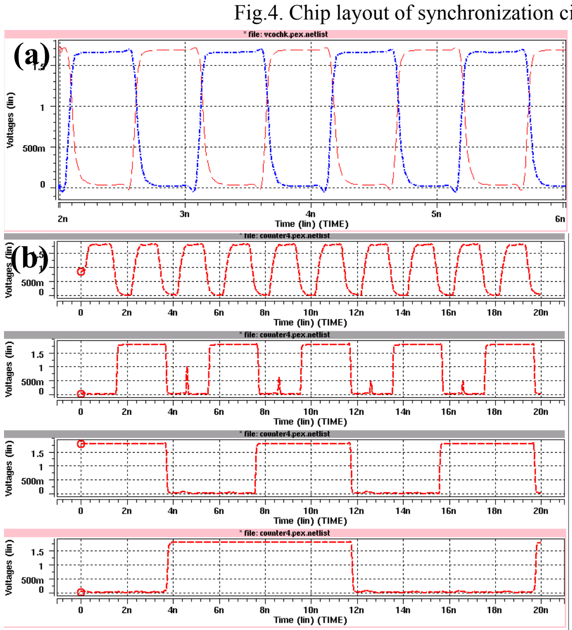


Fig.6. HSPICE results. (a) VCO output (repetition frequency 960MHz). (b) 4bit counter output.

P-20

The Development of UWB Gaussian Monocycle Pulse Synchronization Circuit based on 0.18-µm CMOS Technology

Nobuo Sasaki, Pran Kanai Saha and Takamaro Kikkawa

Research Center for Nanodevices and Systems, Hiroshima University
1-4-2 Kagamiyama, Higashi-Hiroshima, 739-8527 Japan
E-mail: {nsasaki, kikkawa}@sxsys.hiroshima-u.ac.jp

RCNS Hiroshima University

Wireless Inter-chip Interconnection

Signal Delay Due to RC → Serious Problem for Future ULSI

Solutions

- Copper/low-k Interconnection → Limitation from Materials
- RF Wireless Technology → Re-configurable Interconnection

Goal

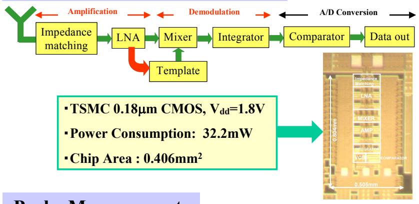
- Development of On-Chip Wireless Interconnections for High Speed Clock/Data Transmission.
- Pulse-based UWB → Multiple Accessibility

Target Performance

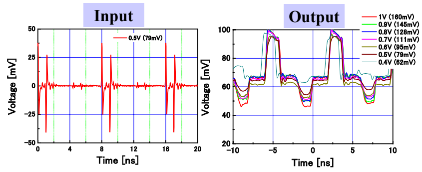
- Single Chip
- 1Gbps Data Rate (Single Channel)
- Target Distance : 1mm ～ 1cm

Previous Achievement

Block Diagram of UWB Receiver



Probe Measurements



Improvement of Receiver

Previous Circuit

- Succeeded in the demodulation of OOK modulated Gaussian Monocycle Pulse
- LNA output was used as template signal to avoid the synchronization problems

Improvement

- Development of synchronization circuit for Gaussian Monocycle Pulse (GMP)
  1. Phase synchronization
  2. Frequency synchronization

Synchronization Algorithm

1. Phase Synchronization

- Received signal $r(t)$: Gaussian Monocycle Pulse
- Template signal 1 $v_1(t)$: Same waveform as $r(t)$

$$r(t) = v_1(t) = -\left(\frac{2\pi t}{\tau}\right) e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2}$$

- Mixer + Integrator → Correlation between $r(t)$ and $v_1(t)$

$$\int_{-T}^{T} r(t)\cdot v_1(t-\Delta t_i)\,dt = \begin{cases} \geq V_{th} \rightarrow \Delta t_{i+1} = \Delta t_i \equiv \Delta t_{locked} \\ < V_{th} \rightarrow \Delta t_{i+1} = \Delta t_i + \delta t \end{cases}$$

Where V_{th}: Threshold voltage, δt : Unit delay

Δt_i : Time shift

2. Frequency Synchronization using orthogonality

- Received signal $r(t)$: Gaussian Monocycle Pulse
- Template signal 2 $v_2(t)$: $dr(t)/dt$

$$v_2(t) = \left\{\left(\frac{2\pi t}{\tau}\right)^2 - 1\right\} e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2}$$

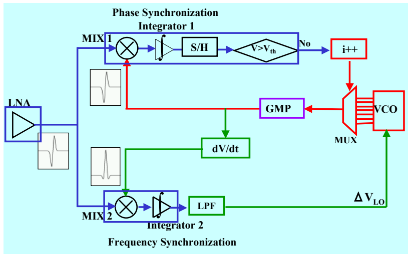
- Mixer + Integrator → Correlation between $r(t)$ and $v_2(t)$

$$\Delta V_{LO} \propto \int_{-T}^{T} r(t)\cdot v_2(t-\Delta t_{locked})\,dt \begin{cases} > 0 \rightarrow \Delta f_{LO} > 0 \\ = 0 \rightarrow \Delta f_{LO} = 0 \\ < 0 \rightarrow \Delta f_{LO} < 0 \end{cases}$$

Where ΔV_{LO}: Control voltage variation of local oscillator

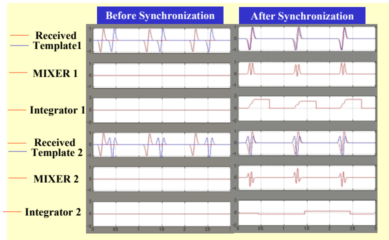
Δf_{LO} : Frequency variation of local oscillator

Circuit Block Diagram



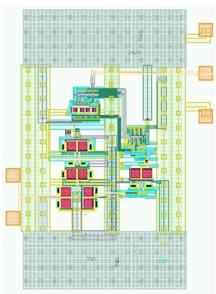
Previous work | This work | Poster 22 | Next issue

MATLAB Simulation

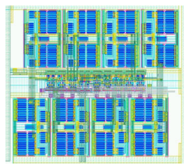


Simulation Condition:
f_{LO} (Rx)=1GHz, f_{LO} (Tx)=1.001GHz
The center frequency of GMP f_c=5GHz
Unit delay δt = 65ps

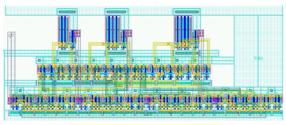
Phase Synchronization Circuit



Whole Circuit

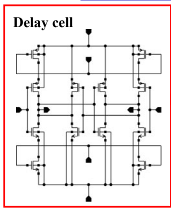


VCO+MUX

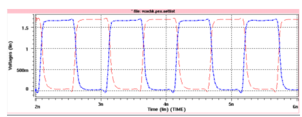


4bit Counter

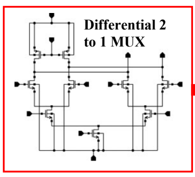
Differential VCO



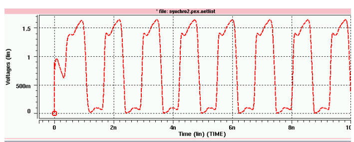
- 8 stage
- Differential
- f=960MHz
- Unit delay 65ps



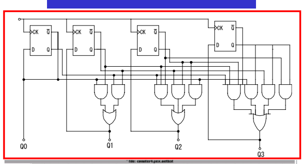
Differential 8 to 1 Multiplexer

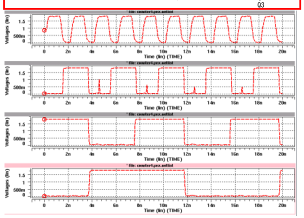


- Differential
- f=790MHz after MUX
- Unit delay 79ps



4 bit Counter





Summary

- The new synchronization scheme for Gaussian monocycle pulse was developed.
- MATLAB/Simulink results indicate that delay cells at least below 200ps are necessary.
- HSPICE simulation of phase synchronization circuit was demonstrated. The VCO repetition frequency after multiplexer was 790MHz.

21st COE the 4th Int. Workshop
September 16, 2005. Hiroshima, JAPAN